MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX109

Low Voltage, Full Duplex CVSD CODEC with Serial Control

ADVANCE INFORMATION

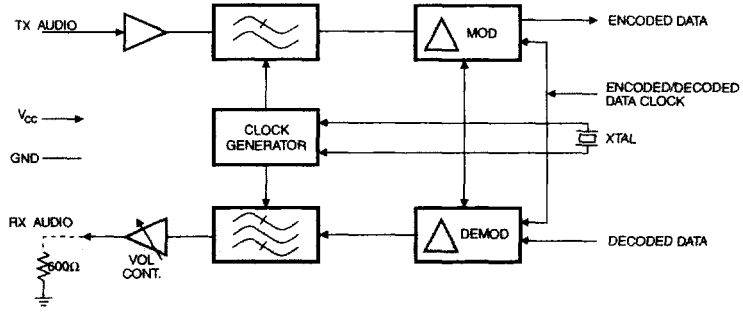
Shipping JUNE 1997

Features

- **Single Chip Full Duplex CVSD CODEC**
- **On-chip Input and Output Filters**
- **On-chip Volume Control**
- **Low Power, Single Supply analog CMOS**
- **Wide Frequency Reference using Ceramic Oscillator**

Applications

- **Digital Cordless Phones**
- **Digital PCN/PCS Systems**
- **Digital Delay Lines**
- **Digital Voice Storage**
- **Multiplexers**
- **Switches and Phones**
- **Time Domain Scramblers**



The MX109 is a CVSD (Continuously Variable Slope Delta Modulation) Codec. A low-power CMOS device, designed for use in cordless telephones, the MX109 is also suitable for applications in delta multiplexers, switches and phones, and Time Domain Scrambling. The encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be externally injected in the 8k to 64k bps range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal or ceramic resonator.

The encoder has an enable function for use in multiplexer applications and when disabled, the encoder output remains in a high-impedance "tri-state" mode.

The MX109 is available in 16-pin PDIP (MX109P), and 16-pin SOIC (MX109DW) packages.

www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

Doc. # 20480121.005

CONTENTS

Section **Page**

 www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

1. Block Diagram

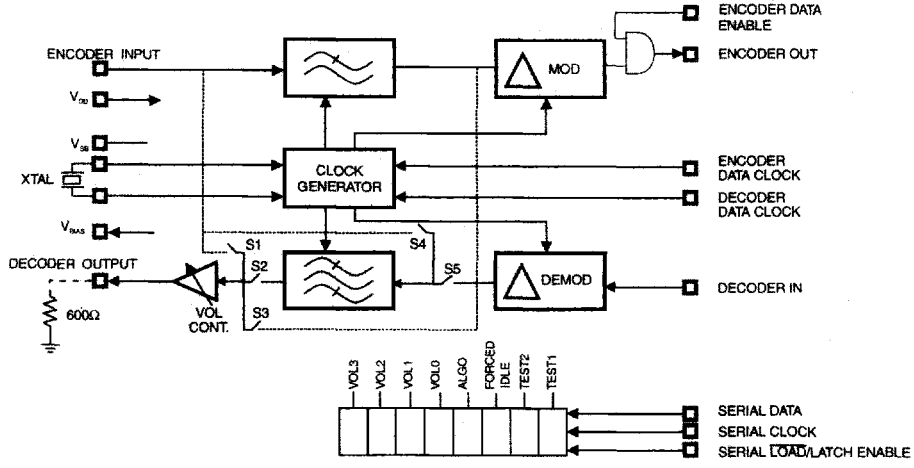


Figure 1: Device Block Diagram

Note: The state of S1-S5 is controlled via Test 1 and Test 2 according to Table 4

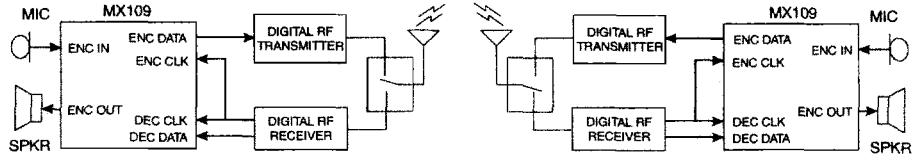


Figure 2: Typical Wireless System Incorporating the MX109

 www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

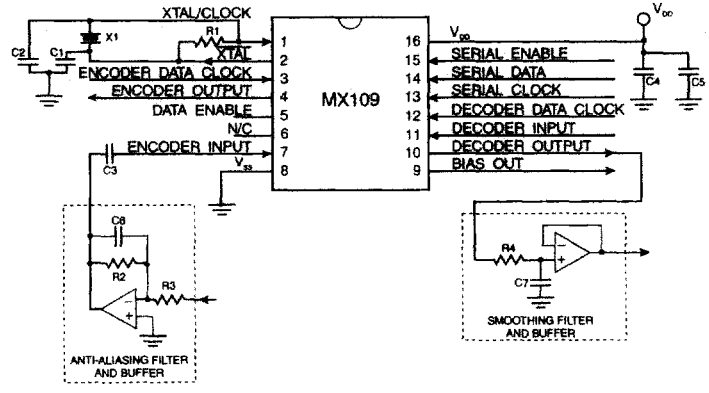
2. Signal List

Pin No.	Name	Type	Description
1	Xtal/Clock	Input	Input to the clock oscillator inverter. A 3.58 MHz Xtal input or externally derived clock is injected here. See Figure 3.
2	$\overline{\text{Xtal}}$	Output	The 3.58 MHz output of the clock oscillator inverter.
3	Encoder Data Clock		A logic port. External encode clock input.
4	Encoder Output	Output	The encoder digital output.
5	Encoder Data Enable	Input	Data is made available at the encoder output pin by control of this input. Internal 1MΩ pullup.
6	N/C		No internal Connection
7	Encoder Input	Input	The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
8	V_{SS}	Power	Negative Supply, normally ground potential
9	V_{BIAS}	Output	Buffered $V_{DD}/2$.
10	Decoder Output	Output	The recovered analog signal is output at this pin. It is the buffered output of a bandpass filter and requires external components
11	Decoder Input	Input	The received digital signal input. Internal 1 MΩ pullup
12	Decoder Data Clock	Input	A logic port. External decode clock input
13	Serial Clock	Output	This is the serial clock input
14	Serial Data	Input	This is the serial data input. Data is loaded in the following order: VOL3, VOL2, VOL1, VOL0, ALGO, FORCE IDLE, TEST 2, TEST 1
15	Serial $\overline{\text{Load}}$/Latch Enable	Input	A logic 1 applied to this input will enable serial programming
16	V_{DD}	Power	Positive Supply

www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

Doc. # 20480121.005

3. External Components



R1	Note 1	1MΩ	±10%
R2		10kΩ	±10%
R3		10kΩ	±10%
R4		10kΩ	±10%
C1	Note 2	33pF	±20%
C2	Note 2	27pF	±20%

C3	Note 3	1.0µF	±20%
C4	Note 4	0.47µF	±20%
C5		0.001µF	±20%
C6		0.0022µF	±20%
C7		0.0022µF	±20%
X1	Note 5	3.58MHz	

Figure 3: Recommended External Components

External Component Notes:

1. Oscillator inverter bias resistor.
2. Xtal circuit load capacitor.
3. Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with an even lower source impedance.
4. V_{DD} decoupling capacitor.
5. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note

4. General Description

The MX109 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones, and Time Domain Scramblers. The encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be externally injected in the 8k to 64k bps range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal or ceramic resonator.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

5. Application

5.1 Control Data

Serial data is loaded into the MX109's serial shift register together with the serial clock. When a logic "0" is applied to the Load/Latch input the serial data is loaded into the parallel register. A logic "1" on the Load/Latch input latches the data into the parallel register to be used elsewhere in the chip. The data word format (see section 5.1.1) and bit settings (see section 5.1.2) are shown below. The timing diagram for loading the serial data is shown in Figure 4.

5.1.1 Data Word Format

AMP/ATTENUATION LEVEL							
D7	D6	D5	D4	D3	D2	D1	D0
VOL3	VOL2	VOL1	VOL0	ALG	FORCE IDLE	TEST 2	TEST 1

5.1.2 Bit Settings

GAIN	VOL3	VOL2	VOL1	VOL0
9dB	1	1	1	1
6dB	1	1	1	0
3dB	1	1	0	1
0dB	1	1	0	0
-3dB	1	0	1	1
-6dB	1	0	1	0
-9dB	1	0	0	1
-12dB	1	0	0	0
-15dB	0	1	1	1
-18dB	0	1	1	0
-21dB	0	1	0	1
-24dB	0	1	0	0
-27dB	0	0	1	1
-30dB	0	0	1	0
-33dB	0	0	0	1
MUTE	0	0	0	0

Table 1: Gain/Attenuation Selection

ALG	Algorithm Status
0	3-bit companding
1	4-bit companding

Table 2: Companding Algorithm Settings

FORCE IDLE	Encoder Output
1	1010101010 . . .
0	CVSD encoded signal

Table 3: Forced Idle Settings

 www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

Doc. # 20480121.005

TEST 1	TEST 2	MODE
0	0	Normal Operation
0	1	ENC IN to volume Control
1	0	ENC IN to decode BPF to volume control
1	1	ENC IN to Encode LPF to volume control

Table 4: Test Mode Settings

5.2 Serial Interface Timing

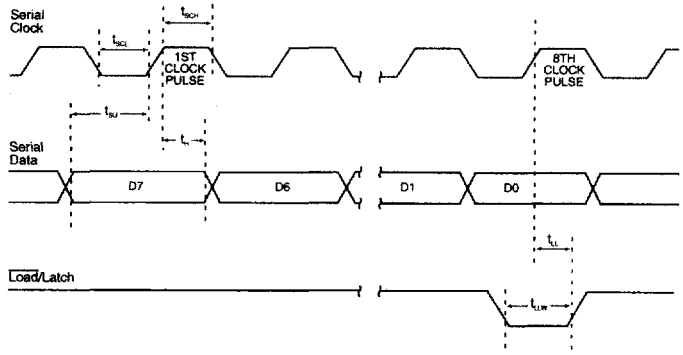


Figure 4: Serial Interface Timing Diagram

Abbreviation	Description	Time
t_{SCH}	Serial Clock high pulse width	50ns min.
t_{SU}	Data set-up time	30ns min.
t_{LL}	$\overline{\text{Load}}$ / Latch set - up time	50ns min.
t_{SCL}	Serial Clock low pulse width	50ns min.
t_H	Data hold time	40ns min.
t_{LLW}	$\overline{\text{Load}}$ / Latch pulse width	80ns min.

Table 5: Serial Interface Timing Specifications

 www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

5.3 CODEC

5.3.1 Timing Information

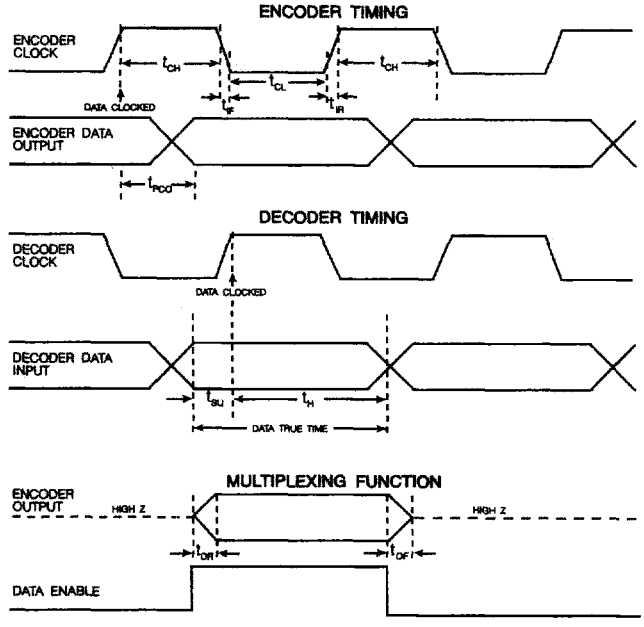


Figure 5: Encode/Decode Timing Diagram

Abbreviation	*Description*	*Time*			
		Min.	Typ.	Max.	Units
t_{CH}	Clock pulse width (logic 1)	1.0			µs.
t_{CL}	Clock pulse width (logic 0)	1.0			µs
t_{IR}	Clock rise time		100		ns
t_{IF}	Clock fall time		100		ns
t_{SU}	Data set-up time			450	ns
t_H	Data hold time	600			ns
$t_{SU} + t_H$	Data true time		1.5		µs
t_{PCO}	Clock to output delay time		750		ns
t_{DR}	Data rise time		100		ns
t_{DF}	Data fall time		100		ns
	Xtal input frequency		3.58		MHz

Table 6: Encode/Decode Timing Specifcations

5.3.2 CODEC Performance

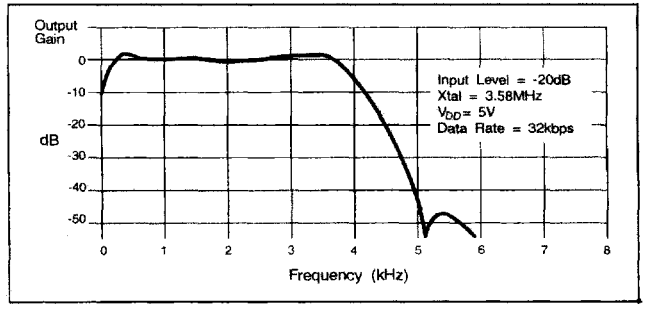


Figure 6: Typical CODEC Frequency Response

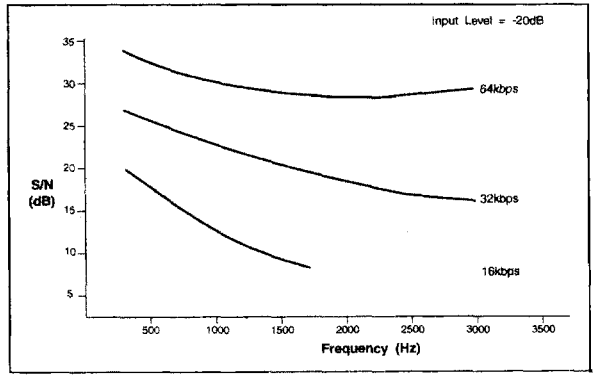


Figure 7: Typical S/N ratio with Input Frequency

 www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.
Correct operation of the device outside these limits is not implied.

General	Min.	Typ.	Max.	Units
Supply Voltage	-0.3		7.0	V
Input Voltage at any pin to V_{SS}	-0.3		(V_{DD} +0.3)	V
Current				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pins	-20		20	mA
P/DW Packages				
Total Allowable Power Dissipation at T_{AMB} = 25°C			800	mW max.
Derating above 25°C			10	mW/°C above 25°C
Operating Temperature	-30°		70°	°C
Storage Temperature	-40°		85°	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied

	Min.	Max.	Units
V_{DD}	2.7	5.5	V
Operating Temperature	-30	75	°C
Xtal/Clock f_0		3.58	MHz

www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

Doc. # 20480121.005

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.

V_{DD} = 5.0V, T_{AMB} = 25°C

Xtal/Clock f_0 = 3.58MHz, Audio Test Frequency = 820Hz

Sample Clock Rate = 32kbps, Audio level 0dB ref. (0dBmO) = 489mV_{RMS}

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current			5.0		mA
Logic Levels					
Input Logic "1"		70%V_{DD}			V
Input Logic "0"				30%V_{DD}	V
Output Logic "1"		80%V_{DD}			V
Output Logic "0"				20%V_{DD}	V
Digital Input Impedance					
Logic I/O Pins			10		MΩ
Logic Input Pins, Pullup Resistor	2	300			kΩ
Digital Output Impedance			4		kΩ
Analog Input Impedance			100		kΩ
Analog Output Impedance	5		200		Ω
Insertion Loss	1		0		dB
Dynamic Values V_{DD} = 5.0V					
Encoder:					
Analog Signal Input Levels	5	-30		6	dB
Principal Integrator Frequency			275		Hz
Encoder Filter Passband (3dB)				3800	Hz
Compand Time Constant			4		ms
Decoder:					
Analog Signal Output Levels	5	-33	0	9	dB
Decoder Filter Passband (3dB)	2	250		3800	Hz
Encoder/Decoder (Full Codec):					
Passband		300		3400	Hz
Stopband		6		10	kHz
Stopband Attenuation			60		dB
Passband Gain			0		dB
Passband Ripple		-3		3	dB
Output Noise (Input Short Circuit)	6		-54		dBp
Group Delay Distortion	3				
(1000Hz-2600Hz)				450	µs
(600Hz-2800Hz)				750	µs
(500Hz-3000Hz)				1.5	ms
Xtal/Clock Frequency		3.0	3.58	4.0	MHz

Operating Characteristics Notes:

1. All logic inputs except Encoder and Decoder Data Clocks.
2. With passband gain of ±1dB.
3. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
4. Relative Timings are shown in Figure 4.
5. Recommended values.
6. Psophometric weighted measurement.

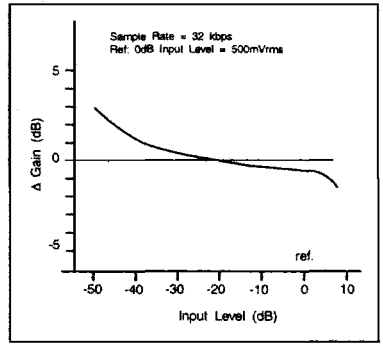


Figure 8: typical Variation of Gain with Input Level

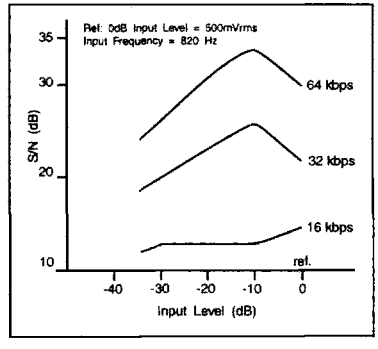
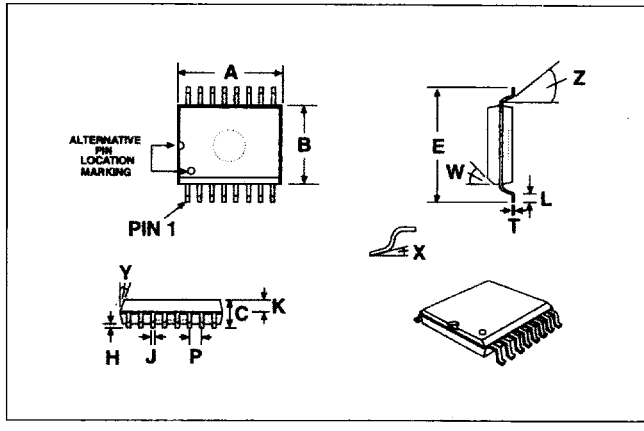


Figure 9: Typical Variation S/N ratio with Input Level

 www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

6.2 Packaging

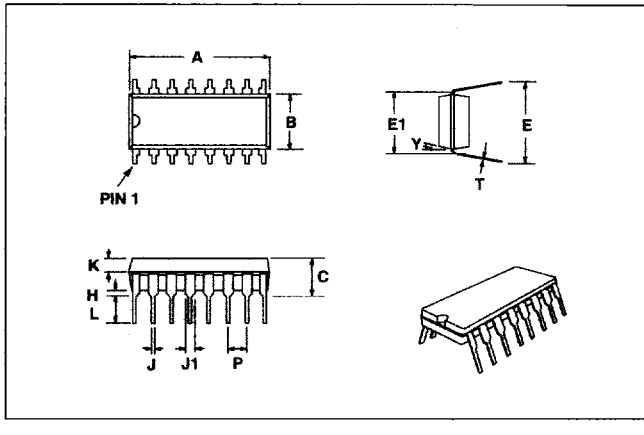


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 16-pin SOIC Mechanical Outline: order as part no. MX109DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91)
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 16-pin PDIP Mechanical Outline: order as part no. MX109P

 www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA