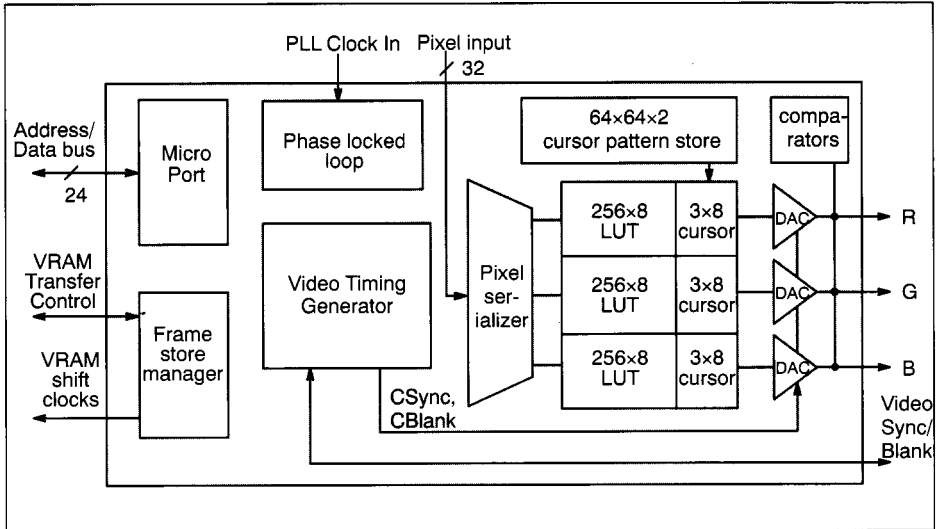


COLOR VIDEO CONTROLLER
PRELIMINARY INFORMATION

MAIN FEATURES

Video rates up to 135MHz
 Programmable pixel depth and multiplexing ratios
 1, 2, 4 and 8-bit pseudo color pixels
 15, 16 or 24-bit true color support
 Software configurable Video Timing Generator
 Comprehensive video RAM framestore manager
 On-chip phase-locked loop pixel clock generator
 64x64 pixel x3 color hardware cursor
 Triple 8-bit DACs
 Triple 256x8 anti-sparkle palette RAM
 Support for split SAM VRAMs
 Software and hardware compatible with IMS G332

BENEFITS

Reduced component count
 Reduced system power consumption
 Enhanced system flexibility
 Easy upgradeability
 All digital signals below RFI regulated frequency
 Reduced system design time

APPLICATIONS

High resolution graphics and imaging
 Broadcast/CC television systems
 X-terminals
 Low cost workstations
 High-resolution color add-in boards
 'Processor Direct' PC graphics systems

DESCRIPTION

The IMS G335 is a very high performance CMOS device, integrating a triple 8-bit palette-DAC with all the control functions required to produce high resolution color graphic displays. It offers a number of significant enhancements over the older IMS G332.

The IMS G335 supports multiple pseudo color and true color display formats, and offers enormous flexibility in system design and use.

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13.1 Introduction

The IMS G335 provides all the necessary functions to control real-time operation of a raster scan video display, using dual-ported video RAMs.

The device consists of a 32-bit variable format multiplexed pixel interface, a programmable video timing generator (VTG), a 256 location color lookup table (LUT) with variable addressing modes, triple 8-bit video Digital-to-Analogue Converters (video DACs), a $64 \times 64 \times 2$ bit cursor store and 3 location cursor LUT, a programmable cursor positioning/insertion controller, a video memory control system and phase-locked loop clock generator.

A brief description of each functional block is given in Sections 13.1.1 to 13.1.8; for more detailed information please refer to the relevant section in the datasheet.

Software and hardware compatibility with IMS G332

The IMS G335 has been designed to be software and hardware compatible with the IMS G332. Pins used for new signals on the IMS G335 were defined as **HoldToGround** on the IMS G332, so new devices can be drop-in replacements. A number of features have been added to the IMS G335 to further improve flexibility and simplify design compared to the IMS G332. **The IMS G335 is recommended for all new designs.**

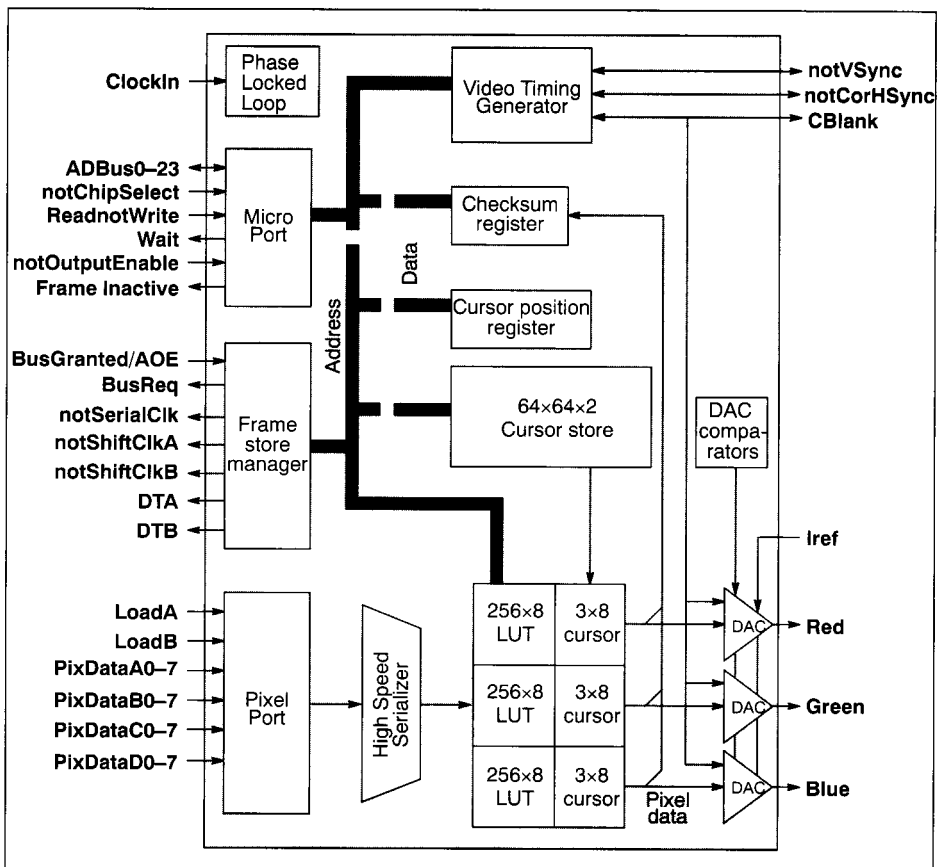


Figure 13.1 IMS G335 Block Diagram

13.1.1 Clocks

An on-chip phase-locked loop clock generator allows the IMS G335 to be driven from a low speed clock in the 5MHz to 10MHz range, which is internally multiplied by a user-specified factor to achieve video data rates. The controller can be clocked by a full rate system clock if desired, although at a reduced frequency compared to that achievable with the PLL.

13.1.2 Micro Port

The entire IMS G335 register space is read/write accessible via the micro port. This is a 24-bit wide synchronous interface, with multiplexed address and data, for memory-mapped access to all registers. The micro port interface is also used to provide the VRAM shift register transfer address.

To simplify the micro interface design all IMS G335 micro port control signal pulse widths are independent of the system clock frequency. Total read/write cycle times are system frequency dependent and a wait pin is provided to allow synchronization between the IMS G335 clock regime and that of the processor or interface bus.

13.1.3 Video timing generator

The video timing generator is a programmable finite state machine which uses a set of screen description parameters to produce the monitor sync and DAC blanking signals as well as the video RAM shift clock signals. It can be configured to be the system master or, as a slave, to lock onto an external signal which is already synchronous or has been previously genlocked. This may be from another SGS-THOMSON CVC, giving the potential for multiple, synchronous video systems. The timing generator runs at one quarter of the video dot rate and the screen description parameters therefore have a resolution of four pixel periods.

A new interlace mode has been added to the IMS G335, permitting displayed fields to have an even number of lines. Another new option allows line sync signals to be maintained during frame flyback, as required by newer multisync monitors.

13.1.4 Framestore manager

All the requirements of supporting a video RAM framestore are met by the IMS G335. The framestore manager uses framestore description parameters to control VRAM row transfers to maintain a constant supply of pixels to the pixel interface. Support is provided for both synchronous and asynchronous (split SAM) row transfers.

For synchronous reloads, the IMS G335 supplies the refresh address and the transfer strobes, synchronized to the VRAM SC signals, so that a packed pixel framestore can be implemented regardless of the variations in screen format and framestore architecture.

13.1.5 Pixel Port

High pixel rates are achieved by multiplexing the VRAM outputs into a 32 bit wide pixel port, the multiplex ratio being dependent on the bpp format selected. An interleaved memory system is supported with all necessary signals in order to give the maximum possible multiplexing ratio in each case. The IMS G335 supports 24, 16, 15, 8, 4, 2 and 1 bpp.

Pixel Sampling

The IMS G335 provides two pixel sampling modes; internal sampling, where the VRAM data is sampled by internally generated strobes and external sampling where the VRAM data is latched by externally supplied signals.

External sampling simplifies high speed system design and allows higher sampling speeds to be achieved through shorter VRAM data set-up and hold times. Internal sampling provides backwards compatibility with the IMS G332 pixel sampling method. In both modes the IMS G335 automatically adjusts the shift clock frequency, along with the multiplex ratio of the port, according to the bits per pixel mode selected. Further details are given in Section 13.8.

Pixel formats

The XGA graphics standard from IBM includes a 16-bit true color format, split 5,6,5 between the red, green and blue fields. This mode is supported by the IMS G335 and is targeted towards cost-sensitive multimedia applications. It is selectable through Control Register A, and replaces the 6,6,4 format supported by the IMS G332.

13.1.6 Hardware Cursor

The hardware cursor is a complete system. The cursor store and lookup table are memory mapped, its position being modified by a single register access which can occur at any time, becoming valid at the next frame scan. The cursor position is stored in 2's complement relative to the top left pixel on the screen and is independent of monitor specifications.

The IMS G335 includes pixel complement and XGA cursor pixel options. Pixel complement ensures that cursor pixels are always visible, whatever the background color, by displaying the complement of the background pixel color. The XGA option provides support for XGA standard cursor pixel mapping.

13.1.7 Anti-sparkle Color Palette

The serialized pixels are used as addresses into a triple 256x8 pipelined RAM. In pseudo color modes one address is applied to all three RAMs giving a maximum of 256 simultaneous colors out of a possible 16.4 million. In true color each RAM is independently addressed for gamma correction of up to 16.4 million simultaneous colors. The palette has an anti-sparkle mechanism which reduces the visible effect of palette updates during display.

13.1.8 Video DACs

The three 8-bit DACs drive RS-170 level signals directly into a 37.5Ω load. They are blanked with programmable setup, internally by the VTG, externally by the **CBlank** pin or by a combination of the two. Composite Sync may be added to all three DACs.

Each DAC output is attached to a comparator which can be used to detect if a termination load (e.g. monitor cable) is connected to the analogue output. Another option enables the red and blue DAC outputs to be compared against the green DAC to provide board level debugging without a monitor connected. The output state of the comparators may be read from Control Register B.

13.1.9 System Operation

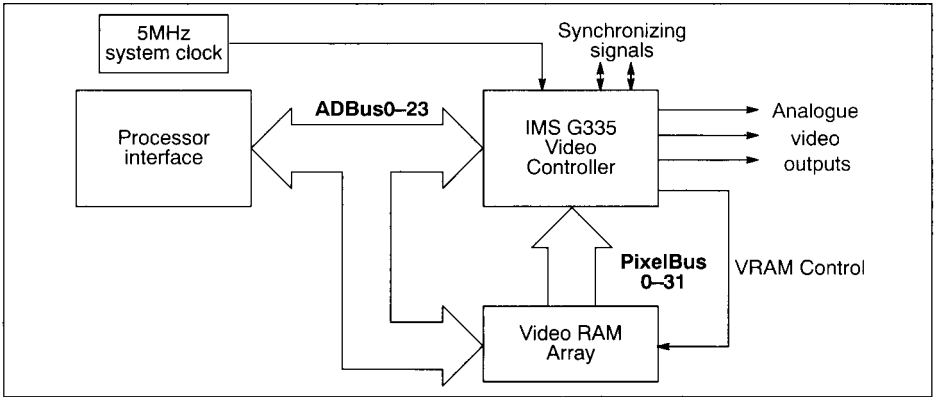


Figure 13.2 IMS G335 operating in a simple graphics system

Figure 13.2 shows how the IMS G335 would fit into a typical single-bitmap display system. The clock is typically sourced from a 5MHz crystal, with the video data being streamed to the screen at the full video rate of up to 135MHz. The video RAM array is directly accessed by the processor, with screen management automatically being performed by the IMS G335. All external digital signals and clocks are running at one quarter of the video rate, alleviating problems of high speed system design.

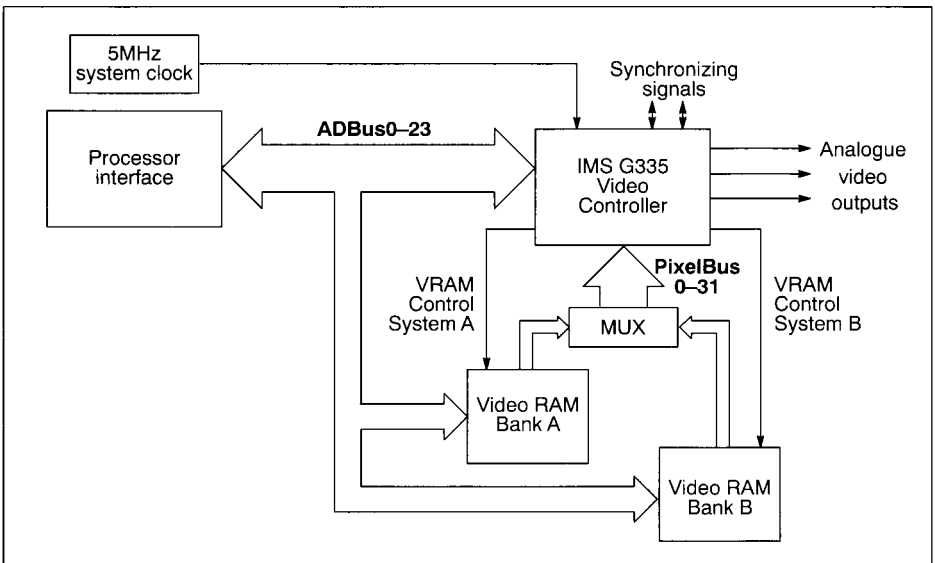


Figure 13.3 IMS G335 operating with an interleaved memory system

Figure 13.3 shows the organization of an interleaved framestore. The IMS G335 accepts alternate loads from each bank in turn through an external multiplexor (or if the video rate is low enough - about 85MHz - the VRAM serial output enables can be used instead of external hardware). The IMS G335 supplies all the controls required to implement this architecture.

13.2 Pin function reference guide

13.2.1 Micro port

Pin name	I/O	Page No.	Comments
ReadnotWrite notOutputEnable notChipSelect Wait	I I I O	173	Microport control signals. Wait is used to extend cycle times if necessary.
ADBus0-23	I/O	173	Multiplexed address and data bus. All 24 bits are used for data; addresses are supplied either on ADBus2-11 or on ADBus3-12 depending on the word width. The port is also used to drive out the 22-bit VRAM transfer address.
FramelInactive	O	195	Timing signal which is active high during vertical blanking.
BusReq BusGranted/AOE	O I	187	DMA control signals used in conjunction with DTA and DTB when refreshing the VRAM shift registers.

13.2.2 Pixel port

Pin name	I/O	Page No.	Comments
notSerialClk	O	192	notSerialClk runs continuously at one quarter the video frequency. This signal must be buffered
notShiftClkA notShiftClkB	O O	192	VRAM clocks running under the control of the timing generator. The clocks run in anti-phase in interleaved mode; only notShiftClkA runs in non-interleaved mode. These clocks must be buffered with an inverting buffer.
DTA DTB	O O	187	VRAM shift register transfer strobes. DTA and DTB are synchronized to notShiftClkA and notShiftClkB respectively. In split SAM mode DTA and DTB are not used (although still active).
LoadA	I	200	Pixel data sampling strobe; non-interleaved and interleaved modes.
LoadB	I	200	Pixel data sampling strobe; interleaved mode only.
CBlank	I/O	174	CBlank is a composite blanking pin. Direction is soft selectable.
PixDataA0-7 PixDataB0-7 PixDataC0-7 PixDataD0-7	I I I I	197	Pixel input ports A-D. Port A is least significant; port D is most significant. In internal latching mode pixel data is latched synchronous to notShiftClkA or notShiftClkB . In external latching mode pixel data is latched on the rising edge of LoadA or LoadB .

13.2.3 Miscellaneous

Pin name	I/O	Page No.	Comments
Reset	I	184	Must be held active high with clocks running for 6 periods of ClkIn in order to reset the IMS G335
HoldtoGround	–	–	These pins must be connected directly to ground, but do not supply ground to the chip.

13.2.4 Phase locked loop

Pin name	I/O	Page No.	Comments
CapPlus CapMinus	N/A	172	Phase locked loop decoupling pins, also used to hard select external dot rate clock source by connecting CapPlus to CapMinus .
ClockIn	I	172	Clock input for both PLL and times-one operation.

13.2.5 Video signals

Pin name	I/O	Page No.	Comments
Red Green Blue	O O O	204, 211	Blanked video current outputs. Drive into doubly terminated 75Ω load.
Iref	I	211	Video DAC reference current.
notVSync notCorHSync	I/O I/O	176	Digital soft configurable sync signals for system synchronization. They are inputs in slave mode and outputs in master mode.

13.2.6 Supplies

Pin name	I/O	Page No.	Comments
AVDD AGND	N/A N/A	229	AVDD/AGND supplies analogue portions of chip.
VDD GND	N/A N/A	229	VDD/GND supplies digital portions of chip.

13.3 Register function reference guide

Register	Word address (hex)	Page No.	Description
Boot Location	#X000	215	Startup location to which must be written the clock multiplication factor, whether PLL or $\times 1$ mode, and the 32/64-bit address alignment selection.
Screen Description Registers	#X021 to #X02B	212	Read/write registers containing the screen description parameters. These are accessible only when the timing generator is not running.
Top of Screen #1	#X02C	210	Read/write register giving ability to reprogram the top of screen pointer while the VTG is disabled.
Framestore description Registers	#X02D, #X02E		Read/write registers containing effective VRAM register length and DMA latency figures.
Mask Register	#X040	210	8-bit pixel address mask register. Read/write accessible at all times. (Operates only on pseudo color pixels)
Control Register A Control Register B	#X060 #X070	213	Read/write control registers contain configuration information. Unassigned bits must be written with zero and are not valid on read. Read/write accessible at all times.
Top of Screen #2 ¹	#X080		Read/write register giving ability to reprogram the top of screen pointer while the VTG is enabled.
Cursor palette	#X0A1 to #X0A3	206	3 \times 24 bit cursor color registers. Read/write accessible at all times.
Checksum registers	#X0C0 to #X0C2	210	RGB frame checksums.
Cursor position	#X0C7	208	24-bit register storing the x-y position of the cursor.
Color Palette	#X100 to #X1FF	209	256 locations of 24-bit colors read/write accessible at all times.
Cursor store	#X200 to #X3FF	206	512 locations of 16-bit words, each containing 8 packed 2-bit pixel color values.
N.B. All other addresses in the range are reserved and must not be written to.			
1 Both Top of Screen locations address the same physical hardware			

Micro port address alignment

The 10-bit addresses given in the table above are word addresses. They are user selectable to align with the address conventions used in 64-bit or 32-bit words. In 32-bit mode, addresses must be supplied on **ADBus2-11**; in 64-bit mode they must be supplied on **ADBus3-12**. The unused address bits **ADBus0-1** (in 32-bit mode) or **ADBus0-2** (in 64 bit mode) are ignored by the IMS G335.

32/64-bit address alignment is selected by programming the appropriate bit of the Boot Location; details are given on page 215.

13.4 Clocks

The IMS G335 has two alternate clocking schemes. The primary clocking system uses a phase locked loop (PLL) on the chip to multiply up the low frequency (<10MHz) input clock to the required video data rate. Alternatively a full dot-rate clock may be supplied (Times 1 mode).

13.4.1 PLL mode

In PLL mode, a 1 μ F capacitor must be connected between **CapPlus** and **CapMinus**. A ceramic capacitor is preferred, with an impedance of less than 3 Ω between 100kHz and 10MHz. If a polarized capacitor is used, the negative terminal must be connected to **CapMinus**. Total PCB track length should be less than 50mm.

13.4.2 Programming the clock frequency

The multiplication factor is stored in bits 4 - 0 of the boot location #X000 and is programmable only after a reset. Whenever the multiplication factor is changed, the PLL will pull into the new frequency within 20 μ s. The second access to the IMS G335 must be held off for this time as described in Section 13.6.5.

Input clock frequencies between 5MHz and 10MHz are recommended for stable operation; multiplication factors from 5 to 31 are permitted, giving a minimum recommended operating frequency of 25MHz and a maximum frequency set by the speed rating of the device.

The input frequencies may vary continuously between the recommended limits. Frequencies outside this range, and multiplication factors of less than 5 (down to 1) will work but special precautions will be needed to ensure power supply noise rejection. The maximum multiplication factor of 31 is a hard limit.

ClockIn must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. ClockIn must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits.

13.4.3 'Times 1' mode

The external dot rate clock can be selected in one of two ways. Either the terminals **CapPlus** and **CapMinus** should be shorted together, or a '0' should be written to the clock source select bit in the boot location. The Times 1 mode timing is shown in Figure 13.47 and parameters in Table 13.39.

It is permissible to short **CapPlus** and **CapMinus** via a FET or relay.

Note that Times 1 clocking does not allow operation up to the maximum speed rating of the device but it does extend the operating frequency down below 25MHz. The minimum operating frequency in Times 1 mode is 5MHz.

13.5 The micro port

13.5.1 Introduction

The micro port is a bidirectional 24-bit interface, consisting of a multiplexed address and data bus and several control signals. It is used for programming the VTG screen description registers, color and cursor look-up tables, cursor store, and other registers.

13.5.2 Word alignment

The IMS G335 is designed for use with 32 and 64-bit processors, and therefore supports both 32 and 64-bit word alignment conventions. With 32-bit alignment selected, the least significant address bit is on **ADBus2**; with 64-bit alignment selected it is on **ADBus3**. This applies only on host processor accesses to the micro port, in which a 10-bit address is input to the device and not on DMA transfer cycles in which a 22-bit word address, **ADBus2–23** is generated by the IMS G335 framestore manager.

Word alignment is selected through the setting of bit 6 of the boot location, see Table 13.24, page 215.

13.5.3 Micro port read/write cycles

To simplify system design and reduce the period that bus access is denied to other devices, micro port control signal timings are not dependent on the pixel frequency. Cycle times remain pixel-rate dependent but all other parameters are specified in absolute times as defined in Tables 13.26 and 13.27.

Four signals control the flow of address and data in and out of the device on **ADBus0-23**:

Signal	I/O	Function
notChipSelect	I	The falling edge latches the address and begins the access.
ReadnotWrite	I	This signal is sampled within 1SClk of the falling edge of notChip select . A low indicates a write cycle; if a valid low pulse has occurred within the sampling window, this indicates a write. The rising edge latches data in on a write. A write cycle can be extended indefinitely by holding this signal low.
notOutputEnable	I	This signal turns on the output buffers during a read cycle; it must be pulsed in order to terminate the access. Read cycles can be extended indefinitely by either holding off the pulse or holding the signal low.
Wait	O	This signal is driven high shortly after notChipselect goes low. It returns to low on a read when valid data is ready or, on a write when the cycle has finished and another access can begin.

Table 13.1 Micro port control signals

13.5.4 Boot write cycles

These accesses are asynchronous and do not depend on the clock speed in any way. Boot writes are available only as the first cycle after a reset and a boot write must be made after every reset. See Table 13.30, page 220 for the timings applicable to boot write cycles.

The boot location may be read through a normal micro port read cycle.

13.6 Video Timing Generator

13.6.1 Introduction

The Video Timing Generator is a programmable finite state machine which provides monitor timing strobes and Composite blanking information to both the analogue and digital outputs. It also provides display format information to the cursor controller and framestore manager.

All of the timing parameters are independently variable with a horizontal resolution of 4 pixels and a vertical resolution of $\frac{1}{2}$ lincetime. This allows for control of a wide range of monitors, including NTSC and PAL/SECAM standard systems.

The VTG can be configured to operate as a slave in both non-interlaced and interlaced modes, synchronizing to a master signal which is either already synchronous or has been previously genlocked.

13.6.2 The display screen

In a raster scan display system the displayed picture is built up of a number of display lines, each consisting of a visible display period and a line flyback period during which the synchronization pulse occurs. The line flyback period is split into three segments, shown in Figure 13.4, known as Front Porch, Back Porch and Line Sync. Standard monitors synchronize to the leading edge of the line sync pulse.

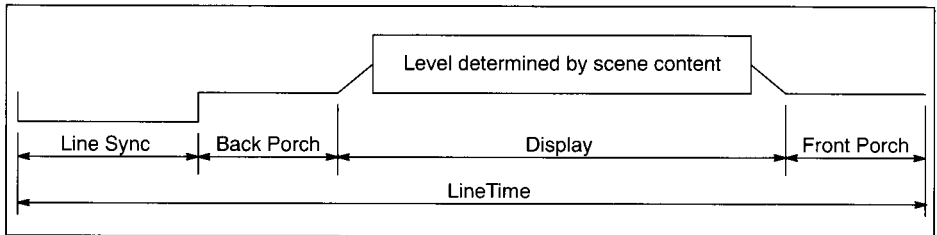


Figure 13.4 Scan line segments

The timing of each of the constituent periods of a line are specified in multiples of four pixels called 'Screen Units' (SU) which are used to specify the line parameters programmed into the screen description registers. In 24 bpp modes, the effective multiplex ratio falls below 4:1 so that on-chip acceleration is not possible. This means that the screen unit definition in these modes varies from the general case.

In 24bpp non-interleaved mode: 1 SU = 1 pixel

In 24bpp interleaved mode: 1 SU = 2 pixels

When programming the screen description registers for these pixel modes, the new SU value must be substituted.

A display picture consists of bursts of display lines (which can number from a few hundred to over a thousand) separated by a number of frame flyback lines. These flyback lines do not carry display information but contain certain sync timings which depend on the waveform standard being obeyed. These timings are also programmed into the screen description registers but, because of their longer duration, are specified in units of half a LineTime. An example of a video output showing frame flyback lines and a few display lines is given at the top of Figure 13.5.

A complete frame comprises a number of discrete time periods, the vertical elements of which, as shown in Figure 13.5, are VPreEqualize, VSync, VPostEqualize, VBlank and VDisplay. The period VSync is the vertical synchronization pulse width. The periods before and after VSync are known as equalization periods (VPreEqualize and VPostEqualize). After VPostEqualize is a period of blanked scan lines, VBlank. The total vertical blanking period is the sum of these four and the position of VSync within it can be adjusted by varying the equalization periods. The display period, Vdisplay, comprises all the displayed lines of the frame.

All of these periods are programmed in multiples of half a lincetime and in a non-interlaced system are in fact even multiples, i.e. a whole number of lines (the interlaced case is dealt with on page 181). After the final displayed line the frame scan cycle returns to VPreEqualize and VSync.

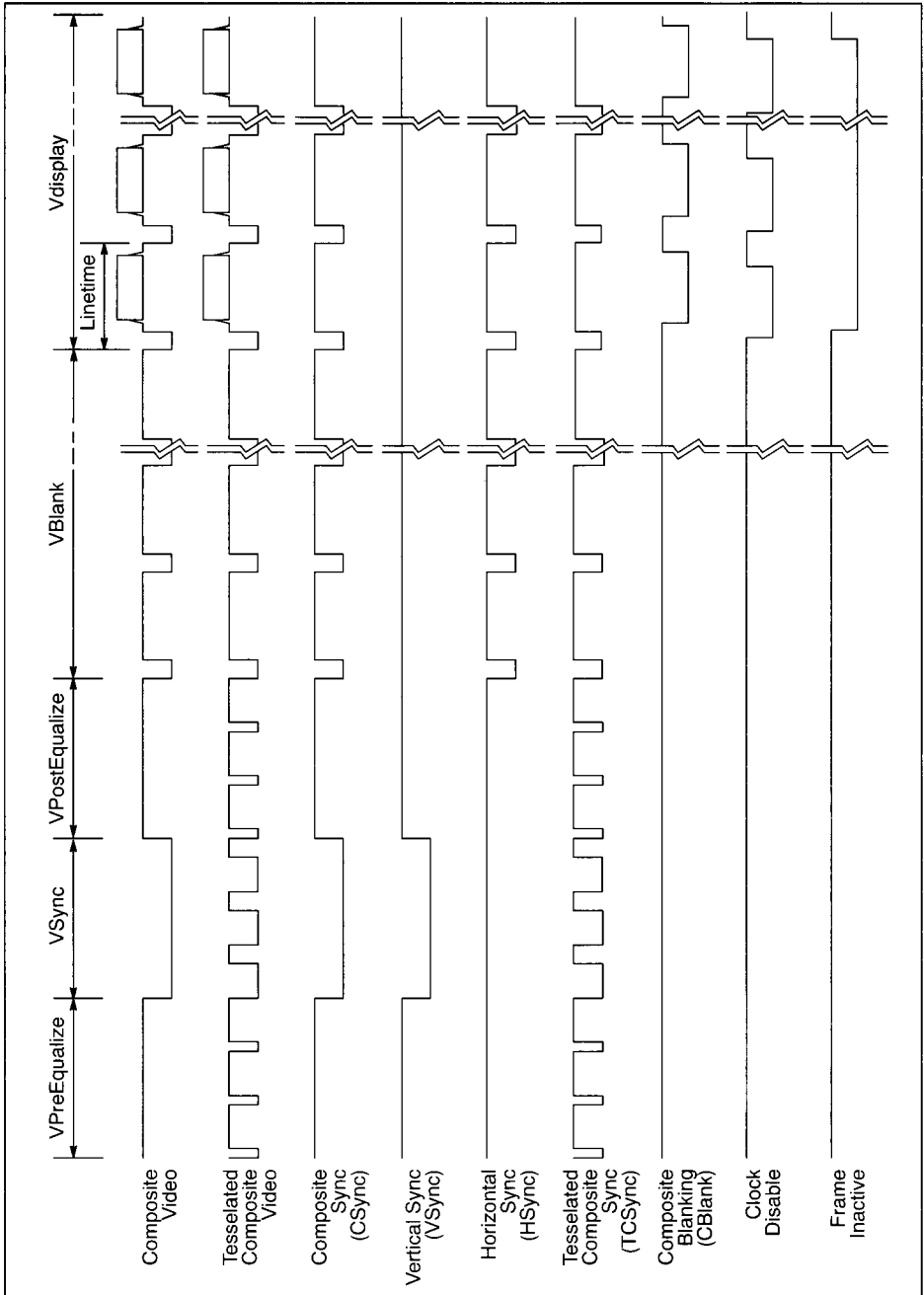


Figure 13.5 Waveforms produced by the Video Timing Generator

13.6.3 Sync waveforms produced by the IMS G335

The IMS G335 produces a number of different sync patterns which are required for different output waveform standards. Nine different waveforms are produced simultaneously which can be directed to different destinations under the control of the Control Register A (Word Address = #X060).

These waveforms are shown in Figure 13.5. Composite Sync comprises the horizontal and vertical sync pulses. Composite Video comprises both horizontal and vertical sync pulses and video information. Tesselated Composite Sync (TCSync) includes tesselated cycles during Pre and Post Equalize and VSync. Composite Blanking is a blanking signal for both horizontal and vertical blanking.

The actions of Control Register A control four basic decisions:

- Whether the video DAC output is video only or video + sync
- Whether the composite sync mixed onto the DAC outputs is tesselated or plain (mux1)
- Whether the **notCorHSync** pin carries tesselated composite, composite or horizontal sync (mux2)
- Whether **CBlank** pin carries composite blank or ClockDisable (mux3)

This is shown diagrammatically in Figure 13.6, which also includes some more detailed information about the timing of the data. The effect of Control Register A is shown in Table 13.2.

Signal Pin	Control Register A Bits	TCSync	HSync	CSync	CBlank	ClkDisable									
							Video only	Composite video	Tesselated composite video	CBlank	No blanking	Force blanking			
notCorHSync	4	0	X	1											
	5	0	1	0											
CBlank	9				0	1									
Red Green Blue	4						X	1	0						
	6						1	0	0						
	10 11									0 0	0 1	1 X			
Digital							Analogue								

Table 13.2 Control signal routing options

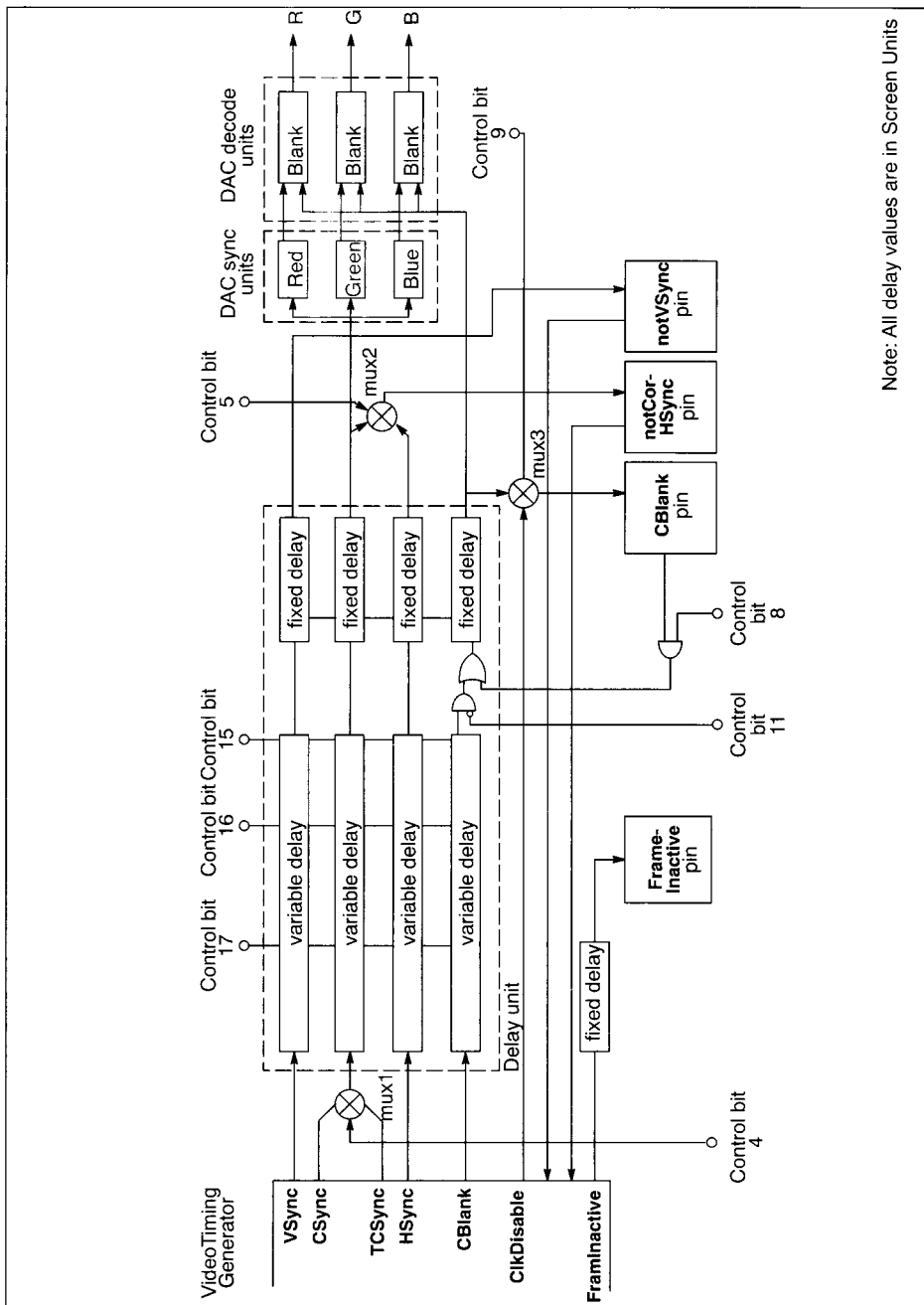
CBlank as input

The function of this pin is controlled by Control Register A, bit 11. When this bit is high, CBlank from the Video Timing Generator is disabled so that the only blanking signal to the DACs is from the **CBlank** pin (as input). When bit 11 is low, CBlank from the Video Timing Generator is ORed with any blanking signal from the **CBlank** pin before being supplied to the DACs.

Internal sync and blank delays

Extra delays can be added to the internal sync and blank delays, in increments of 1 SClk to a maximum of 7SClk periods, by setting bits 15–17 of Control Register A. In external sampling mode, these delays can be compensated for by delaying the **LoadA** and **LoadB** signals by a matching amount. The feature is not available in internal sampling mode (see Section 13.8.5).





Note: All delay values are in Screen Units

Figure 13.6 Digital and analogue sync-ing and blanking system

Horizontal sync during frame flyback

To provide support for certain multisync monitors the IMS G335 supports an additional mode where HSync continues to run during frame flyback (in plain sync mode). Also, if Composite sync is selected, the **notCorHSync** pin will carry the CSync waveform illustrated in Figure 13.7 with the alignment as shown between CSync and HSync. This mode is selected by setting bit 2 of Control Register B (see Table 13.23).

A number of conditions of use are given in the sections headed 'Frame timing parameter calculation', page 184.

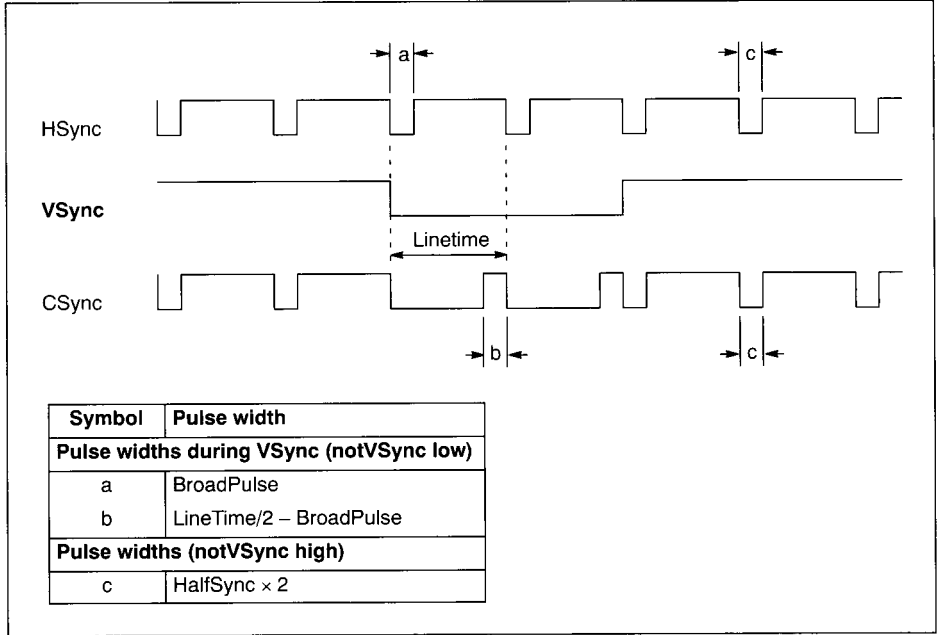


Figure 13.7 Flyback sync pattern

13.6.4 Programming the screen description registers

The screen description registers are memory mapped as shown in Table 13.3, page 182. They contain the line timing parameters, which are programmed in Screen Units (also referred to as one 'SClk') and also the frame timing parameters, which are programmed in units of half a linetime.

These registers can only be written to while the Video Timing Generator is turned off (this is controlled by writing to Control Register A (Address #X060)).

Line timing parameters during blanked and displayed lines

The constituent periods of a display line, introduced in Section 13.6.2, map directly to timing generator registers with two exceptions. Firstly, the line synchronizing pulse is split into two periods of equal duration which are used in immediate succession - the parameter used for this is 'HalfSync'. Secondly, there is no register for FrontPorch, rather the total line time is programmed into a separate register and the end of the scan line occurs when LineTime expires.

All line timing parameters are specified in Screen Units, so that for example, except for 24 bpp mode, a 1024 pixel screen width is described as 256 SU. The line description parameters are illustrated in Figure 13.8.

Figure 13.8 (a) shows the parameters relating to a full scan line. The duration of FrontPorch is not directly defined but is determined by LineTime minus the duration of the other scan line components. HalfSync is used twice in succession to construct the line sync pulse.

Figure 13.8 (b) shows the parameters relating to a short scan line (occurring only in interlaced displays). The overall duration is determined by LineTime. As for a full scan line the duration of the FrontPorch is not directly defined, hence it can differ from the implied FrontPorch value of a full scan line.

Line timing parameters during frame flyback

During frame flyback, the VTG uses two variants of the basic linescan sequence. In VPreEqualize and VPostEqualize the waveform produced is either constant high or tessellated as shown in Figure 13.8 (c). The internal cycle, however, uses the parameter sequence as shown in Figure 13.8 (b) so the parameter ShortDisplay must contain a valid value even though interlace is not being used.

In VSync, the waveform produced is either constant low or tessellated as shown in Figure 13.8 (d). The internal cycle uses both BroadPulse and LineTime, so the parameter BroadPulse must contain a valid value, even if flyback tessellations or composite syncs during flyback are not being used.

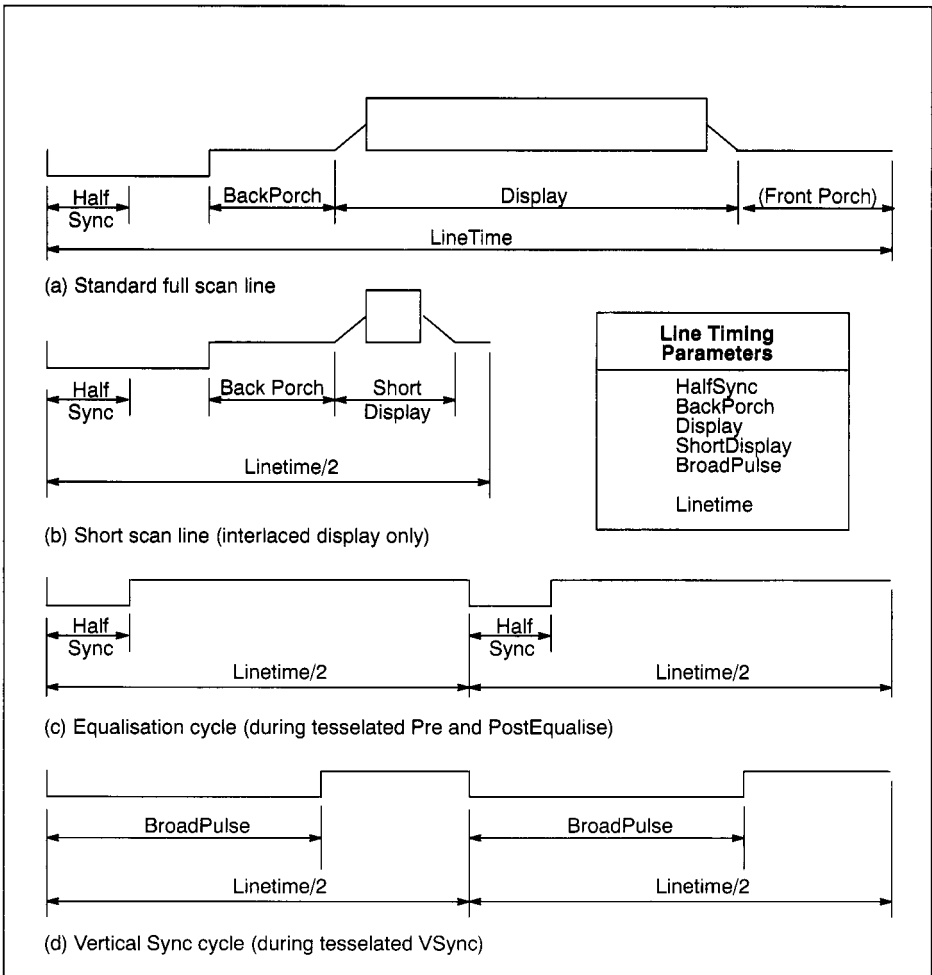


Figure 13.8 Line timing parameters

Frame timing parameters

The IMS G335 generates synchronizing signal timings and levels conforming to both broadcast and closed circuit television standards. This means that, as well as being capable of generating frame sync patterns associated with non-interlaced computer graphics systems, it is also able to produce tessellated sync signals for an interlaced television system (see Figure 13.9).

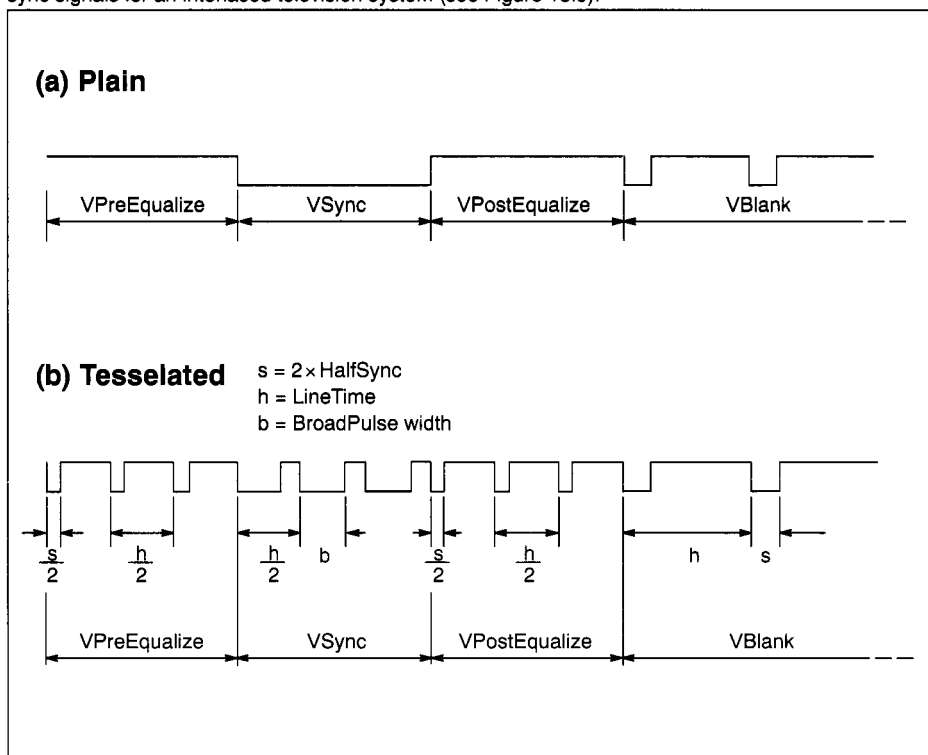


Figure 13.9 Composite Sync frame flyback waveforms

In non-interlaced mode the VBlank and VDisplay parameters must be an even number of $1/2$ lines. The remaining parameters may be odd or even, depending on the monitor specification.

There are two interlace modes:

- TV standard interlace (each field must contain an odd number of lines)
- Even field interlace (each field must contain an even number of lines)

In both these modes bit 1 of Control Register A must be set; bit 14 of Control Register B is used to select either TV standard interlace (set to '0') or Even field interlace (set to '1'). Bit 2 of Control Register A selects the interlace standard required; this bit must be set to 1 for Even field interlace operation.

In TV standard interlace mode, VDisplay must be odd and VBlank may be even or odd, depending on the standard being followed. Note that in both interlace modes the VDisplay parameter describes the number of visible lines in each field, not the number in each frame, so that for example, an n-line interlaced frame, the VDisplay parameter is $n/2$ -LineTime periods.

In Even field interlace mode VBlank and VDisplay must remain even. In this mode the even field (lines 0,2,4...) is displayed first, followed by the odd field (lines 1,3,5...).

In non-interlace there is only one field, so that a 1024-line frame would have 2048 $1/2$ -LineTime periods.

Parameter	Notes	Units	Address
Line timing parameters			
LineTime	Determines the total line time (the sum of the displayed and blanked periods of a single line). For interlaced displays LineTime/2 also determines the duration of short (half) scan lines (see Figure 13.8). LineTime > (2×HalfSync + BackPorch + Display) LineTime must be an even multiple of the period of notSerialClk*	SU	#X02B
HalfSync	Determines the line sync pulse duration (2×HalfSync). HalfSync also determines the low period in pre and post equalize cycles of a tessellated frame flyback waveform.	SU	#X021
BackPorch	Determines the duration of BackPorch (shown in Figure 13.8). Note that BackPorch must exceed TransferDelay by at least two notSerialClk* periods. If BackPorch is less than 16 SCIk periods then the cursor will be offset as described in Section 13.9.5.	SU	#X022
Display	Determines the duration of the visible portion of the scan line. Display must be a multiple of the period of notShiftClk in SUs.	SU	#X023
FrontPorch	The duration of FrontPorch (shown in Figure 13.8) is implied by the following parameters: FrontPorch = LineTime – (Display + BackPorch + (2×HalfSync))		
ShortDisplay	Determines the duration of the visible portion of short (half) scan lines. ShortDisplay < LineTime/2 – (2×HalfSync + BackPorch) Transfer delay must not exceed ShortDisplay. (The parameter TransferDelay is described in Section 13.7).	SU	#X024
Frame timing parameters			
VDisplay	Describes the vertical display field (visible lines). For a non-interlaced display VDisplay = 2×(Lines per frame). For an interlaced display VDisplay = Half lines per field The total number of displayed lines in each frame must be a whole number.	Half lines	#X02A
VBlank	Determines the number of blanked lines during frame flyback. The total frame blanking period is the sum of VBlank, VSync, VPreEqualize and VPostEqualize.	Half lines	#X029
VSynC	Determines the duration of the frame sync pulse and, for a tessellated frame flyback waveform, the number of VSync cycles.	Half lines	#X026
VPreEqualize	Determines the duration of PreEqualize and, for a tessellated frame flyback waveform, the number of PreEqualize cycles.	Half lines	#X027
VPostEqualize	Determines the duration of PostEqualize and, for a tessellated frame flyback waveform, the number of PostEqualize cycles.	Half lines	#X028
BroadPulse	Determines: a. The low period in a VSync cycle of a tessellated frame flyback waveform. b. The pulse widths as shown in Section 13.6.3, Figure 13.7 when sync during flyback has been selected.	SU	#X025
* Note: 1 SU (Screen Unit) = 1 notSerialClk (SCIk) period = 4 pixel periods (except for 24 bpp non-interleaved mode where 1 SU = 1 pixel period and 24 bpp interleaved mode where 1 SU = 2 pixel period)			

Table 13.3 Summary of screen description parameters

Line timing parameter calculation

The line timing parameters can be calculated using the equations given in Table 13.4. Note that if the monitor waveforms are specified in microseconds, they must first be converted to Screen Units by dividing by the period of **notSerialClk**.

During a full line cycle (VBlank, VDisplay)	
HalfSync	= Horizontal Sync/2
BackPorch	= BackPorch
Display	= Display
LineTime	> (2×HalfSync + BackPorch + Display)
During an equalization cycle	
ShortDisplay	< LineTime/2 – (2×HalfSync + BackPorch)
Low period	= HalfSync
High period	= LineTime/2 – HalfSync
During a VSync cycle	
BroadPulse	= LineTime/2 – Pulse width*
Low Period	= BroadPulse
High period	= Pulse width
* Note: Pulse width = duration of serration pulse high time	

Table 13.4 Screen description line parameter equations

The following restrictions on parameter values **must** be observed:

General restrictions
All parameters must be greater than 1. LineTime must be an even multiple of the period of notSerialClk . $2 \times \text{HalfSync} + \text{BackPorch} + \text{Display} > \text{LineTime}/2 > 2 \times \text{HalfSync} + \text{BackPorch}$. The total number of displayed lines in each frame must be a whole number. $\text{TransferDelay} < \text{BackPorch} - 2$ $\text{ShortDisplay} < \text{LineTime}/2 - (2 \times \text{HalfSync} + \text{BackPorch}) - 1$ Display must be a multiple of the period of notShiftClk in SUs. TransferDelay must not exceed ShortDisplay (the parameter TransferDelay is described in Section 13.7).
Additional restrictions in Interlace mode
$\text{BackPorch} + \text{Display} > \text{bit}15 + (2 \times \text{bit}16) + (4 \times \text{bit}17) + 3^{1/2} \text{SClk} + 1 \text{notSerialClk}^*$ $(\text{LineTime}/2 - \text{FrontPorch}) > \text{TransferDelay} + 2$ $\text{TransferDelay} < \text{Display} - 2$ $\text{LineTime}/2 - \text{FrontPorch} > 1$ When the cursor is being used, FrontPorch must be > 4
Additional restrictions in split SAM mode
$(2 \times \text{HalfSync}) + \text{TransferDelay} < \text{LineTime}/2$
* Note: Refers to Control Register A bits 15 to 17 (pixel pipeline delay)

Table 13.5 Restrictions applying to parameter values

Note that a fully worked example for the Hitachi HM4219/4119 monitor is described in Section 17.3, page 341.

Frame timing parameter calculation (non-interlaced)

If the monitor waveforms are specified in milliseconds, then they must be converted to $1/2$ LineTime units as follows:

$$\text{Total number of lines per frame} = \frac{\text{frame period (ms)}}{\text{line period (\mu s)}}$$

Number of flyback lines = Total number of lines – number of displayed lines

The VTG programming rules are:

Number of flyback lines $\times 2$ = VPreEqualize + VSync + VPostEqualize + VBlank
and
VBlank must be even.

Once VSync has been expressed in terms of $1/2$ LineTimes then specification of the remaining parameters is determined by the monitor requirement for the location of VSync in the blanking period. A fully worked example for a non-interlaced monitor is given in Section 17.3, page 341.

If horizontal sync during flyback is selected, the following condition must be satisfied:

- VBlank, VSync, VPreEqualize and VPostEqualize must be even.

Frame timing parameter calculation (interlaced)

The interlaced timings generated by the IMS G335 are highly programmable but are specified to conform to the two major broadcast standards. For this reason there are different restrictions on parameter values. These restrictions are:

- 1 In NTSC (EIA) mode, VBlank must be even
- 2 In PAL/SECAM (CCIR) mode, VBlank must be odd
- 3 In both modes, VDisplay must be odd
- 4 In even field interlace mode, VDisplay and VBlank must be even

In all other respects, parameter calculation is identical to the non-interlace mode. A full table of parameters conforming to NTSC and PAL waveforms is given in Section 17.2, page 337. See Section 13.6.3 for further parameter restrictions if sync during frame flyback is selected.

If horizontal sync during flyback is selected, the following conditions must be satisfied:

- If EIA format has been selected the sum of (VSync + VPreEqualize + VPostEqualize) must be even.
- If CCIR format has been selected the sum of (VSync + VPreEqualize + VPostEqualize) must be odd.
- If Even field interlace format has been selected, VBlank and the sum of (VSync + VPreEqualize + VPostEqualize) must be even.

13.6.5 The VTG startup sequence

Reading from and writing to the VTG registers, which are memory mapped, is only possible while the timing generator is disabled. Enabling and disabling the VTG is achieved by a write to Control Register A (Address = #X060).

On startup, after reset, the host processor must write a configuration pattern to the IMS G335 bootstrap location. The effect of this is to set the PLL multiplication factor, clock source (PLL or external crystal) and microport address alignment.

Startup sequence:

- 1 Assert, then deassert **Reset**.
-Wait 50ns
- 2 Write configuration pattern to bootstrap location.
-Wait 80 μ s to allow PLL to stabilize

Control Register A will contain a default value of #X0000 and Control Register B will contain a default value of #X0200 (Sync pins tristate).

After this the screen parameters, color table, cursor pattern, etc. can be written to the appropriate locations in any order. The processor must then write to Control Register B, followed by Control Register A to enable and start up the VTG. If the rising edge of **ReadnotWrite** occurs after the falling edge of **Wait**, then there will be a fixed delay from the rising edge of **ReadnotWrite** to the falling edge of **notVSync**. If the rising edge of **ReadnotWrite** occurs before the falling edge of **Wait** then the delay will be fixed relative to the falling edge of **Wait**. These delays are detailed in Figure 13.40, page 223. The IMS G335 can be reprogrammed without asserting **Reset**.

The reprogramming sequence has three steps:

- 1 Write zero to bit 0 of Control Register A, disabling VTG.
- 2 Write to the screen parameter registers chosen for redefinition.
- 3 Write one to bit 0 of Control Register A, (redefining modes if necessary by modifying the relevant register bits) and enabling the VTG.

If only the operating mode is to be changed, step 2 only may be omitted, the remainder of the address space is programmed without disabling the VTG. If the clock multiplication factor is to be changed the full startup procedure must be followed, including reset.

13.6.6 Master and slave modes

Master mode configuration

The IMS G335 is set to operate as a master by setting the *Device Operating Mode* bit (Control Register A bit 3) low. This sets the composite and horizontal sync (**notCorHSync**) and vertical sync (**notVSync**) pins to be outputs. Sync is generated internally, and these two sync pins are driven appropriately, at TTL levels, active low or active high, depending on the setting of Control Register B.

Slave mode configuration

The IMS G335 is set to operate as a slave by setting the *Device Operating Mode* bit (Control Register A bit 3) high. This sets the composite and horizontal sync (**notCorHSync**) and vertical sync (**notVSync**) pins to be inputs. To enable and disable the IMS G335 VTG when configured for slave mode, it is necessary to write the *Device Operating Mode* bit at the same time as writing the VTG enable bit. These two control bits should be written in the same data write regardless of whether they are being written high or low.

Slave mode operation

With non-interlaced slave mode operation, an external horizontal sync is not required, but an external vertical sync must be supplied, as the IMS G335 synchronizes to each frame. The external vertical sync must be supplied to the **notVSync** input, and cannot be supplied to the **notCorHSync** pin.

The IMS G335 has internal synchronizers which eliminate any instability problems. However, unless the system ensures that the sync signals are locked in some way, either by running from a single master clock or by genlocking, then the picture will lock only to the nearest Screen Unit.

For a lock to pixel resolution, the systems must be synchronized and the external **notVSync** signal must be presented with the set up and hold times shown in Figure 13.45.

When using interlaced slave mode operation, external horizontal *and* vertical sync signals must be supplied to the **notCorHSync** and **notVSync** pins respectively. The *Digital Sync Format* mode must be selected to be separate sync, by setting Control Register A bit 5 high (logic 1). The IMS G335 will initially use the horizontal sync to determine which field is to be displayed, and subsequently synchronize on each field (not frame) using vertical sync.

Slave mode synchronization

In interlaced slave mode, if the IMS G335 has not been set to 'HSync during Flyback' operation, incoming HSync pulses should not be present during frame flyback. If any pulses are present during this time, then

correct field synchronization will not be possible. Master HSync pulses may be gated with the IMS G335 **Framelnactive** signal to eliminate any HSync pulses from occurring while **Framelnactive** is asserted. If the G335 has been set to operate with Hsync during flyback then, as long as the incoming pulses are identical to those produced by the G335, correct field sync will occur with or without this gating.

Position of external HSync pulses in Interlaced mode

When in interlaced slave mode, the position of the external (master) HSync pulse with respect to the internally generated IMS G335 HSync pulse, as output at the DACs, must be as shown in Figures 13.10 and 13.11. The external HSync pulse may occur anywhere between the earliest time and the latest time and must be a minimum of 1Sclk in duration.

This timing specification must be observed for all HSync pulses present during each field.

Early external HSync

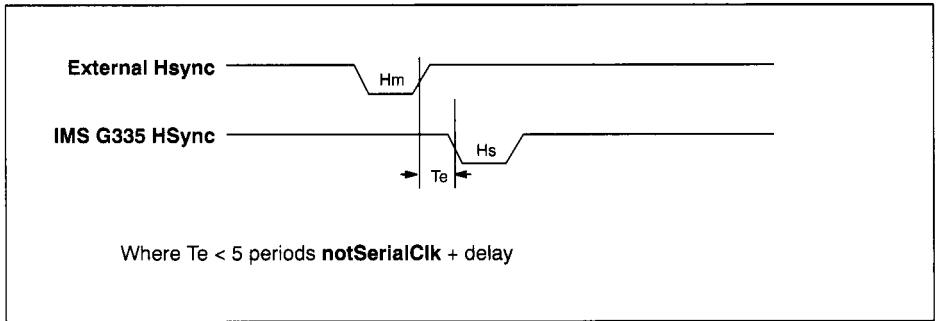


Figure 13.10 Early external HSync

The rising edge of the external HSync pulse must occur less than T_e periods of **notSerialClk** before the falling edge of the internally generated IMS G335 HSync pulse. The delay value is the programmed IMS G335 sync delay (using **Control Register A** bits 15 - 17).

Late external HSync

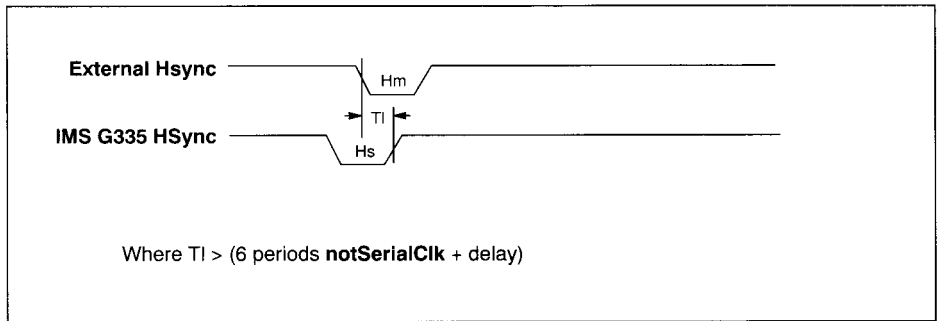


Figure 13.11 Late external HSync

The falling edge of the external HSync pulse must occur more than T_l periods of **notSerialClk** before the rising edge of the internally generated IMS G335 HSync pulse. The delay value is the programmed IMS G335 sync delay (using **Control Register A** bits 15 - 17).

13.7 Framestore manager

13.7.1 Introduction

The framestore manager provides VRAM serial port clocking, SAM refresh address and SAM transfer signal for synchronous shift register reload. Since certain pixel port modes require interleaved banks of VRAM, the framestore manager provides two complete clocking and transfer systems, one for each bank. The reload operation is conducted by a DMA into the framestore, and a fully handshaken DMA is provided for this purpose. Transfer cycles may be optionally disabled by writing to bit 14 of Control Register A.

Using this system, it is possible to implement a fully packed framestore for any pixel depth, independent of screen format and memory architecture (providing the Display parameter is a multiple of **notShiftClk** period in Screen Units).

A new mode has been introduced on the IMS G335 to provide support for VRAMs with split SAM capability, further details are given in Section 13.7.5. Operation of the IMS G335 not using split SAM support is referred to as 'synchronous mode'.

13.7.2 Non-interleaved framestore (synchronous mode)

The screen transfer operation

The IMS G335 provides software programmable strobes, **BusRequest** and **DTA**, which enable it to perform the necessary screen data-transfer cycles on video RAMs to reload their internal shift registers with new data. These may be synchronous updates which happen part way across a line or updates which occur during flyback.

The strobes are controlled by values loaded into the framestore description registers, MemInit and TransferDelay. These are loaded and incremented continuously in turn whenever the display is active (i.e. they count displayed pixels). From the start of any frame, MemInit is loaded first, then TransferDelay. An update cycle is requested at the expiry of MemInit and is completed at the expiry of TransferDelay as shown in Figure 13.12. The IMS G335 also outputs a transfer address specifying the new row of pixels to be displayed. It is left to the user to generate RAS, CAS and any other strobes needed from **BusRequest**, **DTA**, **notSerialClk** and **notShiftClk**.

The transfer sequence is as follows:

- 1 The IMS G335 asserts **BusReq**. When **BusGranted/AOE** is given, it drives **DTA** high and also drives the reload address onto **ADbus2-23**.
- 2 The IMS G335 waits until the TransferDelay period expires, during which time the system must perform a VRAM access.
- 3 After a fixed time (TransferDelay Screen Units) relative to the rising edge of **BusReq**, the IMS G335 drives **DTA** low and tri-states the **ADbus**. One **SClk** cycle later, **BusReq** will go low.

Screen maintenance

The IMS G335 uses the framestore description parameters to implement a packed framestore in the following way:

At the start of each display frame, the IMS G335 initiates a transfer cycle during the backporch of the first vertical blanked line, using the Top of Screen pointer as the transfer address. The data transfer is performed with the delay specified in the TransferDelay register.

This ensures that there is data loaded ready for the first line scan to begin.

At the start of active display the IMS G335 will begin to count **notSerialClk** cycles and will initiate a further transfer cycle after MemInit cycles of **notSerialClk**. It will then follow the transfer sequence as described

above. The falling edge of **DTA** is synchronized to **notShiftClockA** to allow synchronous mid-line updates. The whole **MemInit - TransferDelay** sequence is repeated as many times as necessary until the bottom of screen is reached. When the system reaches the end of a scan line any unused pixels in the **VRAM** shift register are held over to be displayed on the following line.

Thus the period of row transfer operations is:

$$\text{MemInit} + \text{TransferDelay} \text{ (displayed pixels)}$$

and apart from the restrictions shown in Table 13.6, it need bear no relation to the screen line length at all. This permits any display line length with any type of video RAM.

Display	=	Multiple of notShiftClk period in SUs
TransferDelay	<	BackPorch - 2
TransferDelay	≥	System DMA Latency+VRAM Access+1 SClk
Additionally, in an interlaced system only:		
MemInit + TransferDelay	=	Display
TransferDelay	<	ShortDisplay

Table 13.6 Restrictions on Framestore description parameters

The critical parameter as far as DMA accesses are concerned is **TransferDelay** which needs to be long enough to allow for the DMA latency of the drawing processor as well as the access time of the video RAMs.

Note that, with the exception of the first load operation of each frame, the framestore manager only counts **notSerialClk** cycles while the display is active, i.e. it counts displayed pixels.

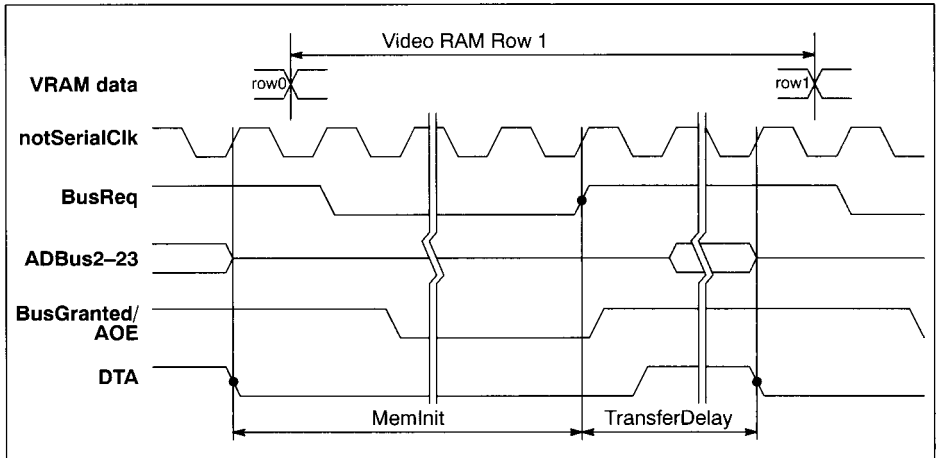


Figure 13.12 Data transfer sequence

Figure 13.12 shows the sequence of events, for a non-interleaved system, during a synchronized VRAM row transfer operation performed by the IMS G335 which takes place part-way along a display line. That is to say an uninterrupted stream of pixels is maintained during a reload of the shift registers. **MemInit** is the time from the falling edge of **DTA** to the assertion of **BusReq**; **TransferDelay** is the time between the assertion of **BusReq** to the falling edge of **DTA**.

Transfer cycles occurring during flyback

Since the IMS G335 allows the user to define an arbitrary linewidth and an arbitrary shift register length, transfer operations can in principle occur at any time during the line.

The IMS G335 uses the programmed value `TransferDelay` to schedule transfer operations early enough to ensure that the VRAM shift registers never run out of data.

Figure 13.13 shows three separate cases of transfer cycle timing:

Case 1 is where the transfer cycle occurs during backporch; this would be the case for the first backporch during vertical blank, where pixels are prefetched for the first displayed line of the frame.

Case 2 is the synchronous transfer case, where the update takes place mid-line. This will generally be the case where the screen width is not programmed to be an exact multiple of the shift register length. In order to avoid visible glitches on the screen at these times, the position of the falling edge of the transfer strobe must be synchronous with `notShiftCkA`.

Case 3 is the case where a synchronous midline update is scheduled to straddle two visible picture lines. If the IMS G335 were to start a transfer cycle at this point it would be holding the memory bus for the whole of the flyback period, preventing any processor access of memory during this time. The IMS G335 therefore holds this transfer cycle over until the start of backporch, allowing memory accesses up until this point. In order to reduce the period when processor memory access is prevented the DMA cycle does not take up the whole of backporch; the DMA operation in case 3 being of the same duration as those in 1 and 2.

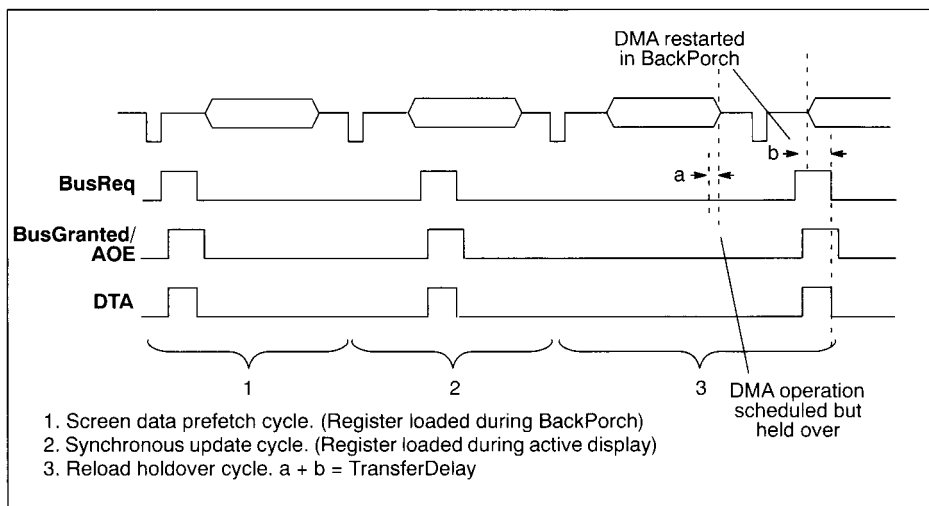


Figure 13.13 Data transfer operational behavior

If $\text{MemInit} + \text{TransferDelay} = \text{Display}$, the transfer cycle is identical to case 2, with the transfer taking place immediately after the end of the scan line.

The transfer address and top of screen pointers

The IMS G335 outputs a new 22-bit address on **ADBus2-23** during every transfer cycle it initiates irrespective of whether the micro port address alignment is set to 32 or 64-bit mode. The first address in each frame is specified in the Top of Screen register, which is programmed on startup but which can be modified at any time. Note that this register appears at two separate locations, #X02C and #X080. #X02C is accessible only when the VTG is disabled, #X080 only when it is running.

The current row address is incremented by the amount specified in bits 13-12 of Control Register A, used in conjunction with the 'Interlace' bit (bit 2). These bits specify the VRAM step length and the screen format. Refer to Table 13.7 for bit assignments.

Changes to the Top of Screen pointer become effective from the top of the subsequent screen (or field in an interlace system).

In setting MemInit + TransferDelay = Display for an interlaced system, one row transfer is made per line. Therefore since transfers are done on a line by line basis, the framestore format for interlace can be identical to that for a non-interlaced system. The address offset for the second field is added automatically by the IMS G335. Address ordering depends on the standard selected. CCIR scans even lines first, EIA scans odd lines first.

In interlace, the first half of Line Zero is always blanked at the video DACs but the IMS G335 will clock the VRAM shift registers as though visible. This preserves compatibility between interlace and non-interlace.

Register Bit		Non-interlace	Interlace	
13	12	Increment	Increment	Second field offset
0	0	1	not used	
0	1	256	2	1
1	0	512	512	256
1	1	1024	1024	512

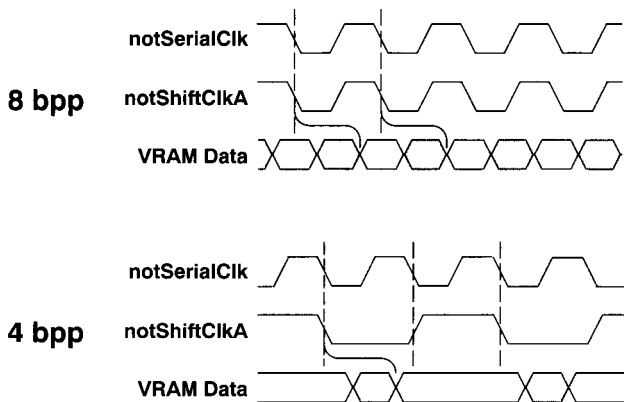
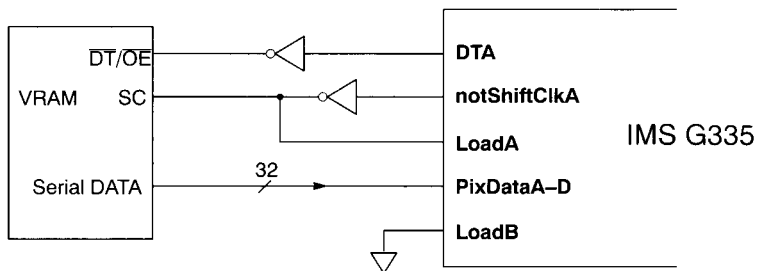
Table 13.7 VRAM address increment as set by Control Register A, bits 12 and 13

VRAM ShiftClock generation

The framestore manager automatically adjusts the frequency of **notShiftClkA** to account for different pixel depths and hence pixel port multiplex ratios.

There are five pixel formats supported in non-interleaved mode; these are shown in Table 13.10, page 197 along with the multiplex ratio of the pixel port and the period of ShiftClock generated by the framestore manager.

ShiftClock generation and usage are illustrated in Figure 13.14. Note that both **notShiftClkA** and **DTA** are buffered and inverted before use.



Note: The remaining modes adjust the frequency of **notShiftClkA** in line with the above diagrams.

Figure 13.14 Non-interleaved VRAM

13.7.3 Interleaved framestore (synchronous mode)

Because of the very high video rates supported by the IMS G335 it is not possible in some situations to supply pixel data fast enough from a single bank of Video RAMs. An interleaved mode has been provided to allow two banks of VRAM to be used, each running at half the frequency required when using a single bank. 32 bits of pixel data are loaded alternately from one VRAM bank then the other.

In interleaved mode, two **notShiftClk** and the **DTA/B** signals are used to control the two banks, the shift clocks running in anti-phase. It can be seen that the falling edge of **notShiftClkA** will cause data to be driven out from VRAM Bank A into the **PixData** input of the IMS G335.

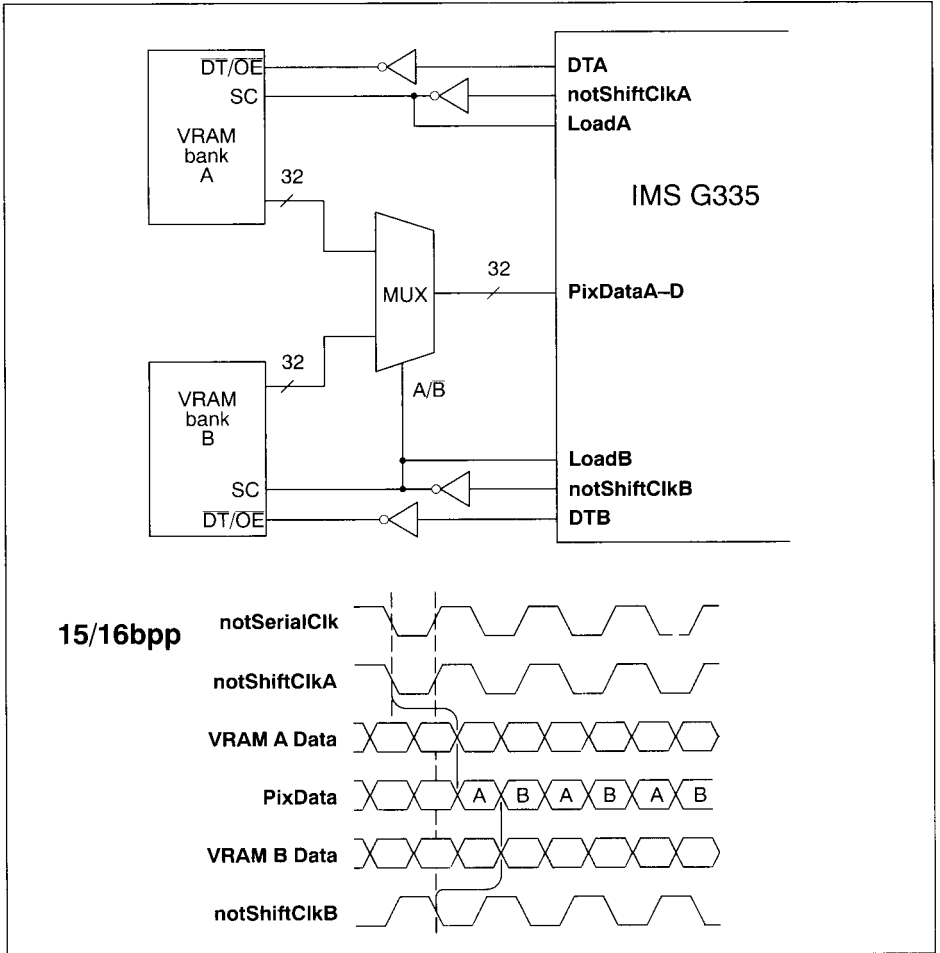


Figure 13.15 Interleaved VRAM banks

Interleaved VRAM control

In order to implement an interleaved framestore, the IMS G335 provides a second set of VRAM clock and transfer signals; **notShiftClkB** and **DTB**. **notShiftClkB** runs in antiphase to **notShiftClkA** so that the data in each bank is skewed by one half the **notShiftClk** period. The two streams of data can then be multiplexed into the IMS G335.

The effect of this is that each bank of video RAM must be clocked at half the rate which would be necessary for a non-interleaved framestore. This is taken into account by the IMS G335 and the ShiftClock periods for all possible pixel depths in interleaved mode are shown in Table 13.11, page 198.

An interleaved framestore system is shown in Figure 13.15, along with the **notShiftClk** and VRAM data waveforms for 15/16 bits per pixel format. In this mode, the IMS G335 alternately samples pixel data from VRAM bank A and B.

The timing of **notShiftClkA** and **notShiftClkB** differs at the beginning and the end of each line, such that the bank select signal must be derived, as shown in Figure 13.15, from the **notShiftClkB** signal and **notShiftClkA**.

VRAM reload in an interleaved framestore

The basic reload cycle in interleaved format is the same as the standard format. The difference is that, because of the skew between **notShiftClkA** and **notShiftClkB**, the **DTB** strobe must be delayed by a similar amount with respect to **DTA**. This amount varies depending on the pixel depth, and is automatically adjusted by the IMS G335.

The data transfer sequence is shown in Figures 13.16 to 13.18 for 16, 8 and 4 bpp, the remaining modes being simply an extension of these waveforms.

In all cases, the beginning of the DMA cycle is identical to the non-interleaved case, the difference being that the falling edge of **DTB** is delayed by one half period of **notShiftClk(A or B)**, with **BusReq** remaining asserted until one period **notSerialClk** after the falling edge of **DTB**. Also, the reload address driven onto the ADBus remains valid until after the falling edge of **DTB**.

Note that all the VRAM controls and clocks, **DTA/B** and **notShiftClkA/B** must be buffered and inverted before use.

Use of an interleaved system affects the framestore description parameters in that the effective VRAM shift register length is doubled from that in non-interleaved mode. Meminit must therefore be modified to account for this, leaving TransferDelay the same.

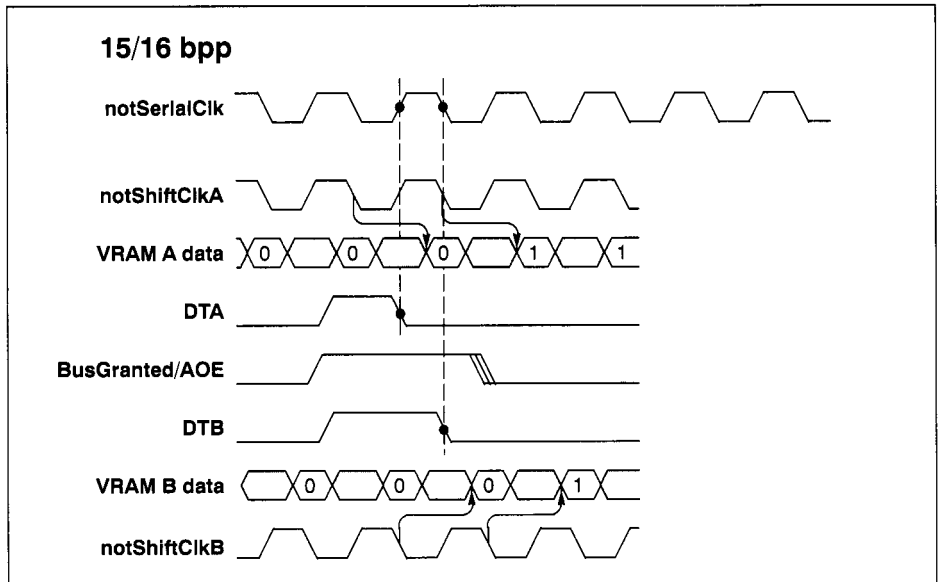


Figure 13.16 Data transfer sequence - interleaved, 15/16bpp

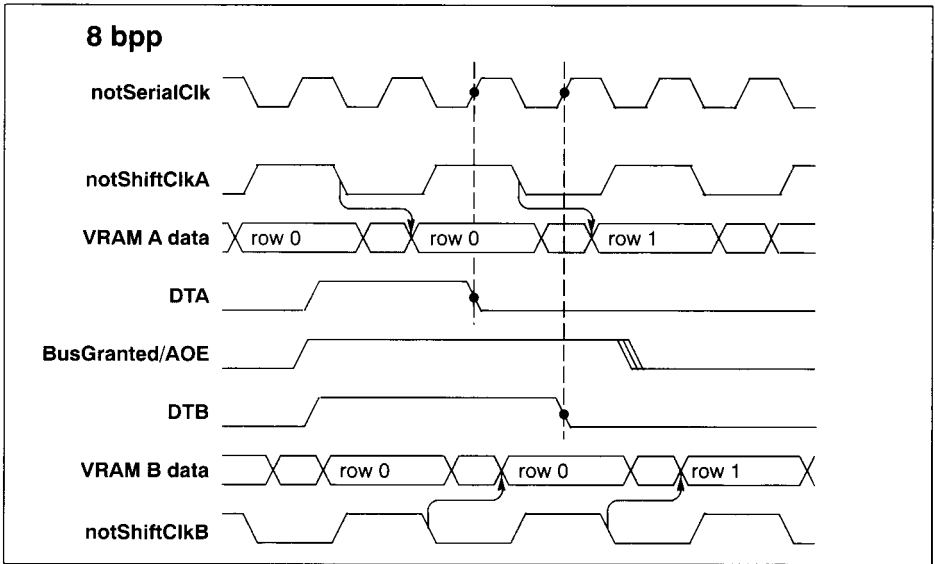


Figure 13.17 Data transfer sequence - interleaved, 8bpp

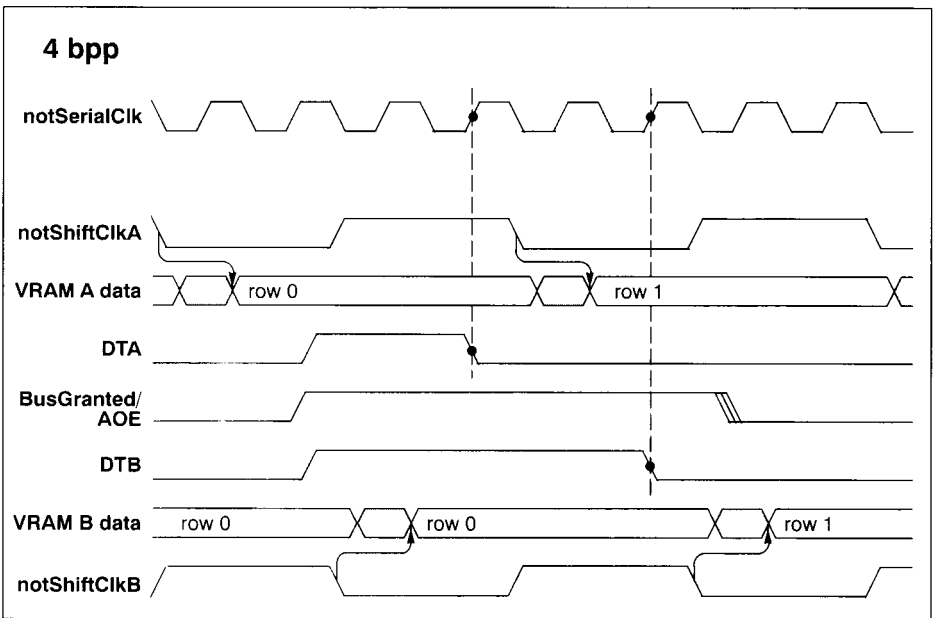


Figure 13.18 Data transfer sequence - interleaved, 4bpp

13.7.4 Framelnactive

A further timing signal, **Framelnactive**, is provided which can be used to convey frame timing information to the host. This signal may be used in multiboard systems where frame swapping is used to implement animation, for example. **Framelnactive** is asserted whenever the timing generator enters frame flyback and is deasserted on entering active display.

13.7.5 Split SAM VRAM support

The use of split Serial Access Memory (SAM) Video RAM allows simplified system design and reduces bus control time significantly. Split SAM devices have their serial shift register split into two, one half being updated while the other half is shifting out. The transfer window for split SAM devices is increased from 1 shift clock period to half the period of the entire serial shift register, making the update timings much less critical and system design easier.

The IMS G335 split SAM mode provides support for VRAMs with a split SAM capability. In this mode the VRAM update timings are less critical than for seamless (synchronous) update; VRAM update being completed by the system after initiation by the IMS G335. Bus control time is reduced since the bus is cycled as fast as the system allows instead of being governed by worst-case timings programmed into TransferDelay.

In split SAM mode some pin functions are changed compared with their operation in synchronous mode, (see Table 13.8).

Pin	Synchronous mode		Split SAM mode	
	I/O	Function	I/O	Function
DTA	O	Performs transfer of VRAM A data synchronous to notShiftClkA	x	not used ¹
DTB	O	Performs transfer of VRAM B data synchronous to notShiftClkB	x	not used ¹
BusReq	O	Requests DMA cycle	O	Requests DMA cycle.
BusGranted/AOE	I	Grants DMA cycle, drives refresh address onto ADBus.	I	Rising edge drives refresh address onto ADBus, falling edge tri-states ADBus and cancels BusReq.
Note: 1 The DTA and DTB pins are active during split SAM DMA cycles although not performing transfer of VRAM data. TransferDelay must still be programmed with a value satisfying the conditions given in Table 13.5, though not directly used.				

Table 13.8 Pin functions in synchronous and split SAM modes

Operation of the split SAM mode

The split SAM mode works as follows:

At the start of each field, during the backporch of the first vertical blanked line, the IMS G335 requests a data transfer, using the Top of Screen pointer as the transfer address. At the conclusion of this transfer, it increments the transfer address by the amount specified in Control Register A. As soon as the displayed screen is reached and pixels are being clocked out of the VRAM serial port, the IMS G335 uses MemInit to set the period of data transfer requests.

At the point when MemInit expires, **BusReq** will go high, after which a rising edge on **BusGranted/AOE** will turn on the **ADBus** with the refresh address. The system is then free to perform the transfer cycle in any way it sees fit. On the falling edge of **BusGranted/AOE**, the **ADBus** will be tristated and **BusReq** driven low with a $1\frac{1}{4}$ SClk delay. No timing information will be supplied by the IMS G335 other than the initial bus request. At the conclusion of each transfer operation during display, the transfer address is incremented by **half** the amount specified in Control Register A, bits 12-13. The VRAM step length is shown in Table 13.9.

In interleaved mode, data transfer can occur in both banks simultaneously. The IMS G335 automatically delays the transfer request until bank B has finished clocking data out of the relevant shift register. This delay will vary depending on the bits per pixel mode and must be subtracted from the time available for transfer to occur.

Register bit		Split SAM VRAM address increment	
13	12	First backporch in VBlank	During displayed screen
0	0	not allowed	not allowed
0	1	256	128
1	0	512	256
1	1	1024	512

Table 13.9 Control of split SAM VRAM address increment

In normal operation the first transfer in each field is a non-split transfer while the remainder will be split transfers. The **FrameInactive** signal can be connected to the VRAM's DSF pin to perform this switch since it is high only during the prefetch transfer which occurs during vertical retrace. During all other transfer operations, it is guaranteed to be low.

A block diagram showing example connections between VRAM and the IMS G335 in split SAM mode is given in Figure 13.19. A timing diagram for split SAM mode is given in Figure 13.35, page 219.

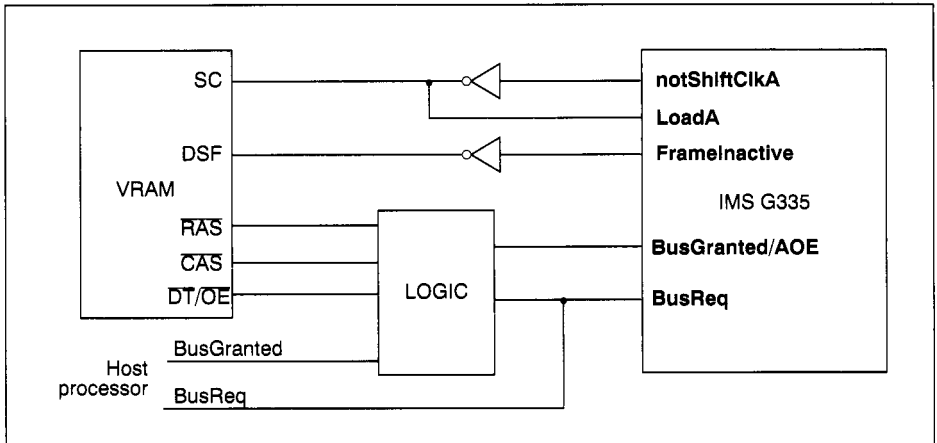


Figure 13.19 Example VRAM connections in split SAM mode

Split SAM support in interlaced mode

The IMS G335 provides support for split SAM operation in interlaced mode, allowing the use of similar VRAM connections and logic to those shown in Figure 13.19. In interlaced split SAM mode the following conditions apply:

- 1 Control Register A, bit 1 must be set to interlaced mode, Control Register A, bit 2 may be set to either EIA or CCIR standard and Control Register B, bit 3 must be set to split SAM operation.
- 2 The VRAM address increments are identical to those shown in Table 13.7, page 190 for non split SAM operation.
- 3 The VRAM should be configured to perform unsplit transfers (i.e. the VRAM DSF pin should be held low) even though split SAM is selected on the IMS G335. This enables the same **BusReq/AOE** logic to be used for both non-interlaced and interlaced split SAM modes.
- 4 MemInit must be set to the same value as Display; this ensures that a row transfer occurs at the end of each line, enabling the framestore manager to generate the two interlaced display fields from a single contiguous framestore.

13.8 The Pixel Port

The IMS G335 has a 32-bit wide pixel input port which can be programmed to sample pixels in a number of pixel depths and formats, summarized in Tables 13.10 and 13.11.

13.8.1 Non-interleaved framestore

The IMS G335 supports five depths of pixel using a non-interleaved framestore (illustrated in Figure 13.14, page 191).

Control Register A bits				Bits per pixel	ShiftClk period	MUX ratio	Use of LUT
22	21	20	18				
1	1	0	0	24	1 SCIk	1:1	Full color*
0	1	1	0	8	1 SCIk	4:1	Pseudo color
0	1	0	0	4	2 SCiKs	8:1	Pseudo color
0	0	1	0	2	4 SCiKs	16:1	Pseudo color
0	0	0	0	1	8 SCiKs	32:1	Pseudo color

*Note that in this mode 1SU = 1 pixel (see Section 13.8.3)

Table 13.10 Non-interleaved pixel modes

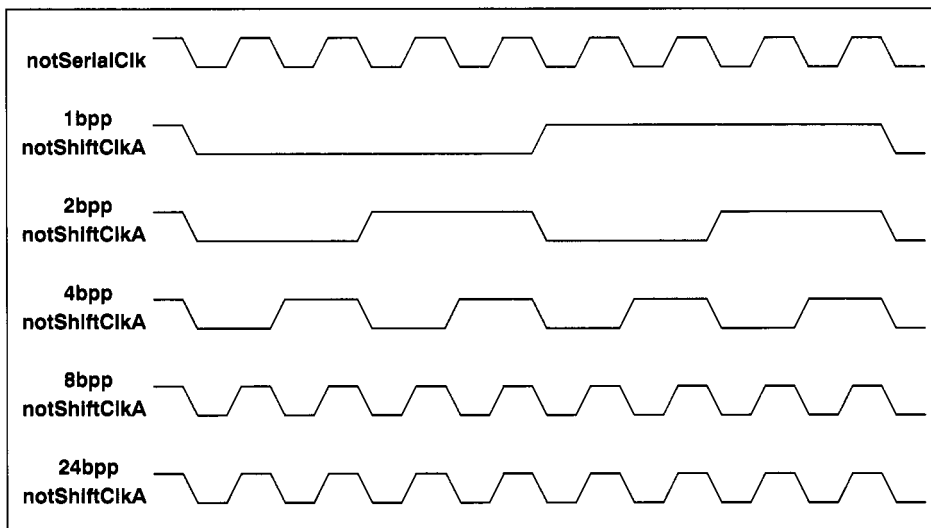


Figure 13.20 notShiftClkA operation in non-interleaved pixel modes

13.8.2 Interleaved framestore

In interleaved mode, the IMS G335 supports seven depths of pixel as shown in Table 13.11. Interleaved sampling is necessary to implement the true color modes, and the remaining modes are supported to allow for a consistent framestore design. The interleaved framestore system is introduced in Section 13.7.3, page 192.

Control Register A bits				Bits per pixel	ShiftClk period	MUX ratio	Use of LUT
22	21	20	18				
1	1	0	1	24	1 SClk	1:1	Full color*
1	0	1	1	16	1 SClk	2:1	True color
1	0	0	1	15	1 SClk	2:1	True color
0	1	1	1	8	2 SClks	4:1	Pseudo color
0	1	0	1	4	4 SClks	8:1	Pseudo color
0	0	1	1	2	8 SClks	16:1	Pseudo color
0	0	0	1	1	16 SClks	32:1	Pseudo color

*Note that in this mode 1 SU = 2 pixels (see Section 13.8.3)

Table 13.11 Interleaved pixel modes

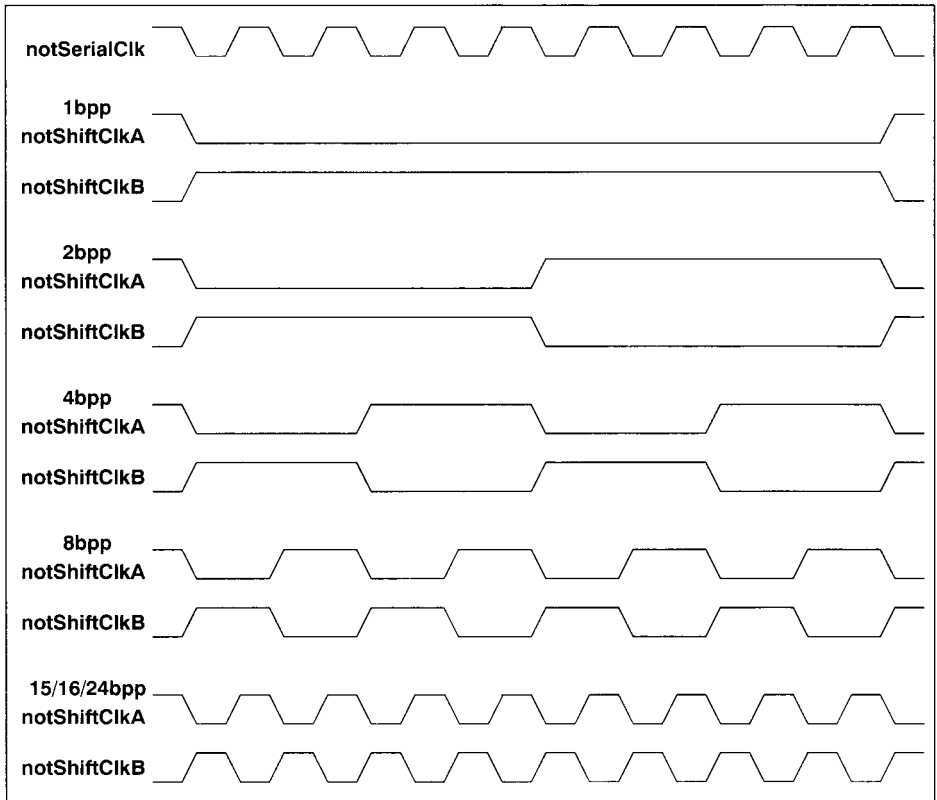


Figure 13.21 notShiftClkA/B operation in interleaved pixel modes

13.8.3 24-bits per pixel modes

Since only one 24-bit pixel at a time can be latched at the pixel input port, these modes are limited to operation at below the maximum rated device video rate. Latched pixel repetition is used to implement 24-bit functionality, whilst the internal device video pipeline remains operating at four pixels per SClk cycle. Thus in non-interleaved mode, since only one pixel can be latched in per SClk, the maximum video dot rate achievable is one quarter of the device rated speed. In interleaved mode, since two pixels can be latched in per SClk, the maximum video dot rate is one half of the rated speed.

Screen Units

As a result of the above, when programming the video timing generator screen description registers, the number of pixels per 'Screen Unit' (SU) used to calculate parameter values in these modes differs from the four pixels per SU used in other modes:

In 24bpp non-interleaved mode, 1 SU = 1 pixel
In 24bpp interleaved mode, 1 SU = 2 pixels

Clock frequency

The PLL clock frequency multiplication factor programmed into the Boot Location must differ from that required to produce the apparent displayed video dot rate in these modes:

In 24bpp non-interleaved mode, the device operating speed = video dot rate \times 4
In 24bpp interleaved mode, the device operating speed = video dot rate \times 2

Thus, for example, if a 25MHz VGA screen is required to be displayed in 24bpp from a non-interleaved framestore, then the IMS G335 must be programmed to operate with the PLL set to 100MHz, and the horizontal timing parameters calculated with one pixel per Screen Unit.

13.8.4 Pixel sampling modes

For both interleaved and non-interleaved framestores there are two alternate pixel sampling modes, software selectable via Control Register B, bit 0 (see Table 13.23, page 214):

- Internal sampling, whereby the pixel port automatically samples the pixel information without the need for an external load signal. The sampling frequency and sampling point are adjusted to cope with the specified pixel format and the type of framestore, interleaved or non-interleaved, which is being supported.
- External sampling, in which pixels are sampled according to strobes on the **LoadA** and **LoadB** input pins.

This mode allows higher sampling speeds to be achieved through shorter VRAM data set up and hold times. By eliminating the need to consider the tolerance of an external buffer and the skew between clocking and latching signals, much faster clocking of data out of VRAM is possible. Design of high speed systems is simplified since no matching of buffer propagation delays, capacitance loading or signal skew is required.

Internal sampling

The IMS G335 generates an internal pixel sampling signal derived from the **notShiftClkA(B)** signal(s). The sampling windows in non-interleaved and interleaved modes are defined as follows:

Non-Interleaved mode

The pixel data is sampled around the the first falling edge of **notShiftClkA** after any previous falling edge of **notShiftClkA**. The data must be set up with respect to the latching edge and remain valid until after it with the timings as given in Table 13.34, page 225.

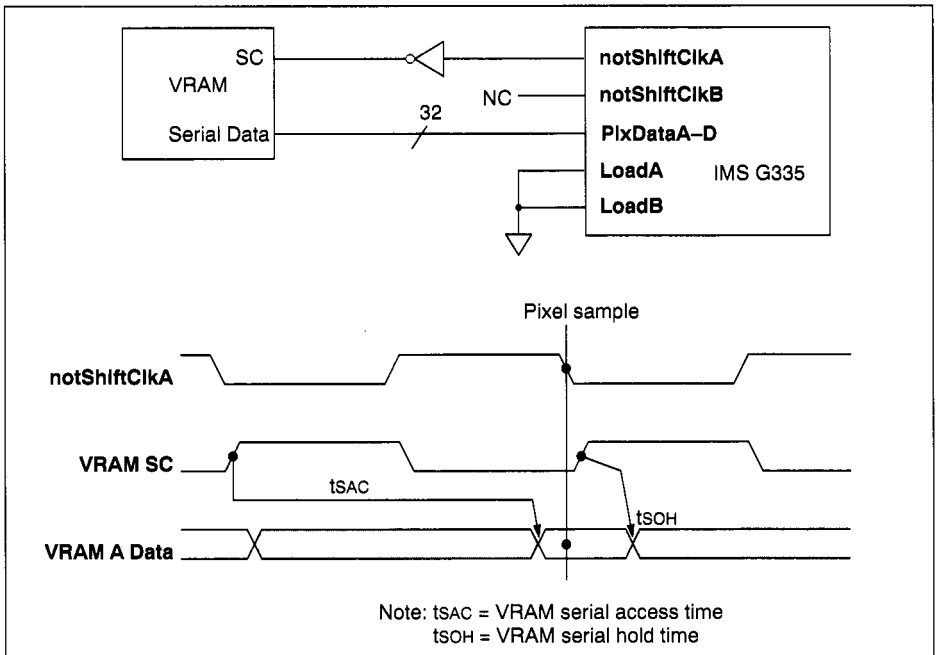


Figure 13.22 Non-interleaved, internal sampling example

Interleaved mode

VRAM bank A pixel data is sampled around the first falling edge of **notShiftClkA** after any previous falling edge of **notShiftClkA**. The data must be set up with respect to the latching edge and remain valid until after it with the timings given in Table 13.34, page 225.

VRAM bank B pixel data is sampled around the first falling edge of **notShiftClkB** after any previous falling edge of **notShiftClkB**. The data must be set up with respect to the latching edge and remain valid until after it with the timings given in Table 13.34, page 225.

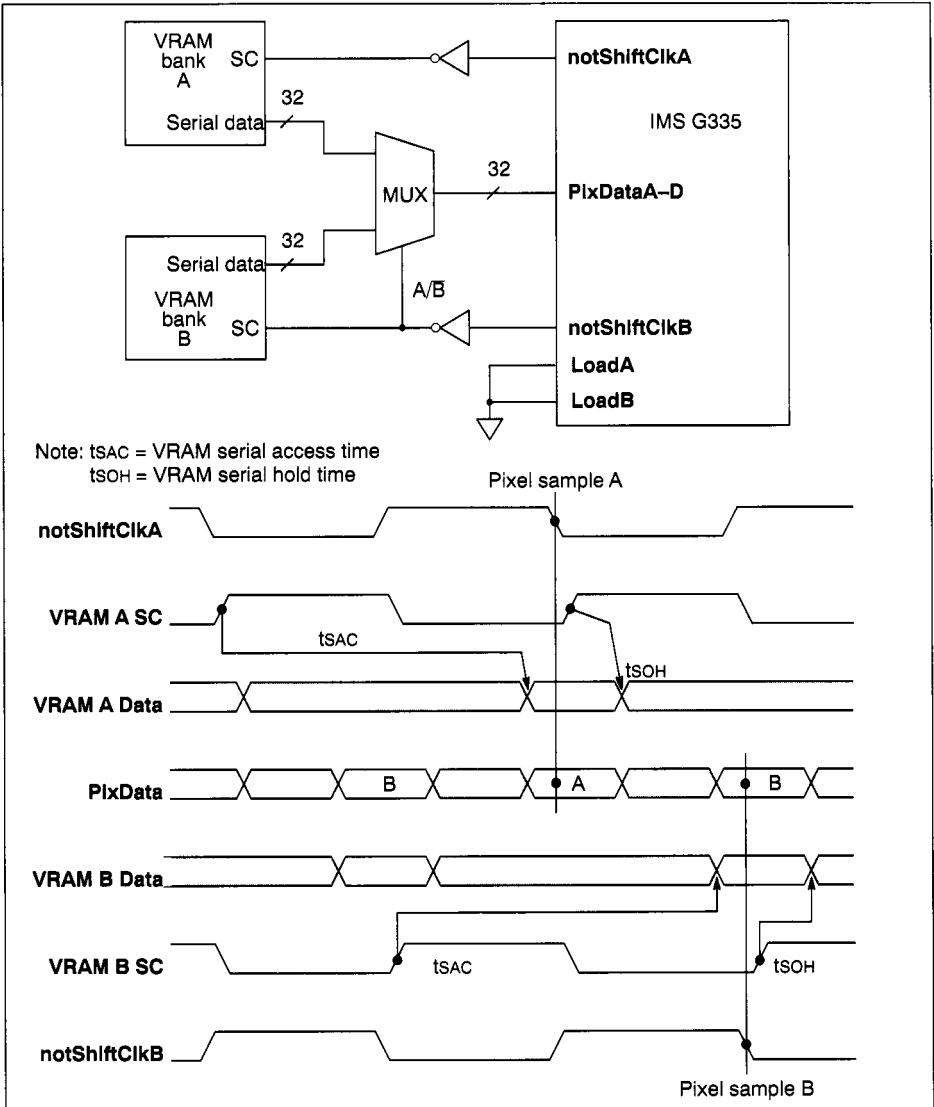


Figure 13.23 Interleaved, internal sampling example

External sampling

The IMS G335 samples pixels relative to the **LoadA/B** input pins. The sampling windows in non-interleaved and interleaved modes are defined as follows:

Non-interleaved mode

The pixel data is sampled around the first rising edge of **LoadA** after any previous rising edge of **LoadA**. The data must be set up with respect to the latching edge and remain valid after it with the timings given in Table 13.35, page 225.

The latching **LoadA** rising edge must occur within the valid sampling window (t_{CLLH} , Table 13.35) relative to the previous falling edge of **notShiftClkA**.

The **LoadB** pin must be held inactive to ground.

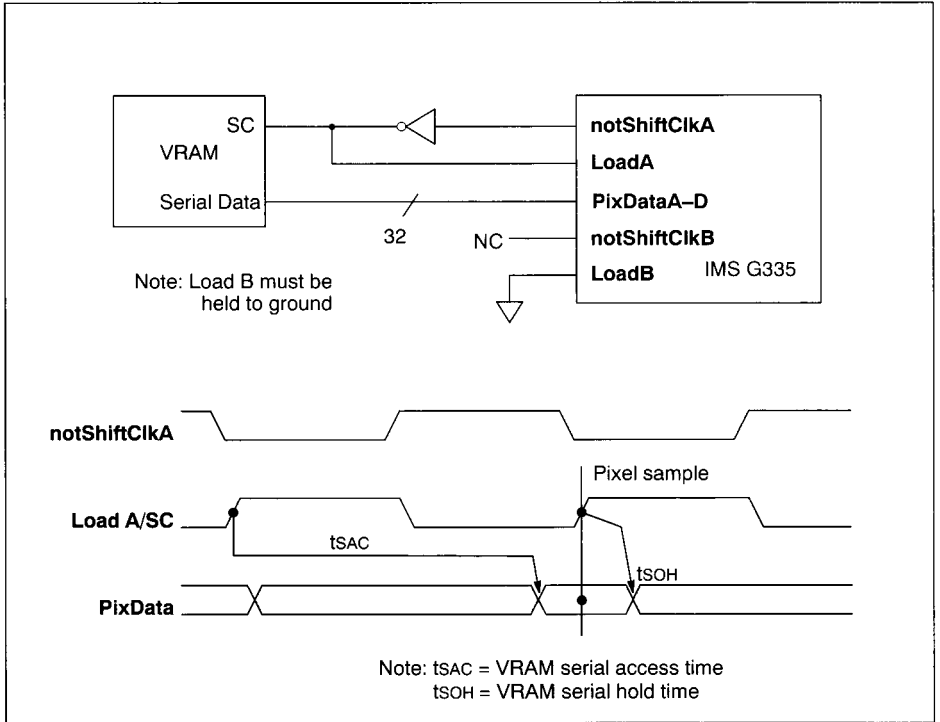


Figure 13.24 Non-interleaved, external sampling example

Interleaved mode

VRAM bank A pixel data is sampled around the first rising edge of **LoadA** after any previous rising edge of **LoadA**. The data must be set up with respect to the latching edge and remain valid until after it with the timings given in Table 13.35, page 225.

VRAM bank B pixel data is sampled around the first rising edge of **LoadB** after any previous rising edge of **LoadB**. The data must be set up with respect to the latching edge and remain valid until after it with the timings given in Table 13.35, page 225.

The latching **LoadA/B** rising edge must occur within the valid sampling window (t_{CLLH} , Table 13.35) relative to the previous falling edge of **notShiftClkA/B**.

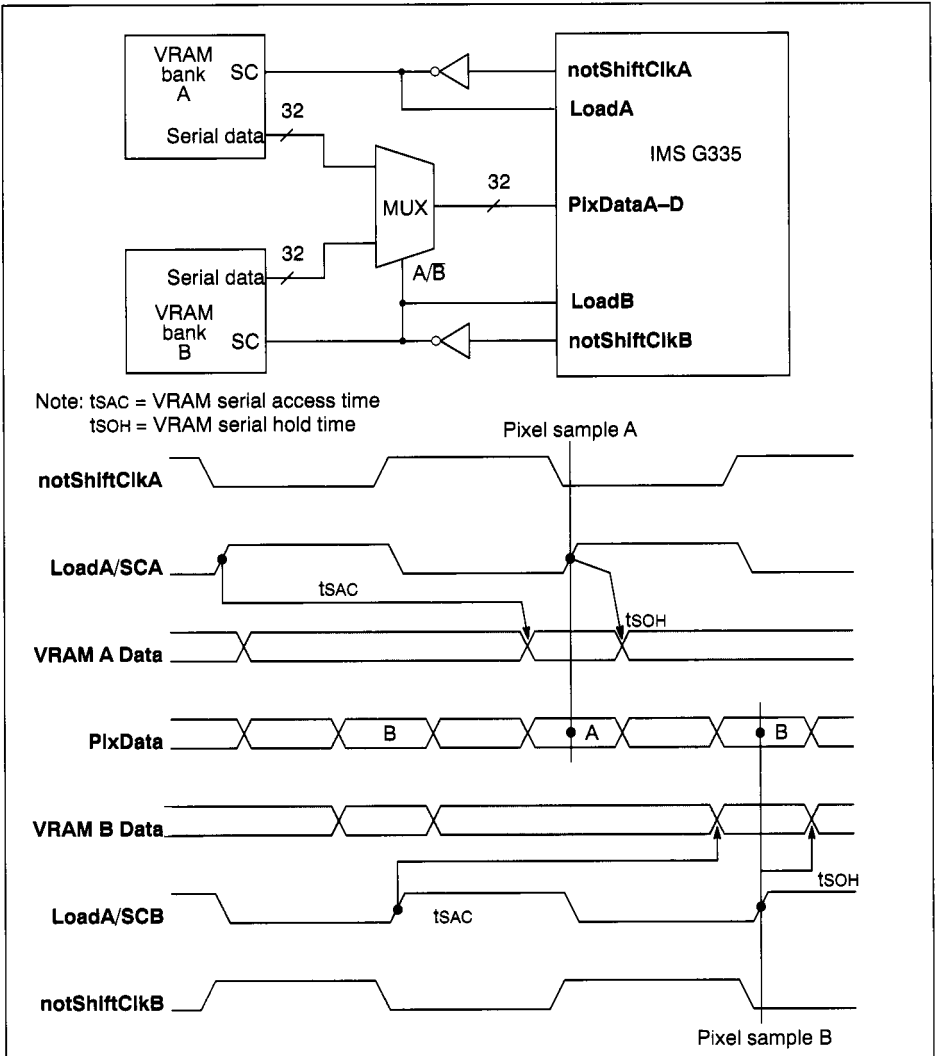


Figure 13.25 Interleaved, external sampling example

13.8.5 Pipeline delays in the pixel path

It can be seen that the pipeline delay between the VRAM and the DAC outputs depends on the bits per pixel format. The IMS G335 automatically adjusts the internal pipeline delays of the sync and blank signals, as well as cursor position, to account for this. These delays are specified in Figure 13.37, page 221.

Extra pipeline delays

It is possible to delay the point at which sync and blank signals are applied to the pixel stream, by setting bits 17-15 of Control Register A. These bits are binary coded to produce 0-7 **notSerialClk** periods of delay in addition to the pixel-format dependent delays described above. This facility is useful if extra video streams are to be switched into the pixel path, or buffering down a backplane is needed.

If this facility is required, any external pipeline delay in the pixel path must be matched in the pixel sampling pin(s) **LoadA** (and **LoadB**). This facility is **not** available in internal sampling mode.

13.8.6 Pixel formats

True color modes (15 and 16 bits per pixel)

Each pair of pixel ports (A and B, and C and D) supplies a two-byte pixel value which is split into red, green and blue fields as illustrated below. The ports are used in the order A,B then C,D. In 15 bits per pixel mode bits 0-4 are blue, 5-9 are green, and 10-14 are red (RGB format 5,5,5). In 16 bits per pixel mode bits 0-4 are blue, 5-10 are green, and 11-15 are red (RGB format 5,6,5).

Full color mode (24 bits per pixel)

Ports A, B and C supply the displayed pixel; pixel data on port D is ignored. The byte/color assignment is shown in Figure 13.27.

For all the 15, 16 and 24bpp formats the resulting Red, Green and Blue pixel values are passed through the color palette, which can act as a gamma correcting table, before being displayed by the DACs.

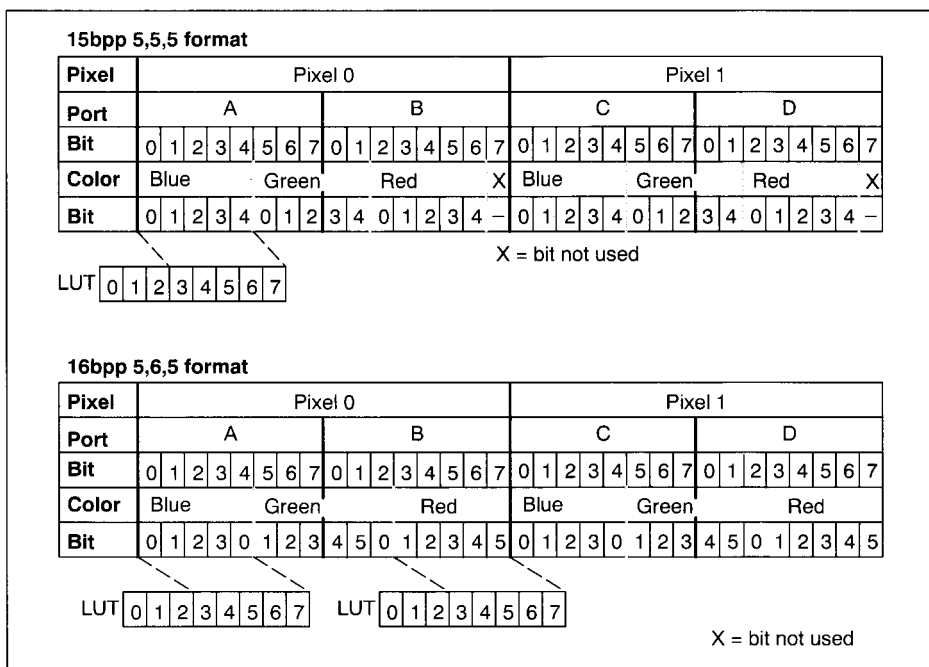


Figure 13.26 Pixel mapping for 15 and 16bpp

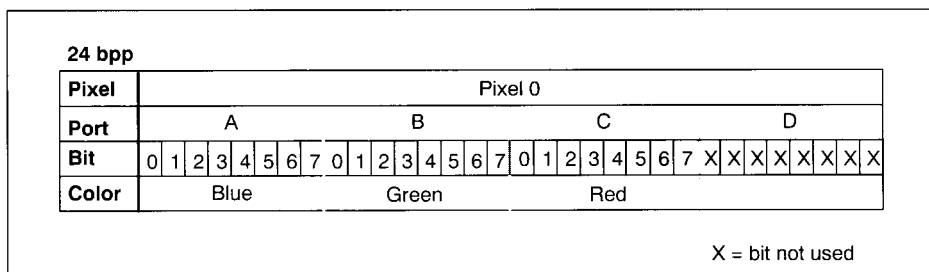


Figure 13.27 Pixel mapping for 24bpp

Pseudo color modes (1, 2, 4 and 8 bits per pixel)

The latched pixel data is serialized to the color palette in the order Port A, B, C, and D. Each pseudo pixel is masked by the 8-bit mask register before acting as a pointer to a pre-loaded 24-bit color in the color palette.

Reduced pixel format sizes use the lower order address bits and therefore access the lower color palette locations.

Pixel mode	Pixels per port	1st pixel	Last pixel	LUT address bits	LUT locations used
8	1	Bits 0-7	–	0-7	0-255
4	2	Bits 0-3	Bits 4-7	0-3	0-15
2	4	Bits 0-1	Bits 6-7	0-1	0-3
1	8	Bit 0	Bit 7	0	0-1

Table 13.12 Pseudo color modes

13.9 Hardware cursor

To reduce the amount of external hardware and limit software overhead, an on-chip cursor store is provided on the IMS G335. This is memory mapped through addresses #X200-3FF. The result is a 64 line×64 pixel three color cursor, with transparency and pixel complement options. The cursor is enabled or disabled by bit 23 in Control Register A (Address #X060).

13.9.1 Cursor store Micro port address #X200-3FF

The cursor store is addressed as 512×16 bit words, each word being formatted into 8 pixels×2 bits.

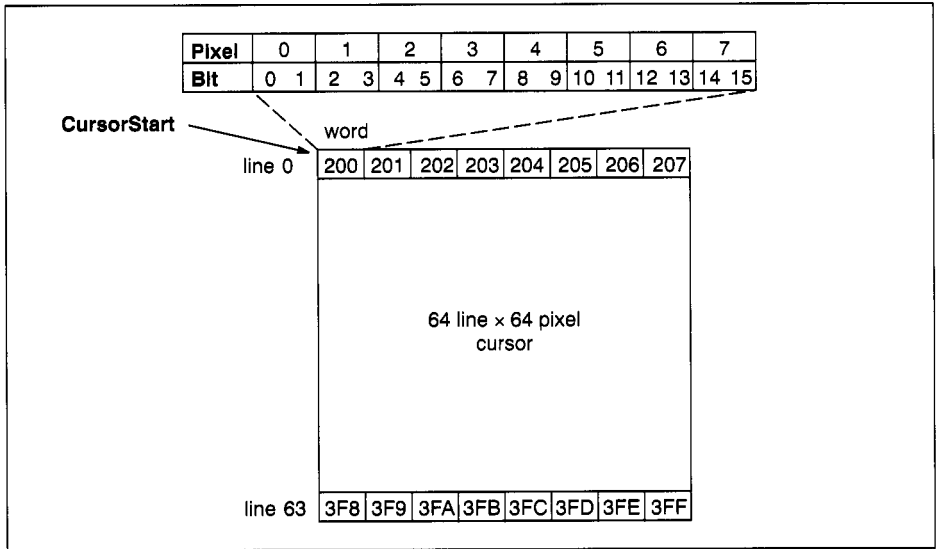


Figure 13.28 Cursor store format

13.9.2 Cursor palette Micro port address #X0A1-3

The cursor palette consists of 3 × 24 bit color registers.

Bit	23 – 16	15 – 8	7 – 0
Color	Red	Green	Blue

Table 13.13 Cursor palette color register

13.9.3 Cursor pixel options

Three options are available to determine cursor pixel appearance, depending on the setting of Control Register B, bits 12 and 13 (see Table 13.14).

Control Reg. B		Function
Bit 13	Bit 12	
0	0	Standard cursor, 3 colors + transparency
0	1	2 colors + transparency + complement (pixel complement option)
1	0	Invalid
1	1	XGA cursor format

Table 13.14 Selection of cursor pixel options

Default cursor setting

On reset, the cursor defaults to the standard format setting.

Pixel complement

The pixel complement option replaces one of the cursor colors with 'pixel complement'. This generates the complement (all bits inverted) of the pseudo or true color pixel already on the screen, ensuring that cursor pixels programmed with this will always be visible whatever the background. This option is selectable through bit 12 of Control Register B.

XGA cursor format

The XGA cursor option maps the cursor palette according to the XGA standard. This option is selectable through bit 13 of Control Register B.

Depending on which option is selected the 2-bit pixel values are decoded as shown in Table 13.15.

Pixel value	Standard format	Pixel complement option	XGA format
0 0	Cursor transparent. Background color displayed.	Cursor transparent. Background color displayed.	Color from cursor palette register 2
0 1	Color from cursor palette register 1	Complement of background color	Color from cursor palette register 3
1 0	Color from cursor palette register 2	Color from cursor palette register 2	Cursor transparent. Background color displayed.
1 1	Color from cursor palette register 3	Color from cursor palette register 3	Complement of background color

Table 13.15 Cursor pixel decoding

13.9.4 Cursor position Micro port address #X0C7

Cursor position is held in a single 24-bit register as an x-y location relative to the top left (0,0) of the screen. The position defined is that of the topmost, leftmost pixel of the cursor (**CursorStart**). The x-address and y-address are two's complement values in the range -64 to 2047.

Bit	23	12	11	0
	x-address (horizontal)		y-address (vertical)	

Table 13.16 Cursor position register

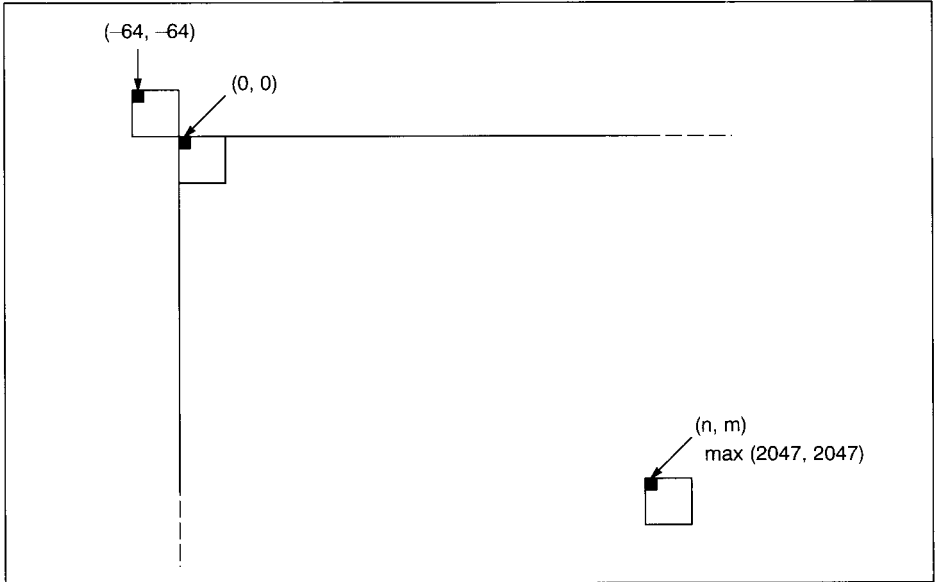


Figure 13.29 Cursor position

Maximum X-address

The X position of **CursorStart** must never exceed n+1 where n is the number of pixels on a line. The absolute limit is n=2046

Maximum Y-address

The Y position of **CursorStart** may be any value up to 2047 irrespective of screen dimensions.

13.9.5 Cursor offset for displays with short BackPorch

For displays where BackPorch is defined as less than 16 Screen Units the cursor position will be offset to the right by:

$$\text{Offset} = (16 - \text{BackPorch}) \text{ Screen Units}$$

13.9.6 Cursor x-resolution in 24 bits per pixel modes

The horizontal resolution of the cursor does not change in these modes even though the pixel resolution changes. Thus in 24 bpp, non-interleaved, the cursor occupies 16 horizontal pixels, while in 24 bpp, interleaved, it occupies 32 horizontal pixels. In both cases, the cursor still has a resolution of 64 pixels, i.e: it is 4x and 2x the horizontal resolution of the screen.

The cursor is always 64 lines high, whatever the pixel mode.

13.10 Anti-sparkle color palette

The color palette consists of 256x 24 bit color registers.

Bit	23 – 16	15 – 8	7 – 0
Color	Red	Green	Blue

Table 13.17 Color palette - color register

These read/write registers are located at Micro port address #X100 - #X1FF.

The color palette is used both by the pseudo color pixels (as an expansion table) and by the true color pixels (each component can address a different location, at which there can be a gamma correction value).

If it is required to display an expanded pseudo color picture and a true color picture without reloading the palette in between, then the simplest solution is to write the color number to each of the Red, Green and Blue portions of each color palette register. This is shown in Table 13.18.

Color register	Value (hex)
0	00 00 00
1	01 01 01
...	...
254	FE FE FE
255	FF FF FF

Table 13.18

When using the pseudo-color modes this would produce a grey scale from black (0) to white (255). In true color modes this would allow each color to be varied from low intensity (0) to high intensity (255).

13.10.1 Gamma correction

Due to the nature of the phosphors used on color monitor screens, color intensity displayed is not a linear function of the applied electron beam energy. The relationship between monitor input voltage and the observed intensity on the screen is approximated by the power curve shown in Figure 13.30.

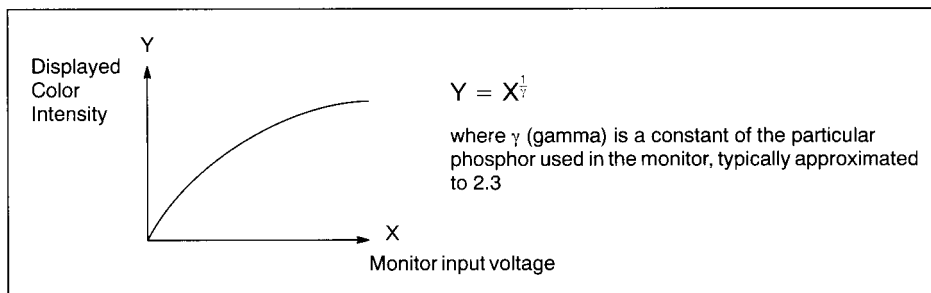


Figure 13.30 Gamma correction power curve

To create a gamma corrected color palette each register value is calculated as follows:

$$\text{Corrected color value} = 255 \times \left(\frac{\text{color value}}{255} \right)^{\frac{1}{\gamma}}$$

Therefore palette value = a log (γ log (color value)), where color value is the required intensity.

$$\text{Hence palette value} = 255 \times \text{a log} \left\{ \gamma \log \left(\frac{\text{color value}}{255} \right) \right\}$$

Color value	0	25	50	75	100	125	150	175	200	225	255
Corrected value	0	1	6	15	30	49	75	107	146	191	255
Corrected value (hex)	00	01	06	0F	1C	31	4B	6B	92	BF	FF

Table 13.19 Example results for $\gamma=2.3$

13.10.2 Mask register

The 8-bit mask register masks the pseudo-color pixel inputs to the three LUTs. Setting a bit in the mask register to zero causes the corresponding LUT address bit to be set to zero. The mask register has no effect on the picture when the IMS G335 is operating in true color modes.

13.10.3 Anti-sparkle operation

The IMS G335 includes a 256x24 bit color look up table which is mapped directly into the micro port address space. Complete color values are written by a single write cycle on the micro port. In order to minimize picture disturbance whilst a color palette entry is being accessed, the previous pixel is repeated at the DACs. This enables updates to the color palette during the active display period rather than having to wait for frame flyback.

13.11 Checksum registers

There are three 24-bit checksum registers, one for each color channel. Their purpose is to facilitate testing the device and systems containing it. The checksum is located directly before the DACs and after the color and cursor palettes.

The checksum registers are reset by the falling edge of **FrameInactive**. They accumulate only those pixels which are visible on the screen, i.e. those pixels which are unblanked. The checksum value is dependent on the cursor position and whether or not interlaced mode is selected, but independent of sync modes and flyback patterns. The registers should be read during the first part of frame flyback. At the end of this period they are reset, and at other times they are accumulating and are consequently invalid.

The checksum registers are addressed from the microport as 24-bit words containing low, middle and high bytes as follows:

Micro port address	Bits 16-23	Bits 8-15	Bits 0-7
#X0C0	Red bits 0-7	Green bits 0-7	Blue bits 0-7
#X0C1	Red bits 8-15	Green bits 8-15	Blue bits 8-15
#X0C2	Red bits 16-23	Green bits 16-23	Blue bits 16-23

Table 13.20 Checksum registers

The checksum is a shift register that uses feedback to create a pseudo-random sequence. As each pixel arrives, its 8-bit value is XOR-ed with the lowest 8 bits of the register, and the register is shifted. The feedback minimizes the risk of two errors in the pixel stream cancelling to give a correct checksum value.

Checksums may be generated for given test screens either by using a "golden chip" which is known to be working correctly, or by computing with the algorithm given in Section 17.4, page 345.

Checksum test

The IMS G335 includes an option to implement a checksum test with zero data applied directly to the checksum register. The effect of this is to test the register itself prior to further system diagnostics. The checksum test option is selected through Control Register B, bit 8.

13.12 The video DACs

The video DACs have 8-bit resolution, and are designed to drive a doubly terminated 75Ω transmission line and produce analogue outputs compatible with RS170 and RS343 video standards.

The DACs work by sourcing a current proportional to their digital input. The DAC unit current for each digital increment is defined by an external **Iref** current source:

$$1 \text{ DAC unit} = I_{\text{ref}}/120$$

The video information output by each gun ranges from 0 to 255 units under the control of the digital input from the color palette or the pixel pin.

A sync pedestal of 108 DAC units and a blanking pedestal of 20 DAC units are provided. The sync pedestal allows superposition of the sync timing signals on the video outputs. The blanking pedestal ensures that no visible trace appears on the screen during flyback. Both of these pedestals can be set to zero by Control Register A.

Figure 13.31 shows the DAC output levels; the DAC characteristics being given in Table 13.43.

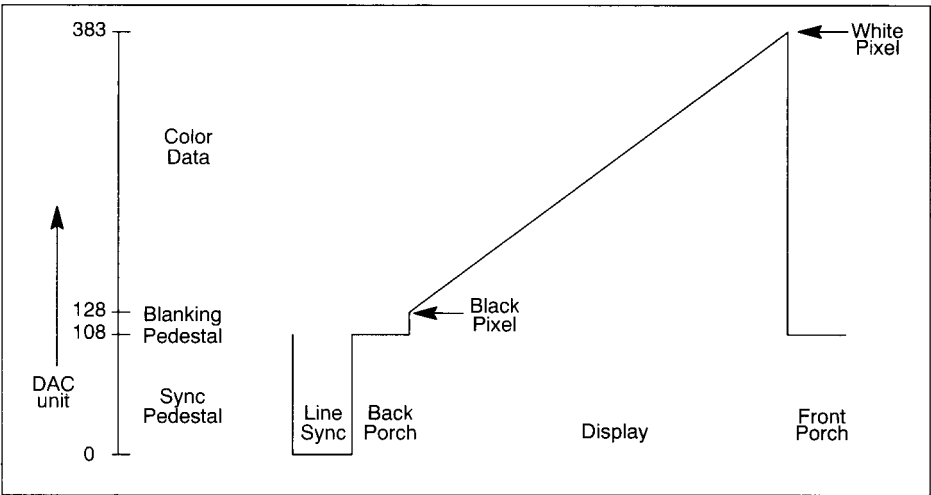


Figure 13.31 DAC output levels

13.12.1 DAC comparators

A voltage comparator is attached to the output of each DAC. Their purpose is to provide an automatic test capability for the analogue outputs. The state of all comparator outputs is sampled and stored by writing a 1 to Control Register B, bit 7. Their state then be read back from bits 4-6 of that register.

Register bit = High when DAC level > reference level.

There are two options for comparator reference levels:

- 1 For all three DACs, there is an internal fixed reference level.
- 2 For the blue and red DACs there is the option of using the output of the Green DAC as the reference, selected by Control Register A bit 19.

Using DAC comparators

The fixed internal reference can be used for coarse checking of the voltage levels at the DAC outputs. For instance, if the DAC voltage is less than reference, and the comparison returns a 1, then a system fault such as disconnected or broken monitor lead can be implied. The comparison with another DAC output can be used for more sophisticated checking such as board level debugging without requiring a monitor to be connected.

13.13 Register reference guide

13.13.1 Timing Generator and Framestore Manager maps

Register	Word address (hex)	Units	Notes
Screen description registers			
HalfSync	021	Screen Units	1
BackPorch	022	Screen Units	
Display	023	Screen Units	
ShortDisplay	024	Screen Units	
BroadPulse	025	Screen Units	
VSync	026	Half lines	
VPreEqualize	027	Half lines	
VPostEqualize	028	Half lines	
VBlank	029	Half lines	
VDisplay	02A	Half lines	
LineTime	02B	Screen Units	
Top of Screen #1			
LineStart	02C	Screen Units	
Framestore description registers			
MemInit	02D	Screen Units	
TransferDelay	02E	Screen Units	2
Notes			
1 For all pixel depths except 24 bpp: 1 Screen Unit = 4 pixels horizontally = 1 Serial Clock period In 24 bpp non-interleaved mode: 1 Screen Unit = 1 pixel horizontally In 24 bpp interleaved mode: 1 Screen Unit = 2 pixels horizontally			
2 Note that TransferDelay is a constant time (determined by the system) rather than a constant number of pixels. Thus changes in pixel rate will mean changing TransferDelay to compensate.			

Table 13.21 VTG register allocation

Timing generator and Framestore manager reset behavior

On reset, the Timing generator and Framestore manager will be set to their inactive state. The register contents are unchanged by reset and, on the first reset after power-up, are undefined.

13.13.2 The control registers and boot location

Control Register A

Bit	Function	Comments
0	Enable VTG	0 = VTG disabled 1 = VTG enabled
1	Screen format	0 = Non-interlaced 1 = Interlaced
2	Interlace standard	0 = EIA format 1 = CCIR format
3	Operating mode	0 = Master mode 1 = Slave mode
4	Frame flyback pattern	0 = Tesselated sync 1 = Plain sync
5	Digital sync format	0 = Composite sync 1 = Separate sync
6	Analogue video format	0 = Composite video + sync 1 = Video only
7	Blank level	0 = No blank pedestal 1 = Blanking pedestal
8	Blank I/O	0 = CBlank is output 1 = CBlank is input
9	Blank function switch	0 = Delayed CBlank at pad 1 = Undelayed CBlank, at pad
10	Force blanking (irrespective of bit 11)	0 = No Action 1 = Screen blanked
11	Turn off blanking	0 = Blanking enabled 1 = Blanking disabled
12-13	VRAM address increment	See definition (Section 13.7.2, page 187)
14	Turn off transfer cycles	0 = DMA transfer cycles enabled 1 = DMA transfer cycles disabled
15	Pixel pipeline delay	As for bits 16-17
16-17	Pixel pipeline delay	Delays sampling point by 0 - 7 VTG clock cycles (see Section 13.8.5, page 204)
18	Pixel port interleaving	0 = Non-interleaved 1 = Interleaved
19	Comparator reference	0 = Compare DAC with reference 1 = Compare DAC with green DAC
20-22	Bits per pixel	See definition (Section 13.8.1, page 197)
23	Cursor disable	0 = Cursor enabled 1 = Cursor disabled

Table 13.22 Control Register A bit allocations (Address #X060)

Control Register B

This register is at address #X070 and the startup sequence after reset may still include a write #0000 to this address before writing control data. Bits 0 to 15 of Control Register B are used as shown in Table 13.23. Bits 15 to 23 continue to be reserved.

Control Register B bit allocations

Bit	Function	Comments	Note
0	Pixel Sampling mode	0 = Internal 1 = External (see Section 13.8.4)	
1	DAC Sync pedestals	0 = Sync on all DACs 1 = Sync on green only	
2	Flyback waveform.	0 = No Hsync during flyback 1 = Sync during flyback (see Section 13.6.3)	1
3	VRAM SAM style	0 = Synchronous 1 = Split SAM (see Section 13.7.5)	
4–6	DAC comparator bits	READ ONLY 4 = Blue, 5= Green, 6 = Red 0 = Correct operation 1 = Fault. (see Section 13.12.1)	
7	Turn on Comparators	0 = DAC comparators off	
8	Checksum test	0 = Checksum on pixel data 1 = Checksum on zero data	
9	Tristate sync pins	0 = Sync pins active 1 = Sync pins tristate	2
10	notVSync Polarity	0 = notVSync active low 1 = notVSync active high	
11	notCorHSync polarity	0 = notCorHSync active low 1 = notCorHSync active high	
12	Complement cursor	0 = 3 colors + transparency 1 = 2 colors + transparency + complement	3
13	XGA cursor	0 = Ordinary cursor 1 = XGA cursor (see Section 13.9.3)	3
14	Even field interlace	0 = TV standard interlace 1 = Even field interlace (see Section 13.6.4)	4
15–23	reserved, write zero		
<p>Notes:</p> <ol style="list-style-type: none"> Setting bit 2 high overrides the effect of bit 4 of Control Register A, i.e. composite sync in flyback will override the choice of tessellated or plain sync. This bit will reset High. Bits 12 and 13 must both be set to 1 for XGA cursor. Bit 2 of Control Register A must also be set high for Even field interlace. 			

Table 13.23 Control Register B bit allocations (Address #X070)

Control Register A and B reset defaults

On reset, Control Register A is set to zero and in Control Register B all bits **except** bit 9 are set to zero; bit 9 is set to one.



Boot location

Bit	Function	Comments
0-4	PLL multiplier	Binary coded PLL multiplication factor
5	Clock source select	0 = External ($\times 1$) clock 1 = PLL clock
6	Micro port address alignment	0 = 32 bit 1 = 64 bit
7-23	Reserved	Write zero

Table 13.24 Boot location Write bit allocations (Address #X000)

The boot location must be written on power-up and after any reset before attempting to access any other locations from the micro port. The timing of this first cycle may differ from subsequent write cycles; see Table 13.30 and Figure 13.36 (page 220) for the relevant timing parameters.

Boot location readback

The boot location is readable at any time after a configuration (boot) write. The mapping of the boot location read bits is shown in Table 13.25.

Bit	Function	Comments
0-12	Reserved	Invalid on read
13-17	PLL multiplier	Binary coded PLL multiplication factor
18	Clock source select	0 = External ($\times 1$) clock 1 = PLL clock
19	Micro port address alignment	0 = 32 bit 1 = 64 bit
20-23	Reserved	Invalid on read

Table 13.25 Boot location Read bit allocation (Address #X000)

Boot location reset defaults

On reset, the boot location register value is set to zero, (i.e. $\times 1$ clock, 32-bit word alignment).

13.14 Timing reference guide

13.14.1 Micro port timing

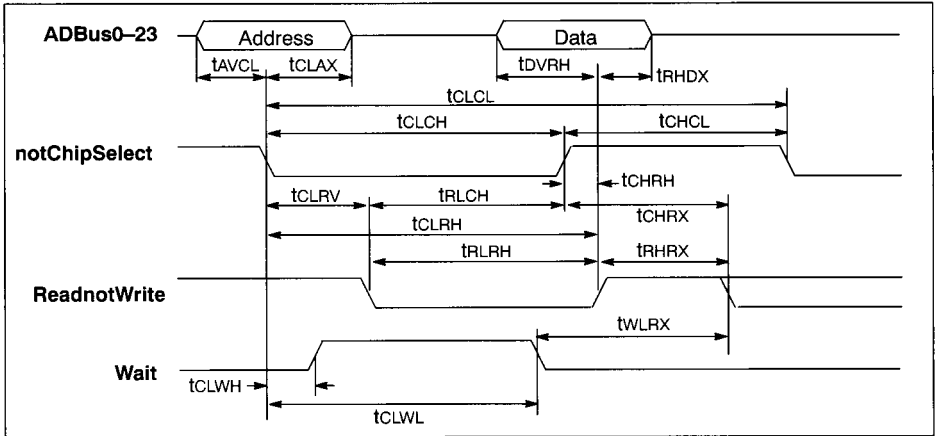


Figure 13.32 Micro port write cycle

Symbol	Description	Min.	Max.	Unit	Notes
tAVCL	Address setup time	10		ns	
tCLAX	Address hold time	10		ns	
tCLRVR	ReadnotWrite setup time		1 SCIk-10	ns	1
tCLRCH	ReadnotWrite low to notChipSelect high	10		ns	
tCLRHR	ReadnotWrite hold time	20		ns	
tRLRH	ReadnotWrite low time	20		ns	
tRHRX	ReadnotWrite high to ReadnotWrite invalid	2SCIk+10		ns	
tWLRX	Wait low to ReadnotWrite invalid	0			
tDVRH	Write data setup time	10		ns	
tRHDX	Write data hold time	10		ns	
tCLCL	Cycle time	4 SCIk			
tCLWH	notChipSelect low to Wait high	0	20	ns	
tCLWL	notChipSelect low to Wait low	2 SCIk	3 SCIk+10	ns	2
tCHRHR	notChipSelect high to ReadnotWrite high		1 SCIk-5	ns	
tCLCH	notChipSelect low time	20		ns	
tCHCL	notChipSelect high time	2SCIk+10		ns	
tCHRHR	notChipSelect high, ReadnotWrite invalid	0		ns	

Note: These parameters are not characterized and are subject to change

Notes:

- 1 This condition will be satisfied if EITHER there has been a valid write pulse before this point OR the **ReadnotWrite** signal is low at this point.
- 2 The meaning of the **Wait** signal is changed to define the earliest point at which a new **notChipSelect** access can begin. It can still be interpreted in the same way as the IMS G332 to indicate that data may now be strobed into the device but this will have an impact on speed.

Table 13.26 Micro port write cycle parameters

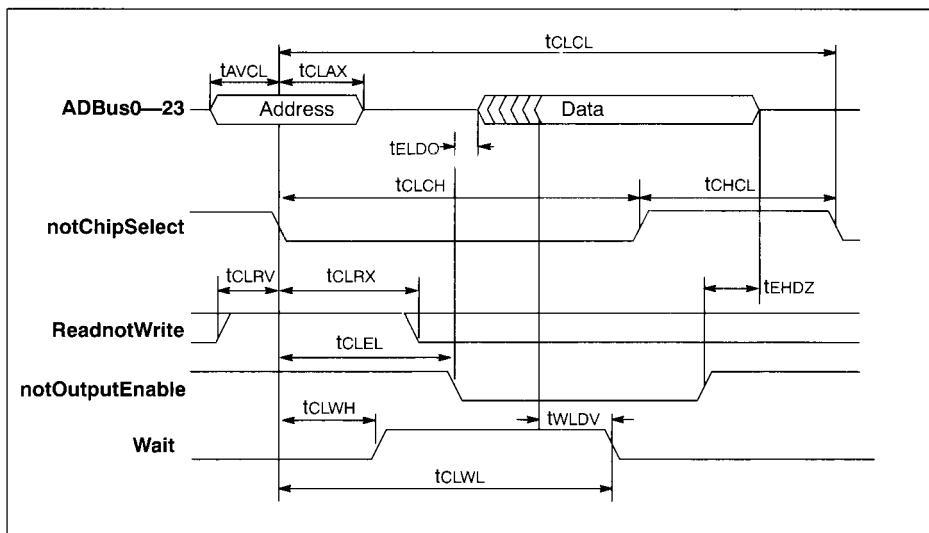


Figure 13.33 Micro port read cycle

Symbol	Description	Min.	Max.	Unit	Notes
tAVCL	Address setup time	10		ns	
tCLAX	Address hold time	10		ns	
tCLRv	ReadnotWrite setup time		-10	ns	
tELDQ	Output turn on delay		20	ns	
tEHDZ	Output hold time from notOutputEnable	5	20	ns	
tCLCL	Cycle time	7 SCIk			
tCLEL	notChipSelect low to notOutputEnable	tCLAX			1
tCLWH	notChipSelect low to Wait high	0	20	ns	
tCLWL	notChipSelect low to Wait low	3.5 SCIk	4.5 SCIk+30	ns	2
tCLRv	notChipSelect low to Readnot-Write invalid	2 SCIk		ns	
tWLDV	Data valid to Wait low		0	ns	
tCLCH	notChipSelect low time	20		ns	
tCHCL	notChipSelect high time	2 SCIk + 20		ns	
Note: These parameters are not characterized and are subject to change					
Notes					
1 To avoid bus contention, notOutputEnable must not be driven low while address is valid.					
2 The meaning of Wait in a read cycle is unchanged with respect to the IMS G332.					

Table 13.27 Micro port read cycle parameters

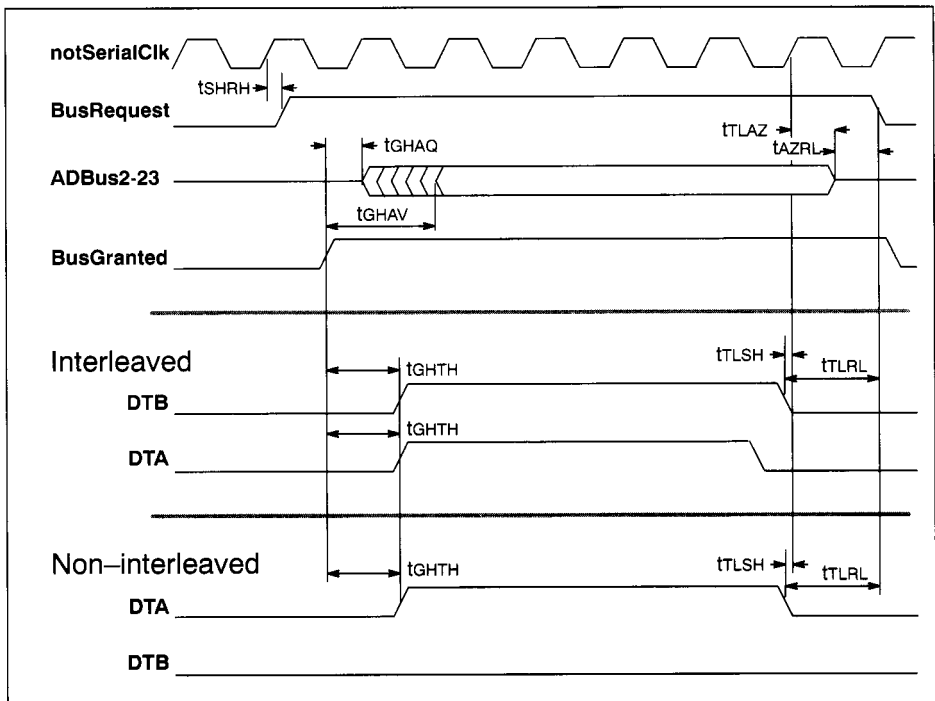


Figure 13.34 Micro port DMA and transfer timings

Symbol	Description	Min.	Max.	Unit
tSHRH	notSerialClk to BusRequest skew	-5	5	ns
tGHTH	BusGranted high to DTA/B high	0	30	ns
tGHAQ	Transfer address turn on delay	5		ns
tGHAV	Transfer address access time		35	ns
tTSLH	DTA/B to notSerialClk skew	-5	5	ns
tTLRL	DTA/B to BusRequest low	1	1 + 15ns	periods SCIk
tTLAZ	Transfer address hold time	0	1	periods SCIk
tRLCL	BusRequest low to Chipselect low	20		ns
tAZRL	Address hi-Z to BusRequest low	0		ns

Note: These parameters are not characterized and are subject to change

Table 13.28 Micro port DMA and transfer timing parameters

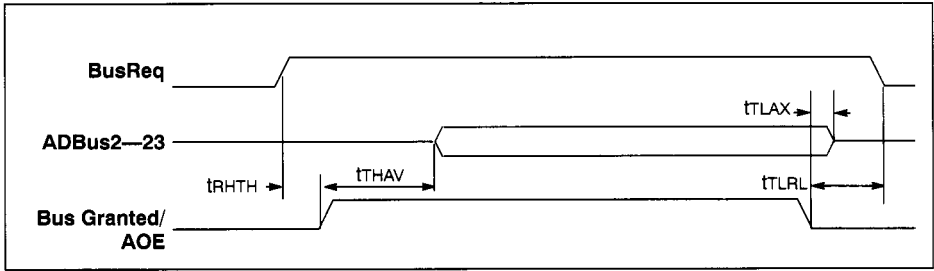


Figure 13.35 Split SAM transfer timing diagram

Symbol	Description	Min	Max	Units	Notes
tRHTH	BusReq to BusGranted/AOE holdoff	0		ns	
tTHAV	Output turn-on time from BusGranted/AOE		35	ns	
tTLAX	Output turn-off time from BusGranted/AOE	0	15	ns	1
tTLRL	BusReq turn-off time from BusGranted/AOE	$\frac{1}{4}SClk + 15$	$1\frac{1}{4}SClk + 15$	ns	2

Note: These parameters are not characterized and are subject to change

Notes:

- 1 For low frequency applications, when BusGranted/AOE pulse width is $< 1\frac{3}{4}SClk$, tTLAX max will be $((1\frac{3}{4}SClk - AOE \text{ pulse width}) + 15ns)$.
- 2 For low frequency applications, when BusGranted/AOE pulse width is $< 1\frac{3}{4}SClk$, tTLRL max will be $((1\frac{3}{4}SClk - AOE \text{ pulse width}) + 1\frac{1}{4}SClk + 15ns)$.

Table 13.29 Split SAM transfer parameters.

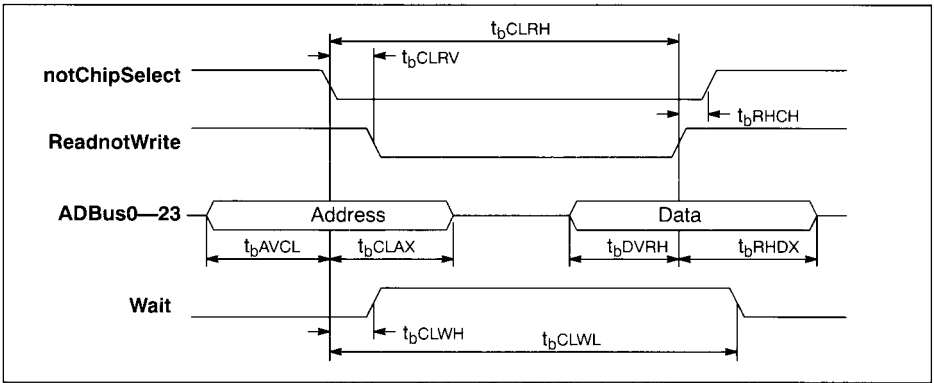


Figure 13.36 Boot write cycle

Symbol	Description	Min.	Max.	Unit
t_{bAVCL}	Address setup time	20		ns
t_{bCLAX}	Address hold time	10		ns
t_{bCLRV}	ReadnotWrite setup time		20	ns
t_{bCLRH}	ReadnotWrite hold time	50		ns
t_{bDVRH}	Write data setup time	20		ns
t_{bRHDX}	Write data hold time	10		ns
t_{bCLWH}	notChipSelect low to wait high	0		ns
t_{bCLWL}	notChipSelect low to wait low		3 +30ns	periods SClk
t_{bRHCH}	ReadnotWrite high to notChipSelect high	0		ns

Note: These figures are not characterized and are subject to change

Table 13.30 Boot write cycle parameters

13.14.2 Pipeline delays

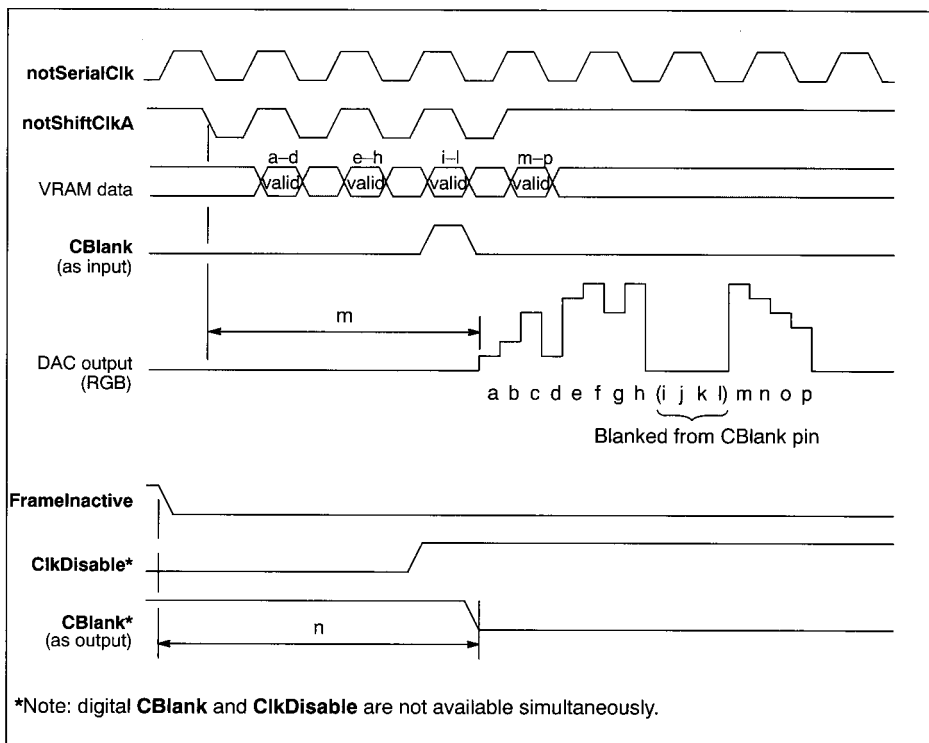


Figure 13.37 Relationship between **notShiftClk**, **Framelnactive**, **CBlank** and **ClkDisable** (8 bpp mode, non-interleaved)

$m = (2.25SClk + d + \text{notShiftClk period})$ SCiKs for all sampling modes

$n = (2.75SClk + d + \text{notShiftClk period})$ SCiKs for all sampling modes

where $d =$ binary decode of Control Register A bits 15 to 17

Note: Diagram shows delay with Control bits 9 to 11 = 0

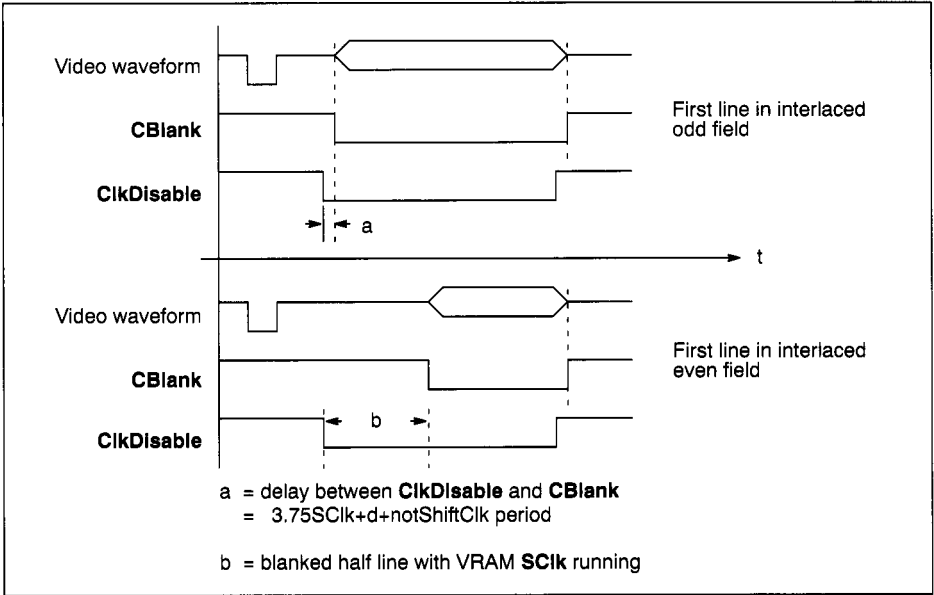


Figure 13.38 Relationship between Video, **CBlank** and **ClkDisable**

13.14.3 Reset timing

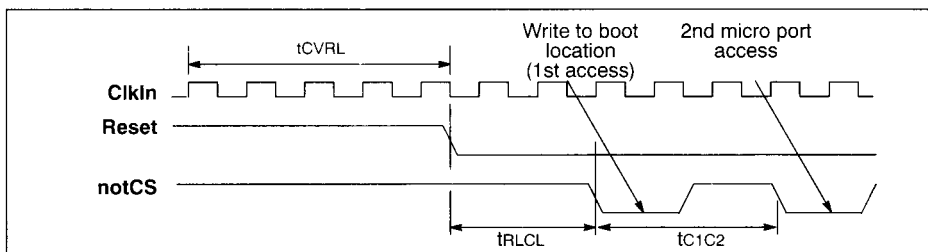


Figure 13.39 Reset timings

Symbol	Description	Min.	Max.	Unit
tRLCL	Reset low to notCS low	100		ns
tCVRL	ClkIn valid to reset low	6		periods Clockin
tC1C2	Time between 1st and 2nd access	80		μs
Note: These parameters are not characterized and are subject to change				

Table 13.31 Reset timing parameters

13.14.4 Video Timing Generator startup delay

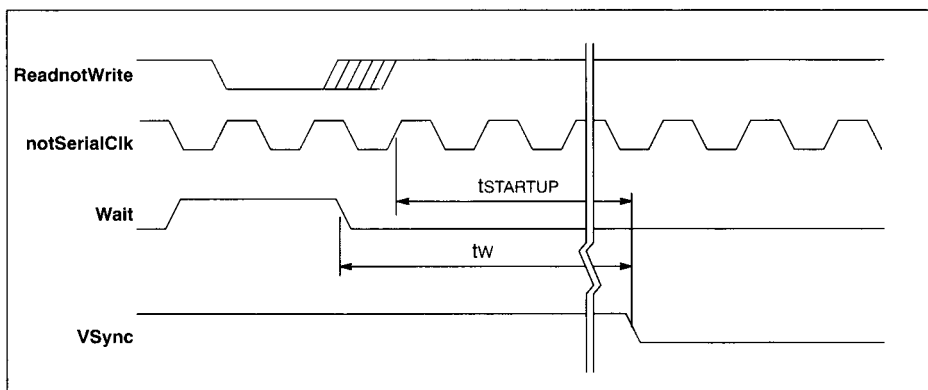


Figure 13.40 Video Timing Generator startup delay

Symbol	Description	Min. ¹	Max. ¹	Unit
tw	Delay from the falling edge of Wait			SClk
tSTARTUP	Pipeline delay from the first rising edge of notSerialClk following the rising edge of ReadnotWrite	$5^{1/2} + d + \text{notShiftClk}$	$6^{1/4} + d + \text{notShiftClk}$	SClk
Note: These parameters are not characterized and are subject to change				
Notes:				
1 d = binary decode of Control Register A, bits 15 to 17				

Table 13.32 Video Timing Generator startup delay parameters

13.14.5 Clock and control signal skew timings

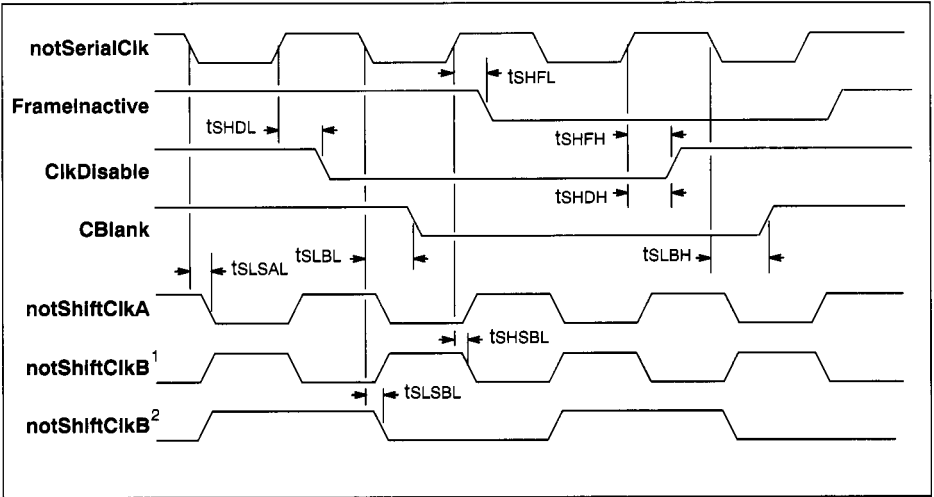


Figure 13.41 Clock and control signal skew timings

Symbol	Description	Min.	Max.	Unit	Notes
tSHFL	notSerialCik to FrameInactive lo skew	0	10	ns	
tSHFH	notSerialCik to FrameInactive hi skew	0	10	ns	
tSHDL	notSerialCik to CikDisable lo skew	0	10	ns	
tSHDH	notSerialCik to CikDisable hi skew	-5	5	ns	
tSLBL	notSerialCik to CBlank lo skew	$\frac{1}{4}SCik-5$	$\frac{1}{4}SCik+5$	ns	
tSLBH	notSerialCik to CBlank hi skew	$\frac{1}{4}SCik-5$	$\frac{1}{4}SCik+5$	ns	
tSLSAL	notSerialCik low to notShiftCikA falling edge skew	-3	3	ns	
tSHSBL	notSerialCik high to notShiftCikB falling edge skew	-3	3	ns	1
tSLSBL	notSerialCik low to notShiftCikB falling edge skew	-3	3	ns	2

Note: These parameters are not characterized and are subject to change

Notes:

- 1 Applies to 24/16/15bpp interleaved only
- 2 Applies to all other interleaved modes

Table 13.33 Clock and control signal skew parameters

13.14.6 Pixel port timing

Internal sampling

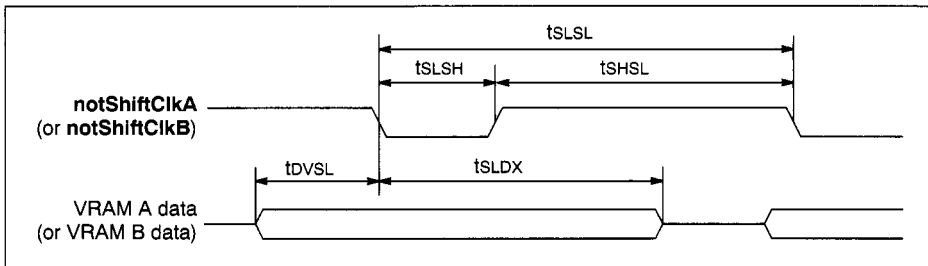


Figure 13.42 Pixel port timing diagram (internal mode)

Symbol	Description	-85 min	-100 min	-110 min	-135 ¹ min	Unit
tSLSL	notShiftCkA period	47	40	36	29	ns
tSLSH	notShiftCkA low time	10	10	10	10	ns
tSHSL	notShiftCkA high time	10	10	10	10	ns
tDVSL	Data set up time	1	1	1		ns
tSLDX	Data hold time	9	9	9		ns

Note: These parameters are not characterized and are subject to change

Note:
1 Internal sampling is not recommended at this frequency

Table 13.34 Pixel port timing parameters (internal mode)

External sampling

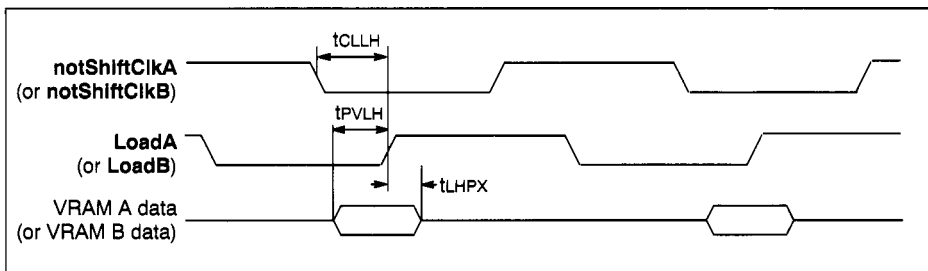


Figure 13.43 Pixel port timing diagram (external mode)

Symbol	Description	Min	Max	Unit
tPVLH	Data set up time	2.5		ns
tLHPX	Data hold time	2.5		ns
tCLLH	notShiftCkA to LoadA high skew	0	7.5	ns

Note: These parameters are not characterized and are subject to change

Table 13.35 Pixel port timing parameters (external mode)

13.14.7 CBlank as input sampling

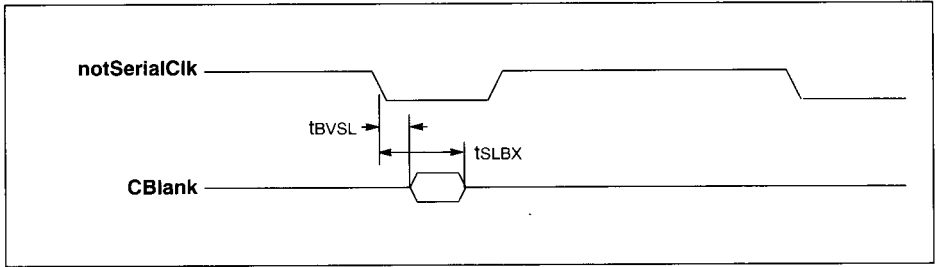


Figure 13.44 Pixel port timing diagram (internal mode)

Symbol	Description	Min	Unit
tBVSL	CBlank set up time	$-1/4\text{SClk}+5$	ns
tSLBX	CBlank hold time	$1/4\text{SClk}+5$	ns
Note: These parameters are not characterized and are subject to change			
Note: 1 These timings apply to both external and internal sampling modes			

Table 13.36 Pixel port timing parameters (sampling with **CBlank** as input)

13.14.8 External synchronization (Slave mode) timing

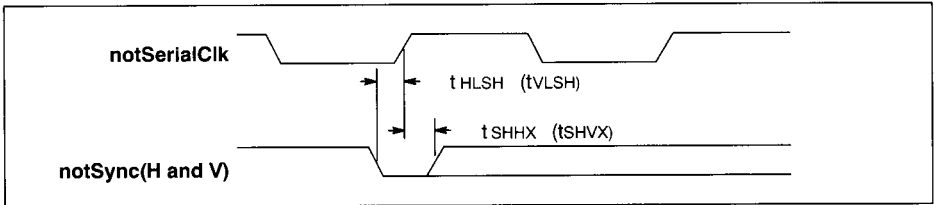


Figure 13.45 External synchronization

Symbol	Description	Min.	Max.	Unit
tVLSH	notVsync setup time	0.25 +5ns	0.75	periods SCIk
tHLSH	notHsync setup time	0.25 +5ns	0.75	periods SCIk
tSHVX	notVsync hold time	0		ns
tSHHX	notHsync hold time	0		ns
Note: These parameters are not characterized and are subject to change				

Table 13.37 External synchronization parameters

13.14.9 Clock timing

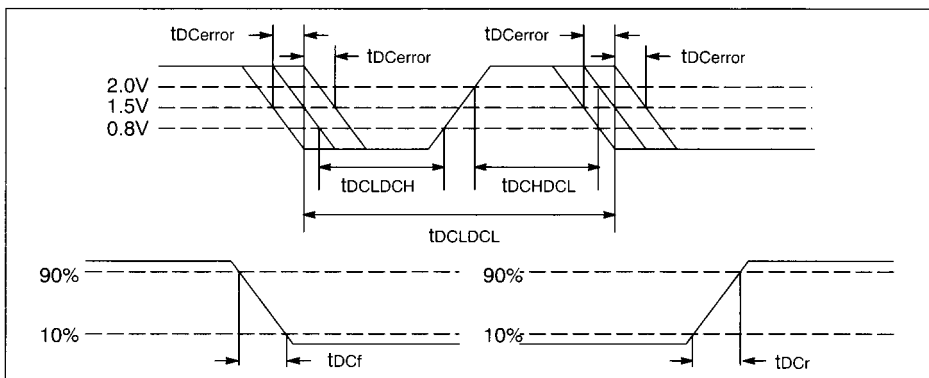


Figure 13.46 ClockIn timing

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
t_{DCLDCH}	ClockIn pulse width low	20			ns	
t_{DCHDCL}	ClockIn pulse width high	20			ns	
t_{DCLDCL}	ClockIn period	100		200	ns	1
$t_{DCError}$	ClockIn timing error			± 0.015	%	2
t_{DCr}	ClockIn rise time			10	ns	3
t_{DCf}	ClockIn fall time			8	ns	3

Notes

- 1 Measured between corresponding points on consecutive falling edges.
- 2 Variation of individual falling edges from their normal times.
- 3 Clock transitions must be monotonic within the range **VIH** to **VIL**.

Note: These parameters are not characterized and are subject to change

Table 13.38 ClockIn timings in PLL mode

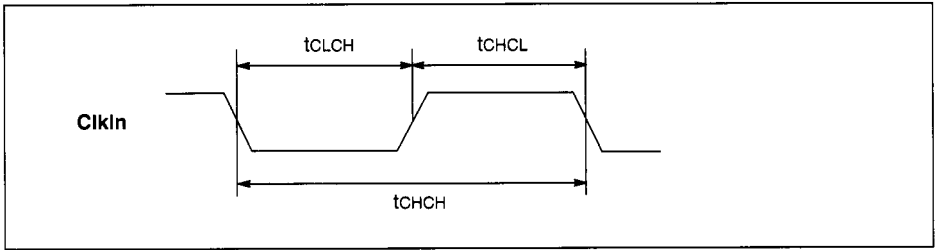


Figure 13.47 'Times 1' mode timing

Symbol	Description	Min.				Max.	Unit
		85MHz	100MHz	110MHz	135MHz ¹		
tCHCH	Cycle time	20	15.1	11.7		200	ns
tCHCL	Clock high time	5	5	5			ns
tCLCH	Clock low time	5	5	5			ns

Note: These parameters are not characterized and are subject to change

Note:

1 Operation at 135MHz is not recommended in x1 mode

Table 13.39 'Times 1' mode Clkin timings

13.15 General parametric conditions and characteristics

13.15.1 Absolute Maximum ratings*

Symbol	Parameter	Min.	Max.	Units	Notes
AVDD/VDD	DC Supply Voltage		7	Volts	
	Voltage on other pins	VSS-1	VDD+0.5	Volts	
TS	Storage temperature (ambient)	-65	150	°C	
TA	Temperature under bias	-40	85	°C	
Iref	Reference current		15	mA	
	Analogue O/P current		45	mA	1
	DC Digital O/P current		25	mA	
Note: These figures are not characterized and are subject to change					
Notes					
1 Per output					

Table 13.40 Absolute Maximum ratings

*Note

Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

13.15.2 Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts	1
GND	Ground		0		Volts	
VIH	Input Logic '1' Voltage	2.0		VDD+0.5	Volts	
VIL	Input Logic '0' Voltage	-0.5		0.8	Volts	
TCQFP	Case Temperature	TBD		TBD	°C	2
Note: These figures are not characterized and are subject to change						
Notes						
1 AVDD = VDD						
2 Measured on the lid of the package at maximum power dissipation.						

Table 13.41 Operating conditions

13.15.3 Operating characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
IDD	Power Supply Current (85MHz)		260	305	mA	1
IDD	Power Supply Current (100MHz)		280	325	mA	1
IDD	Power Supply Current (110MHz)		290	335	mA	1
IDD	Power Supply Current (135MHz)		315	360	mA	1
IIN	Digital Input Current			±10	µA	
IOZ	TriState Dig Output Current			±50	µA	
VOH	Output Logic '1' Voltage	2.4			Volts	
IOH	Output Logic '1' Current	-5			mA	
VOL	Output Logic '0' Voltage			0.4	Volts	
IOL	Output Logic '0' Current	5			mA	
Note: These figures are not characterized and are subject to change						
Notes						
1 Figures shown are for the indicated clock rates (see Section 12.3, Ordering information)						

Table 13.42 Operating characteristics

13.15.4 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
	Resolution	8	8	8	bits	
VO(max)	Output voltage			1.5	Volts	2
IO(max)	Output current			34	mA	VO≤1V
	Full scale error			± 5	%	2, 3
	Sync pedestal error			±10	%	2
	Blank level pedestal error			±10	%	2
	DAC to DAC correlation error			± 2.5	%	2, 4
	Integral Linearity error			± 1	LSB	2, 5, 6
	Differential Linearity error			± 1	LSB	2, 6
	Glitch Energy		75		pVSec	7
Iref	Reference current	7		10	mA	
Vref	Voltage on Iref pin	VDD-3V		VDD	Volts	
Note: These figures are not characterized and are subject to change						
Notes						
1 All voltages with respect to GND unless specified otherwise.						
2 Tested over the operating temperature range and at nominal supply voltage with Iref = -8.88mA.						
3 From the value predicted by the design equation, sync and blank level pedestals off.						
4 About the mid point of the distribution of the 3 DACs measured at full scale deflection.						
5 Linearity measured from the best fit line through the DAC characteristic.						
6 Monotonicity guaranteed. Load = 37.5Ω +30 pF with Iref = -8.88mA.						
7 This parameter is sampled not 100% tested.						

Table 13.43 DAC characteristics

13.15.5 Output drive capability

Parameter	Min.	Max.	Units	Notes
notShiftClkA		25	pF	1
notShiftClkB		25	pF	1
notSerialClk		25	pF	1
DTA		25	pF	
DTB		25	pF	
ADBus [0..23]		25	pF	
Notes				
1 These loadings must be strictly adhered to in order to avoid a degradation in picture quality.				

Table 13.44 Output drive capability

13.16 Package specifications

100 pin plastic quad flatpack package

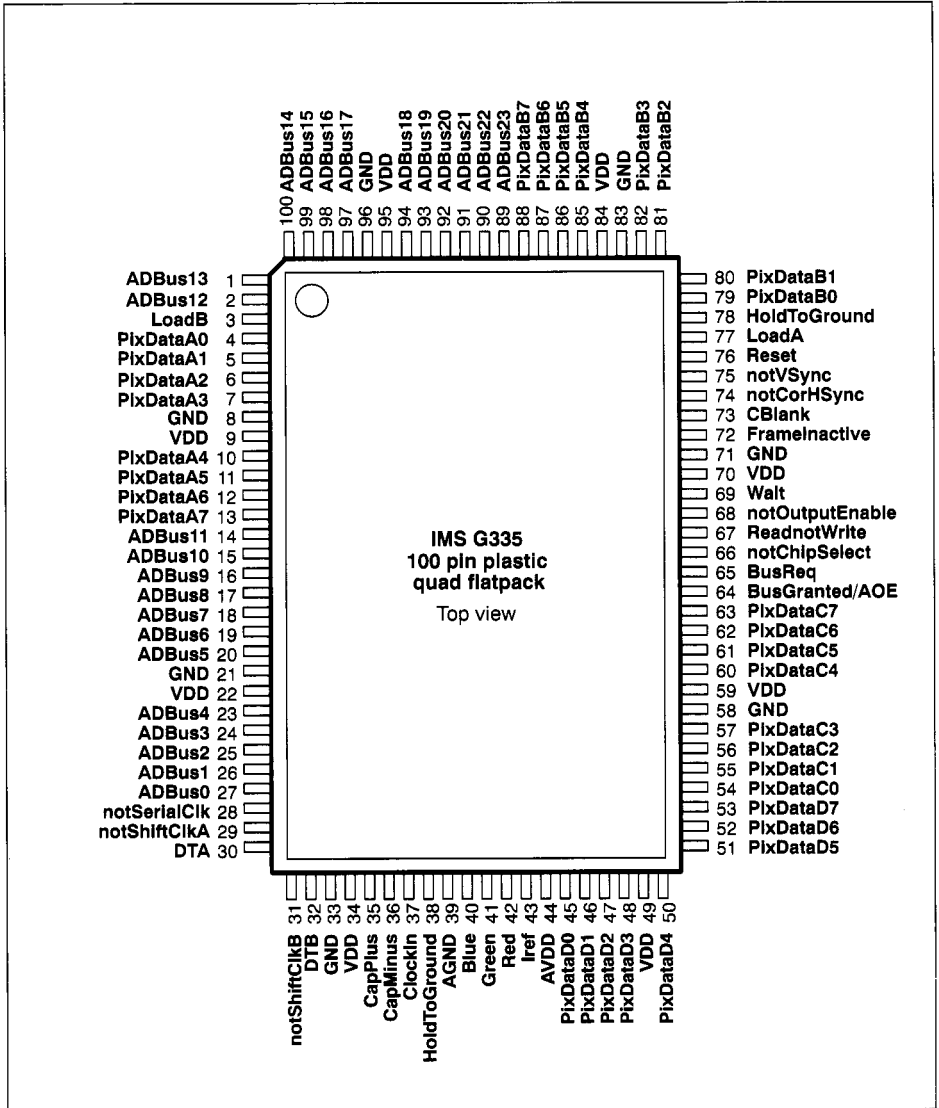
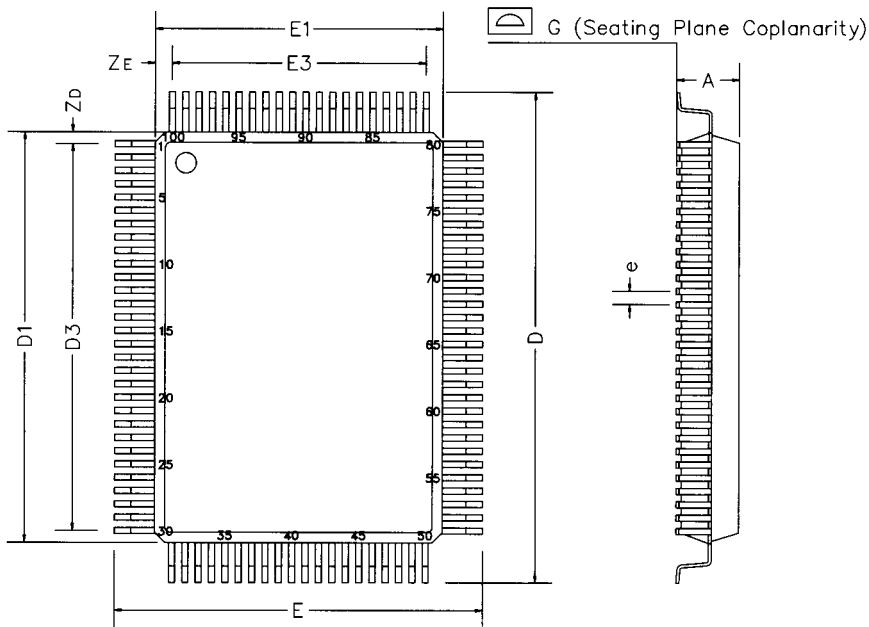
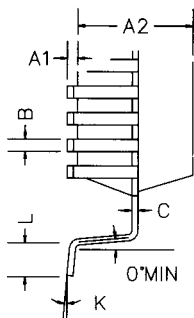


Figure 13.48 IMS G335 100 pin plastic quad flatpack package pinout

DIM	CONTROL DIMENSIONS mm			ALTERNATIVE DIMENSIONS INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	3.400	—	—	0.134
A1	0.100	—	0.360	0.004	—	0.014
A2	2.450	2.800	3.050	0.096	0.110	0.120
B	0.220	—	0.380	0.009	—	0.15
C	0.130	—	0.230	0.005	—	0.009
D	22.950	—	24.150	0.904	—	0.951
D1	19.900	20.000	20.100	0.783	0.787	0.791
D3	—	18.850REF	—	—	0.742REF	—
E	16.950	—	18.150	0.667	—	0.715
E1	13.900	14.000	14.100	0.547	0.551	0.555
E3	—	12.350REF	—	—	0.486REF	—
e	—	0.650BSC	—	—	0.026BSC	—
G	—	—	0.100	—	—	0.004
K	0°	—	7°	0°	—	7°
L	0.650	0.800	0.950	0.026	0.031	0.037
Zd	—	0.580REF	—	—	0.023REF	—
ZE	—	0.830REF	—	—	0.033REF	—



Notes;

1. Maximum lead displacement from notional centre line = $\pm 0.125\text{mm}$.

Figure 13.49 100 pin plastic quad flat pack dimensions

13.17 Ordering information

Device	Clock rate	Package	Part number
IMS G335	85 MHz	100 pin plastic quad flatpack	IMS G335X-85S
IMS G335	110 MHz	100 pin plastic quad flatpack	IMS G335X-11S
IMS G335	135 MHz	100 pin plastic quad flatpack	IMS G335X-13S