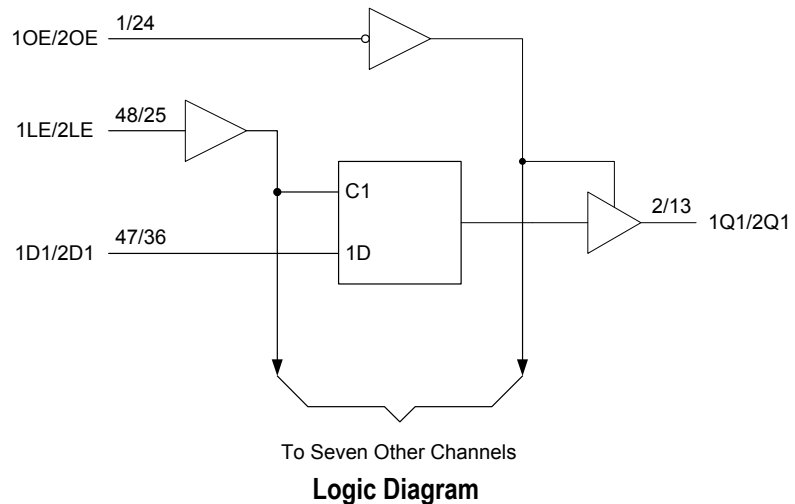
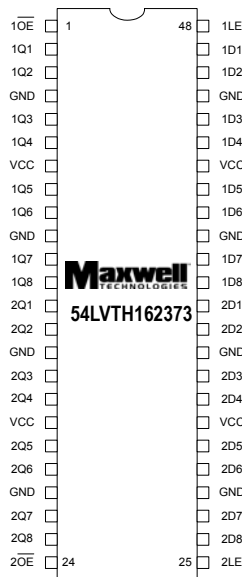


# 54LVTH162373

## 3.3V 16-Bit Transparent D-Type Latches



### FEATURES:

- 3.3V low voltage advanced BiCMOS technology (LVT) 16-bit transparent D-type latches with 3-state outputs
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Excellent Single Event Effect:
  - $SEL_{TH}$ : No LU > 119 MeV/mg/cm<sup>2</sup>
- Package: 48 pin RAD-PAK® flat package
- Operating temperature range:
  - 55 to 125°C
- Distributed  $V_{CC}$  and GND pin configuration minimizes high-speed switching noise
- Supports mixed-mode signal operation
  - 5V input and output voltages with 3.3V  $V_{CC}$
- Supports unregulated battery operation down to 2.7V
- Supports live insertion
- Bus-hold data inputs eliminate the need for external pullup resistors

### DESCRIPTION:

Maxwell Technologies' 54LVTH162373 16-bit transparent D-type latches with 3-state output features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. The 54LVTH162373 is designed for low voltage (3.3V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5V system environment. It is suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The 54LVTH162373 can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is low, the Q output are latched at the levels set up at the data (D) inputs. When LE is high, the Q outputs follow the D inputs. A buffered output-enable (OE) input can be used to place the eight outputs in either a normal logic state or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and the increased drive provide the capability to drive bus lines without the need for interface or pullup components. OE does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high impedance state.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

TABLE 1. PINOUT DESCRIPTION

| PIN                                       | SYMBOL               | DESCRIPTION   |
|---|----------------------|---------------|
| 1, 24                                     | $\overline{1OE-2OE}$ | Output Enable |
| 2, 3, 5, 6, 8, 9, 11, 12                  | 1Q1-1Q8              | Outputs       |
| 4, 10, 15, 21, 28, 34, 39, 45             | GND                  | Ground        |
| 7, 31, 42                                 | V <sub>CC</sub>      | Power Supply  |
| 13, 14, 16, 17, 19, 20, 22, 23            | 2Q1-2Q8              | Outputs       |
| 25, 48                                    | 2LE-1LE              | Latch Enable  |
| 26, 27, 29, 30, 32, 31, 32,<br>33, 35, 36 | 2D8-2D1              | Inputs        |
| 37, 38, 40, 41, 43, 44, 46, 47            | 1D8-1D1              | Inputs        |

TABLE 2. 54LVTH162373 ABSOLUTE MAXIMUM RATINGS

| PARAMETER   | SYMBOL          | MIN  | MAX  | UNIT |
|---|-----------------|------|------|------|
| Supply voltage range  | V <sub>CC</sub> | -0.5 | 4.6  | V    |
| Input voltage range <sup>1</sup>  | V <sub>I</sub>  | -0.5 | 7    | V    |
| Voltage range applied to any output in the high state or power-off state <sup>1</sup> | V <sub>O</sub>  | -0.5 | 7    | V    |
| Current into any output in the low state  | I <sub>O</sub>  | --   | 30   | mA   |
| Current into any output in the high state <sup>2</sup>                                | I <sub>O</sub>  | --   | 30   | mA   |
| Input clamp current (V <sub>I</sub> < 0)  | I <sub>IK</sub> | --   | -50  | mA   |
| Output clamp current (V <sub>O</sub> < 0)   | I <sub>OK</sub> | --   | -50  | mA   |
| Maximum power dissipation at TA = 55°C <sup>3</sup>                                   | P <sub>D</sub>  | --   | 0.85 | mW   |
| Storage temperature range   | T <sub>S</sub>  | -65  | 150  | °C   |

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and V<sub>O</sub> > V<sub>CC</sub>.
3. The maximum package power dissipation is calculated using a junction temperature of 150 °C and a board trace length of 750 mils.

TABLE 3. DELTA LIMITS

| PARAMETER           | VARIATION                          |
|---------------------|------------------------------------|
| I <sub>CC(OL)</sub> | ±10% of specified value in Table 5 |
| I <sub>CC(OH)</sub> | ±10% of specified value in Table 5 |
| I <sub>CC(OD)</sub> | ±10% of specified value in Table 5 |

TABLE 4. 54LVTH162373 RECOMMENDED OPERATING CONDITIONS <sup>1</sup>

| PARAMETER  | SYMBOL              | MIN | MAX | UNIT |
|--|---------------------|-----|-----|------|
| Supply voltage                                       | $V_{CC}$            | 2.7 | 3.6 | V    |
| High-level input voltage                             | $V_{IH}$            | 2   | --  | V    |
| Low-level input voltage                              | $V_{IL}$            | --  | 0.8 | V    |
| Input voltage  | $V_I$               | --  | 5.5 | V    |
| High-level output current                            | $I_{OH}$            | --  | -12 | mA   |
| Low-level output current                             | $I_{OL}$            | --  | 12  | mA   |
| Input transition rise or fall rate (outputs enabled) | $\Delta t/\Delta v$ | --  | 10  | ns/V |
| Operating temperature                                | $T_A$               | -55 | 125 | °C   |

1. Unused control inputs must be held high or low to prevent them from floating.

TABLE 5. 54LVTH162373 DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 3.3V \pm 10\%$ ,  $T_A = -55$  to  $125^\circ\text{C}$ , UNLESS OTHERWISE SPECIFIED)

| PARAMETER                              | SYMBOL               | TEST CONDITIONS   |                         | MIN            | MAX       | UNIT          |               |
|--|----------------------|---|-------------------------|----------------|-----------|---------------|---------------|
| Input Clamp Voltage                    | $V_{IK}$             | $V_{CC} = 2.7$  | $I_I = -18\text{mA}$    | --             | -1.2      | V             |               |
| High-Level Output Voltage              | $V_{OH}$             | $V_{CC} = 3V$   | $I_{OH} = -12\text{mA}$ | 2              | --        | V             |               |
| Low-Level Output Voltage               | $V_{OL}$             | $V_{CC} = 3V$   | $I_{OL} = 12\text{mA}$  | --             | 0.8       | V             |               |
| Input Current                          | $I_I$                | $V_{CC} = 0$ or $3.6V$  | $V_I = 5.5V$            | --             | 10        | $\mu\text{A}$ |               |
|  |                      | $V_{CC} = 3.6V$   | $V_I = V_{CC}$ or GND   | Control inputs | --        |               | $\pm 1$       |
|  |                      | $V_{CC} = 3.6V$   | $V_I = V_{CC}$          | Data Inputs    | --        |               | 1             |
| Hold Current                           | $I_{I(\text{HOLD})}$ | $V_{CC} = 3V$   | $V_I = 0.8V$            | Data Inputs    | 75        | --            | $\mu\text{A}$ |
|  |                      |   | $V_I = 2V$              | Data Inputs    | -75       | --            |               |
| Output Disabled Leakage Current - High | $I_{OZH}$            | $V_{CC} = 3.6V, V_O = 3V$   |                         | --             | 5         | $\mu\text{A}$ |               |
| Output Disabled Leakage Current - Low  | $I_{OZL}$            | $V_{CC} = 3.6V, V_O = 0.5V$   |                         | --             | -5        | $\mu\text{A}$ |               |
| Power Up Current                       | $I_{OZPU}^2$         | $V_{CC} = 0$ to $1.5V, V_O = 0.5V$ to $3V, \overline{OE} = \text{don't care}$ |                         | --             | $\pm 100$ | $\mu\text{A}$ |               |
| Power Down Current                     | $I_{OZPD}^2$         | $V_{CC} = 1.5V$ to $0, V_O = 0.5V$ to $3V, \overline{OE} = \text{don't care}$ |                         | --             | $\pm 100$ | $\mu\text{A}$ |               |

TABLE 5. 54LVTH162373 DC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = 3.3V \pm 10\%, T_A = -55 \text{ to } 125^\circ\text{C}, \text{ UNLESS OTHERWISE SPECIFIED})$ 

| PARAMETER                | SYMBOL            | TEST CONDITIONS   | MIN              | MAX | UNIT |    |
|--------------------------|-------------------|---|------------------|-----|------|----|
| Supply Current           | $I_{CC}$          | $V_{CC} = 3.6V$<br>$I_O = 0$<br>$V_I = V_{CC} \text{ or GND}$                                   | Outputs high     | --  | 0.19 | mA |
|                          |                   |   | Outputs low      | --  | 5    |    |
|                          |                   |   | Outputs disabled | --  | 0.19 |    |
| Delta Supply Current     | $\Delta I_{CC}^1$ | $V_{CC} = 3V \text{ to } 3.6V$ , One input at $V_{CC} - 0.6V$ , Other inputs at $V_{CC}$ or GND | --               | 0.2 | mA   |    |
| Input Capacitance        | $C_I^2$           | $V_I = 3V \text{ or } 0$  | --               | 8   | pF   |    |
| Input Output Capacitance | $C_O^2$           | $V_O = 3V \text{ or } 0$  | --               | 15  | pF   |    |

1. This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.
2. Guaranteed by design.

TABLE 6. 54LVTH162373 AC ELECTRICAL CHARACTERISTICS

 $(V_{CC} = 3.3V \pm 10\%, T_A = -55 \text{ to } 125^\circ\text{C}, \text{ UNLESS OTHERWISE SPECIFIED})$ 

| PARAMETER                              | SYMBOL    | $V_{CC} = 3.3V \pm 0.3V$ |     | $V_{CC} = 2.7V$ |     | UNIT |
|--|-----------|--------------------------|-----|-----------------|-----|------|
|  |           | MIN                      | MAX | MIN             | MAX |      |
| Pulse duration, LE high                | $t_W$     | 3.3                      | --  | 3.0             | --  | ns   |
| Setup time, data before LE $\emptyset$ | $t_{SU}$  | 1.5                      | --  | 0.6             | --  | ns   |
| Hold time, data after LE $\emptyset$   | $t_H$     | 1.8                      | --  | 2               | --  | ns   |
| Propagation Delay Time<br>D to Q       | $t_{PLH}$ | 1.3                      | 5.2 | --              | 6.0 | ns   |
|  | $t_{PHL}$ | 1.4                      | 4.9 | --              | 5.0 |      |
| Propagation Delay Time<br>LE to Q      | $t_{PLH}$ | 2.1                      | 6.0 | --              | 6.5 | ns   |
|  | $t_{PHL}$ | 2.1                      | 5.2 | --              | 4.9 |      |
| Output Enable Time<br>OE to Q          | $t_{PZH}$ | 1.3                      | 8.0 | --              | 7.4 | ns   |
|  | $t_{PZL}$ | 1.3                      | 5.5 | --              | 6.2 |      |
| Output Disable Time<br>OE to Q         | $t_{PHZ}$ | 2.0                      | 6.8 | --              | 6.9 | ns   |
|  | $t_{PLZ}$ | 1.0                      | 7.6 | --              | 6.7 |      |

fp

TABLE 7. FUNCTION TABLE  
(EACH 8-BIT SECTION)

| INPUTS          |    |   | OUTPUT |
|-----------------|----|---|--------|
| $\overline{OE}$ | LE | D | Q      |
| L               | H  | H | H      |
| L               | H  | L | L      |
| L               | L  | X | $Q_0$  |
| H               | X  | X | Z      |

FIGURE 1. LOAD CIRCUIT

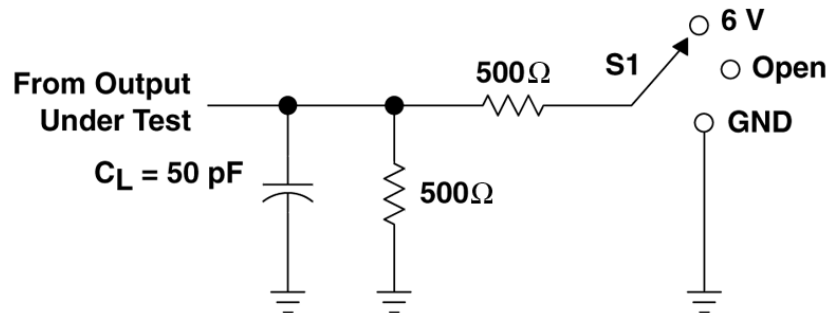


Figure Note:

1.  $C_L$  includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | OPEN |
| $t_{PLZ}/t_{PZL}$ | 6V   |
| $t_{PHZ}/t_{PZH}$ | GND  |

FIGURE 2. PULSE DURATION

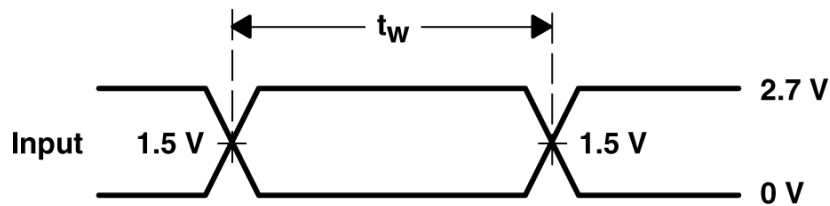


FIGURE 3. SETUP AND HOLD TIMES

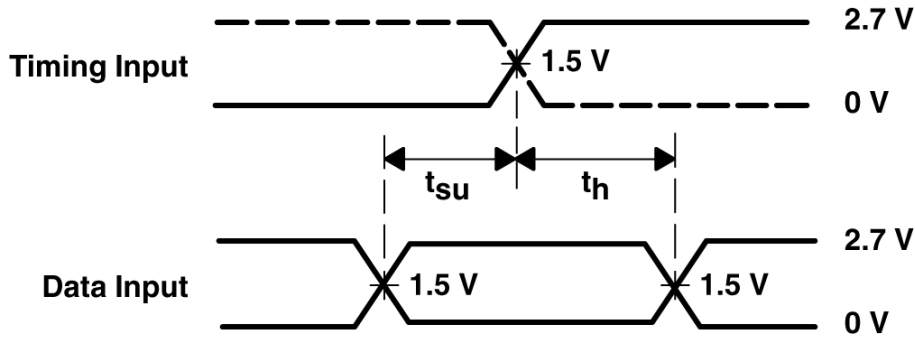


FIGURE 4. PROPAGATION DELAY TIMES INVERTING AND NON-INVERTING OUTPUTS

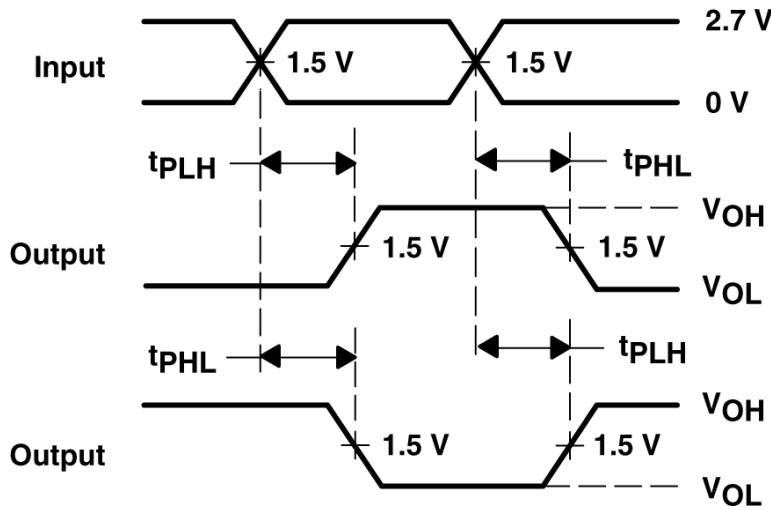
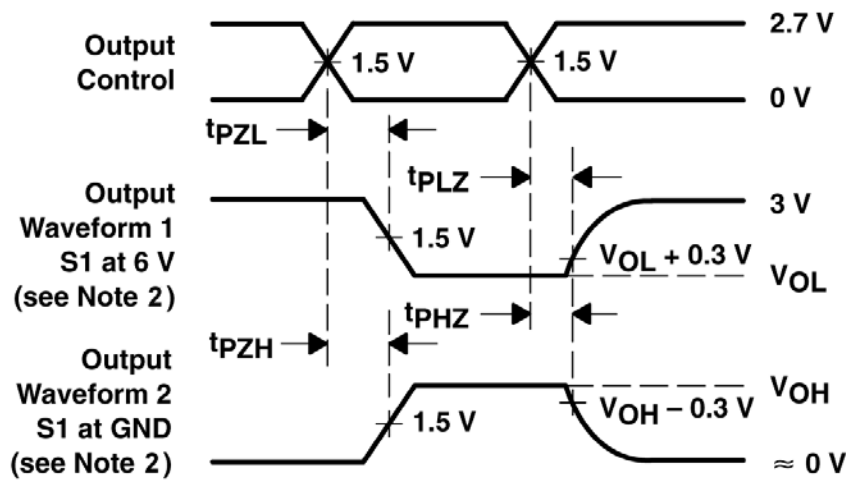
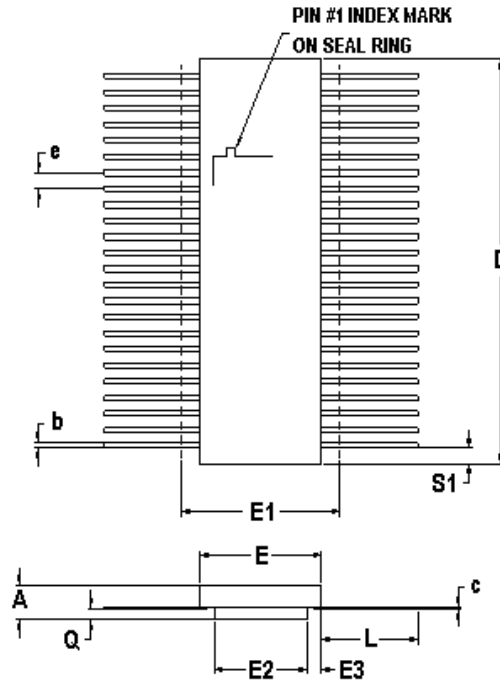


FIGURE 5. ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING



## Figure Notes:

2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $ZO = 5\Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
4. The outputs are measured one at a time with one transition per measurement.



48 PIN RAD-PAK® FLAT PACKAGE

| SYMBOL | DIMENSION |       |       |
|--------|-----------|-------|-------|
|        | MIN       | NOM   | MAX   |
| A      | 0.144     | 0.160 | 0.176 |
| b      | 0.008     | 0.010 | 0.014 |
| c      | 0.004     | 0.006 | 0.007 |
| D      | --        | 0.620 | 0.640 |
| E      | 0.370     | 0.380 | 0.390 |
| E1     | --        | --    | 0.410 |
| E2     | 0.200     | 0.210 | 0.220 |
| E3     | 0.075     | 0.085 | --    |
| e      | 0.025 BSC |       |       |
| L      | 0.275     | 0.285 | 0.295 |
| Q      | 0.013     | 0.019 | 0.045 |
| S1     | 0.005     | 0.018 | --    |
| N      | 48        |       |       |

F48-01

Note: All dimensions in inches



## 3.3V 16-Bit Transparent D-Type

# 54LVTH162373

### Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

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# 3.3V 16-Bit Transparent D-Type

# 54LVTH162373

## Product Ordering Options

