

# OKI Semiconductor

**FEDS82V08520-01**

Issue Date:Feb. 10, 2002

## MS82V08520

**131,072-Word × 32-Bit × 2-Bank SGRAM**

### GENERAL DESCRIPTION

The MS82V08520 is a 8-Mbit system clock synchronous dynamic random access memory.

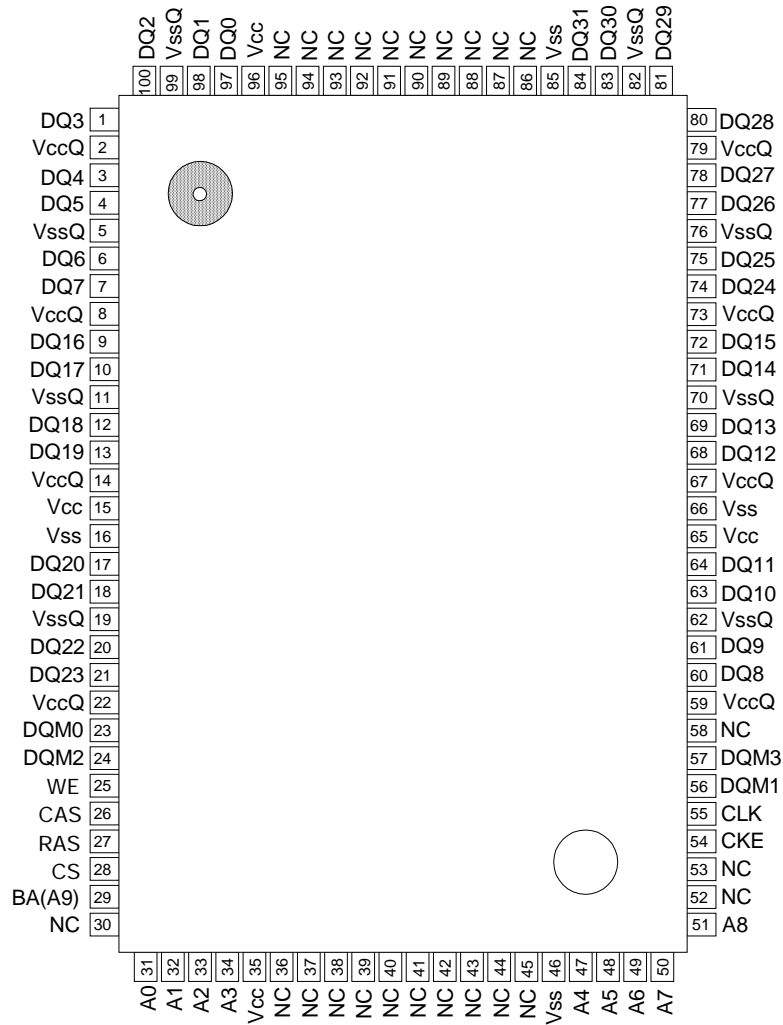
### FEATURES

- 131,072 words × 32 bits × 2 banks memory (512 rows × 256 columns × 32 bits × 2 banks)
- Single 3.3 V ±0.3 V power supply
- LVTTL compatible inputs and outputs
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable CAS latency (2, 3)
- Power Down operation and Clock Suspend operation
- 1,024 refresh cycles/16 ms
- Auto refresh and self refresh capability
- Package:
  - 100-pin plastic QFP (QFP100-P-1420-0.65-BK4) (MS82V08520-xGA)
  - x indicates speed rank.

### PRODUCT FAMILY

Family	Max. Operating Frequency	Access Time	Package
MS82V08520-8	125 MHz	6.5 ns	100-Pin Plastic QFP

**PIN CONFIGURATION (TOP VIEW)**

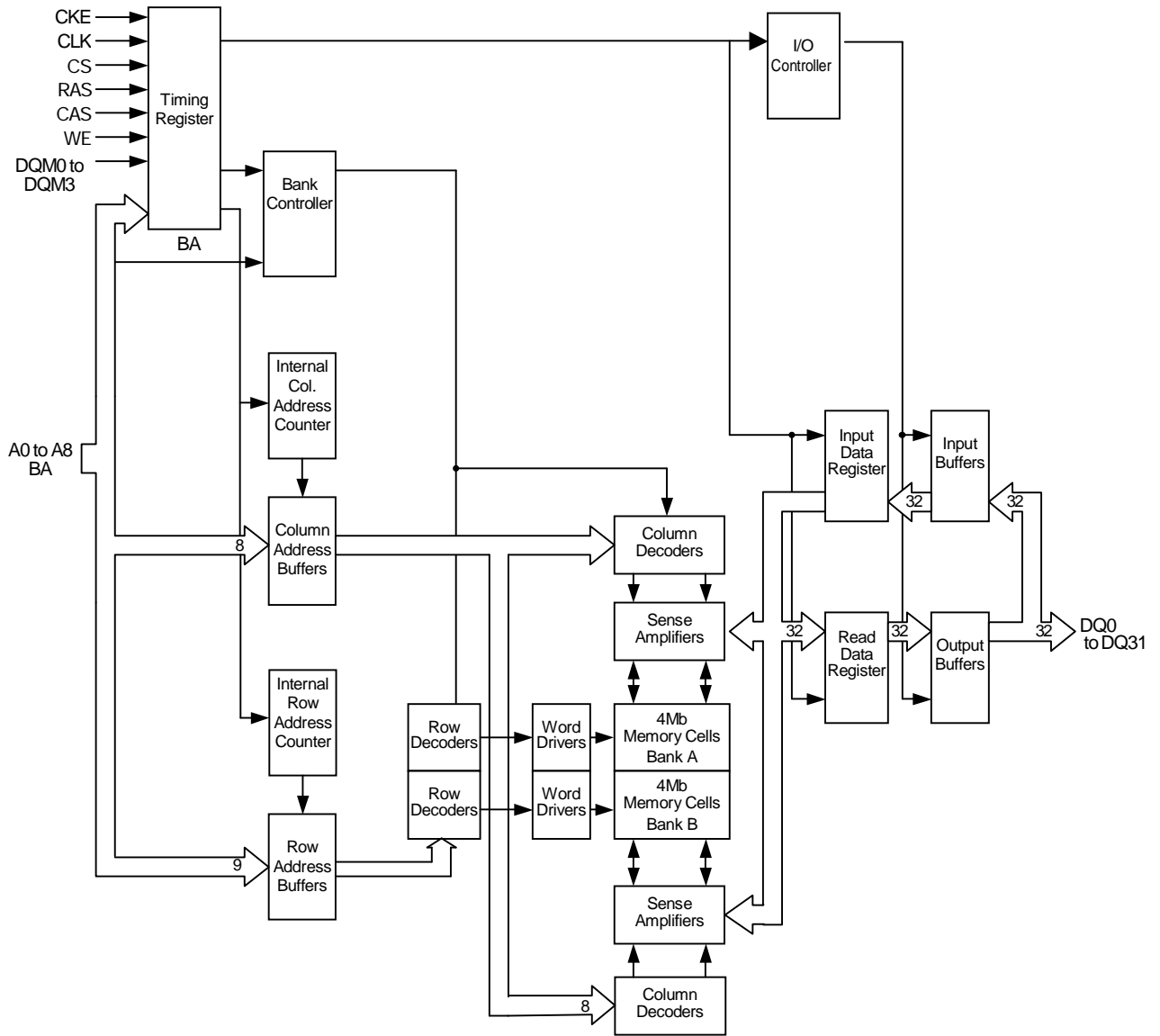


**100-Pin Plastic QFP**

Pin Name	Function	Pin Name	Function
A0 to A8	Row Address Inputs	WE	Write Enable
A0 to A7	Column Address Inputs	DQM0 to DQM3	DQ Mask Enable
BA (A9)	Bank Address	DQ0 to DQ31	Data Inputs/outputs
CLK	System Clock Input	V <sub>CC</sub>	Supply Voltage
CKE	Clock Enable	V <sub>SS</sub>	Ground
CS	Chip Select	V <sub>CCQ</sub>	Supply Voltage for DQ
RAS	Row Address Strobe	V <sub>SSQ</sub>	Ground for DQ
CAS	Column Address Strobe	NC	No Connection

Note: The same power supply voltage level must be provided to every V<sub>CC</sub> pin and V<sub>CCQ</sub> pin.  
The same GND voltage level must be provided to every V<sub>SS</sub> pin and V<sub>SSQ</sub> pin.

**BLOCK DIAGRAM**



**PIN DESCRIPTION**

CLK	Fetches all inputs at the "H" edge.
CS	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, DQM0, DQM1, DQM2 and DQM3.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address: RA0 to RA8, Column address: CA0 to CA7
BA	Selects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time. BA = "L": Bank A                      BA = "H": Bank B
RAS CAS WE	Functionality depends on the combination. For details, see the function truth table.
DQM0 to DQM3	Masks the read data of two clocks later when DQM0 to DQM3 are set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when DQM0 to DQM3 are set "H" at the "H" edge of the clock signal. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, and DQM3 controls DQ24 to DQ31.
DQ0 to DQ31	Data inputs/outputs are multiplexed on the same pin.

- \*Notes: 1. When CS is set "High" at a clock transition from "Low" to "High", all inputs except CLK, CKE, DQM0, DQM1, DQM2, and DQM3 are invalid.  
2. When issuing an active, read or write command, the bank is selected by BA.

BA	Active, read or write
0	Bank A
1	Bank B

3. The auto precharge function is enabled or disabled by the A8 input when the read or write command is issued.

A8	BA	Operation
0	0	After the end of burst, bank A holds the active status.
1	0	After the end of burst, bank A is precharged automatically.
0	1	After the end of burst, bank B holds the active status.
1	1	After the end of burst, bank B is precharged automatically.

4. When issuing a precharge command, the bank to be precharged is selected by the A8 and BA inputs.

A8	BA	Operation
0	0	Bank A is precharged.
0	1	Bank B is precharged.
1	×	Both banks are precharged.

**COMMAND OPERATION****Mode Register Set Command (CS, RAS, CAS, WE = “Low”)**

The MS82V08520 has the mode register that defines the operation mode “CAS Latency, Burst Length, Burst Sequence”. The Mode Register Set command should be executed just after the MS82V08520 is powered on. Before entering this command, all banks must be precharged. Next command can be issued after  $t_{RSC}$ .

**Auto Refresh Command (CS, RAS, CAS = “Low”, WE, CKE = “High”)**

The Auto Refresh command performs refresh automatically by the address counter. The refresh operation must be performed 1,024 times within 16 ms and the next command can be issued after  $t_{RC}$  from last Auto Refresh command. Before entering this command, all banks must be precharged.

**Self Refresh Entry/Exit Command (CS, RAS, CAS, CKE = “Low”, WE = “High”)**

The self refresh operation continues after the Self Refresh Entry command is entered, with CKE level left “low”. This operation terminates by making CKE level “high”. The self refresh operation is performed automatically by the internal address counter on the MS82V08520 chip.

In self refresh mode, no external refresh control is required. Before entering self refresh mode, all banks must be precharged. Next command can be issued after  $t_{RC}$ .

**Single Bank Precharge Command (CS, RAS, WE, A8 = “Low”, CAS = “High”)**

The Single Bank Precharge command triggers bank precharge operation. Precharge bank is selected by BA.

**All Bank Precharge Command (CS, RAS, WE = “Low”, CAS, A8 = “High”)**

The All Bank Precharge command triggers precharge of both Bank A and Bank B.

**Bank Active Command (CS, RAS = “Low”, CAS, WE = “High”)**

The Bank Active command activates the bank selected by BA. The Bank Active command corresponds to conventional DRAM's RAS falling operation. Row addresses “A0 to A8 and BA” are strobed.

**Write Command (CS, CAS, WE, A8 = “Low”, RAS = “High”)**

The Write command is required to begin burst write operation. Then burst access initial bit column address is strobed.

**Write with Auto Precharge Command (CS, CAS, WE = “Low”, RAS, A8 = “High”)**

The Write with Auto Precharge command is required to begin burst write operation with automatic precharge after the burst write. Any command that interrupts this operation cannot be issued.

**Read Command (CS, CAS, A8 = “Low”, RAS, WE = “High”)**

The Read command is required to begin burst read operation. Then burst access initial bit column address is strobed.

**Read with Auto Precharge Command (CS, CAS = “Low”, RAS, WE, A8 = “High”)**

The Read with Auto Precharge command is required to begin burst read operation with automatic precharge after the burst read. Any command that interrupts this operation cannot be issued.

**No Operation Command (CS = “Low”, RAS, CAS, WE = “High”)**

The No Operation command does not trigger any operation.

**Device Deselect Command (CS = “High”)**

The Device Deselect command disables the RAS, CAS, WE and Address input. This command does not trigger any operation.

**Data Write/Output Enable Command (DQMi = “Low”)**

The Data Write/Output Enable command enables DQ0 to DQ31 in read or write.

The each DQM0, 1, 2 and 3 corresponds to DQ0 to DQ7, DQ8 to DQ15, DQ16 to DQ23 and DQ24 to DQ31 respectively.

**Data Mask/Output Disable Command (DQMi = “High”)**

The Data Mask/Output Disable command disables DQ0 to DQ31 in read or write. In read cycle output buffers are disabled after 2 clocks . In write cycle input buffers are disabled at the same clock. The each DQM0, 1, 2 and 3 corresponds to DQ0 to DQ7, DQ8 to DQ15, DQ16 to DQ23 and DQ24 to DQ31 respectively.

**Burst Stop Command (CS, WE = “Low”, RAS, CAS = “High”)**

The Burst Stop command stops burst access when the access is in full page. After the Burst Stop command is entered, the output buffer goes into high impedance state.

**TRUTH TABLE****Command Truth Table**

Function	CS	RAS	CAS	WE	Address		
					BA	A8	A7 to A0
Device Deselect	H	×	×	×	×	×	×
No Operation	L	H	H	H	×	×	×
Mode Register Set	L	L	L	L	OP. CODE		
Auto Refresh	L	L	L	H	×	×	×
Bank Activate	L	L	H	H	BA	RA	
Read	L	H	L	H	BA	L	CA (A7 to A0)
Read with Auto Precharge	L	H	L	H	BA	H	CA (A7 to A0)
Write	L	H	L	L	BA	L	CA (A7 to A0)
Write with Auto Precharge	L	H	L	L	BA	H	CA (A7 to A0)
Precharge Select Bank	L	L	H	L	BA	L	×
Precharge All Banks	L	L	H	L	×	H	×
Burst Stop	L	H	H	L	×	×	×

**DQM Truth Table**

Function	DQM <sub>i</sub>
Data Write/Output Enable	L
Data Mask/Output Disable	H

Function Truth Table (1/2)

							Note 1	
Current State	CS	RAS	CAS	WE	BA	Address	Action	Note
Idle	H	x	x	x	x	x	NOP	
	L	H	H	H	x	x	NOP	
	L	H	H	L	BA	x	ILLEGAL	2
	L	H	L	x	BA	CA, A8	ILLEGAL	2
	L	L	H	H	BA	RA	Row Active	
	L	L	L	L	L	Op-Code	Mode Register Write	
	L	L	H	L	BA	A8	NOP	4
	L	L	L	H	x	x	Auto Refresh/Self refresh	5
Active (ACT)	H	x	x	x	x	x	NOP	
	L	H	H	x	x	x	NOP	
	L	H	L	H	BA	CA, A8	Read	
	L	H	L	L	BA	CA, A8	Write	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A8	Precharge	
	L	L	L	x	x	x	ILLEGAL	
Read (RD)	H	x	x	x	x	x	NOP (Continue Row Active after Burst ends)	
	L	H	H	H	x	x	NOP (Continue Row Active after Burst ends)	
	L	H	H	L	x	x	1,2,4,8 Burst Length : ILLEGAL Full Page Burst : Burst Stop → Row Active	
	L	H	L	H	BA	CA, A8	Term Burst, new Read	3
	L	H	L	L	BA	CA, A8	Term Burst, start Write	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A8	Term Burst, execute Precharge	
	L	L	L	x	x	x	ILLEGAL	
Write (WT)	H	x	x	x	x	x	NOP (Continue Row Active after Burst ends)	
	L	H	H	H	x	x	NOP (Continue Row Active after Burst ends)	
	L	H	H	L	x	x	1,2,4,8 Burst Length : ILLEGAL Full Page Burst : Burst Stop → Row Active	
	L	H	L	H	BA	CA, A8	Term Burst, start Read	3
	L	H	L	L	BA	CA, A8	Term Burst, new Write	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A8	Term Burst, execute Precharge	3
	L	L	L	x	x	x	ILLEGAL	

Function Truth Table (2/2)

								Note 1
Current State	CS	RAS	CAS	WE	BA	Address	Action	Note
Read with Auto Precharge (RAP)	H	×	×	×	×	×	NOP (Continue Burst to End and enter Row Precharge)	
	L	H	H	H	×	×	NOP (Continue Burst to End and enter Row Precharge)	
	L	H	H	L	×	×	ILLEGAL	
	L	H	L	H	BA	CA, A8	ILLEGAL	
	L	H	L	L	BA	CA, A8	ILLEGAL	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A8	ILLEGAL	2
	L	L	L	×	×	×	ILLEGAL	
Write with Auto Precharge (WAP)	H	×	×	×	×	×	NOP (Continue Burst to End and enter Row Precharge)	
	L	H	H	H	×	×	NOP (Continue Burst to End and enter Row Precharge)	
	L	H	H	L	×	×	ILLEGAL	
	L	H	L	H	BA	CA, A8	ILLEGAL	
	L	H	L	L	BA	CA, A8	ILLEGAL	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A8	ILLEGAL	2
	L	L	L	×	×	×	ILLEGAL	
Precharging (PRE)	H	×	×	×	×	×	NOP → Idle after $t_{RP}$	
	L	H	H	H	×	×	NOP → Idle after $t_{RP}$	
	L	H	H	L	BA	×	ILLEGAL	2
	L	H	L	×	BA	CA, A8	ILLEGAL	2
	L	L	H	H	BA	A8	ILLEGAL	2
	L	L	H	L	BA	×	NOP	4
Refreshing (REF)	H	×	×	×	×	×	NOP → Idle after $t_{RC}$	
	L	H	H	H	×	×	NOP → Idle after $t_{RC}$	
	L	H	H	L	×	×	ILLEGAL	
	L	H	L	×	BA	CA, A8	ILLEGAL	
	L	L	H	H	BA	RA	ILLEGAL	
	L	L	H	L	BA	A8	ILLEGAL	
	L	L	L	×	×	×	ILLEGAL	

## ABBREVIATIONS

BA = Bank Address

RA = Row Address

CA = Column Address

NOP = No Operation command

- Notes:
1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.
  2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
  3. To avoid bus contention, satisfy  $t_{CCD}$  and  $t_{DPL}$ .
  4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A8.
  5. Illegal if any bank is not idle.

**Function Truth Table for CKE**

Current State (n)	CKEn-1	CKEn	CS	RAS	CAS	WE	Address	Action	Note
Self Refresh (SREF)	H	x	x	x	x	x	x	INVALID	
	L	H	H	x	x	x	x	Exit Self Refresh → ABI	
	L	H	L	H	H	H	x	Exit Self Refresh → ABI	
	L	H	L	H	H	L	x	ILLEGAL	
	L	H	L	H	L	x	x	ILLEGAL	
	L	H	L	L	x	x	x	ILLEGAL	
	L	L	x	x	x	x	x	NOP (Maintain Self Refresh)	
Power Down (PD)	H	x	x	x	x	x	x	INVALID	
	L	H	H	x	x	x	x	Exit Self Refresh → ABI	
	L	H	L	H	H	H	x	Exit Self Refresh → ABI	
	L	H	L	H	H	L	x	ILLEGAL	
	L	H	L	H	L	x	x	ILLEGAL	
	L	H	L	L	x	x	x	ILLEGAL	
	L	L	x	x	x	x	x	NOP (Continue power down mode)	
All Banks Idle (ABI)	H	H	x	x	x	x	x	Refer to Truth Table	6
	H	L	H	x	x	x	x	Enter Power Down	6
	H	L	L	H	H	H	x	Enter Power Down	6
	H	L	L	H	H	L	x	ILLEGAL	6
	H	L	L	H	L	x	x	ILLEGAL	6
	H	L	L	L	H	L	x	ILLEGAL	6
	H	L	L	L	L	H	x	Enter Self Refresh	6
	H	L	L	L	L	L	x	ILLEGAL	6
	L	L	x	x	x	x	x	NOP	6
Any State Other than Listed Above	H	H	x	x	x	x	x	Refer to Truth Table	
	H	L	x	x	x	x	x	Begin Clock Suspend Next Cycle	
	L	H	x	x	x	x	x	Enable Clock of Next Cycle	
	L	L	x	x	x	x	x	Continue Clock Suspension	

Note: 6. Power-down and self refresh can be entered only when all the banks are in an idle state.

**Mode Set Address Keys**

Operation Code			CAS Latency				Burst Type		Burst Length				
A8	A7	TM	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	0	Mode Setting	0	0	0	Reserved	0	Sequential	0	0	0	1	Reserved
0	1	Vender Use Only	0	0	1	Reserved	1	Interleave	0	0	1	2	Reserved
1	0		0	1	0	2			0	1	0	4	4
1	1		0	1	1	3			0	1	1	8	8
			1	0	0	Reserved			1	0	0	Reserved	Reserved
			1	0	1	Reserved			1	0	1	Reserved	Reserved
			1	1	0	Reserved			1	1	0	Reserved	Reserved
			1	1	1	Reserved			1	1	1	Full Page	Reserved

**POWER ON SEQUENCE**

1. With CKE = "H", DQM = "H" and the other inputs in NOP state, turn on the power supply and start the system clock.
2. After the  $V_{CC}$  voltage has reached the specified level, pause for 200  $\mu$ s or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply an Auto-refresh 2 or more times.
5. Enter the mode register command.

**Burst Length and Sequence**

BL = 2

Starting Address (column address A0, binary)	Sequential Type	Interleave Type
0	0, 1	Not supported
1	1, 0	Not supported

BL = 4

Starting Address (column address A1, A0, binary)	Sequential Type	Interleave Type
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

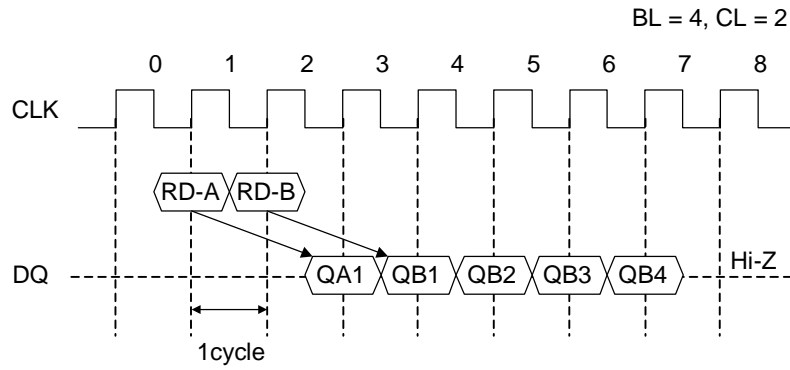
BL = 8

Starting Address (column address A2 to A0, binary)	Sequential Type	Interleave Type
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

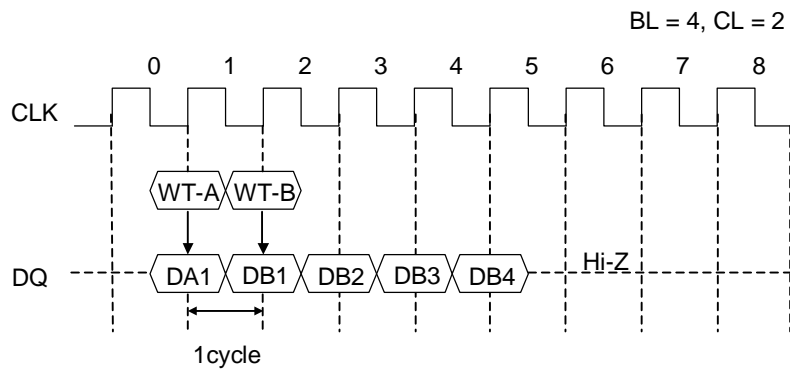
BL = Full: Sequential only

**READ/WRITE COMMAND INTERVAL**

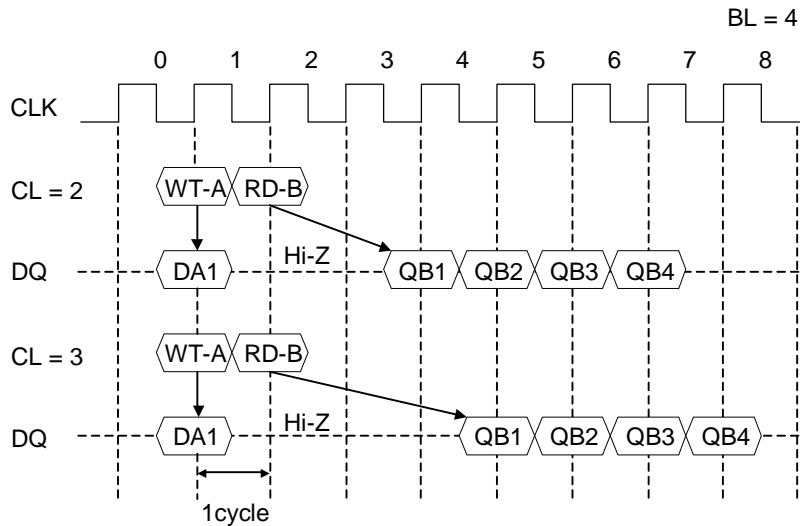
**Read to Read Command Interval**



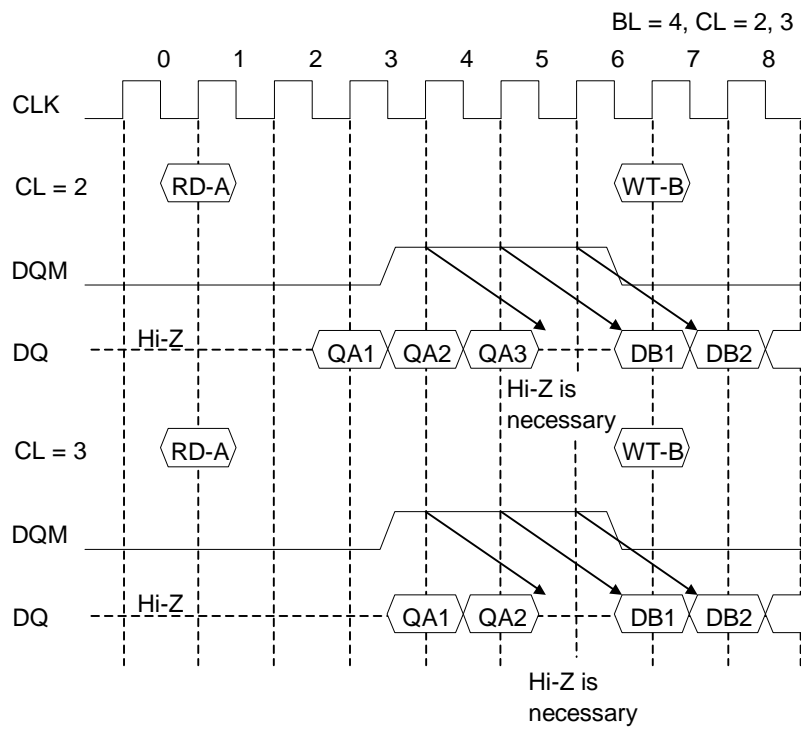
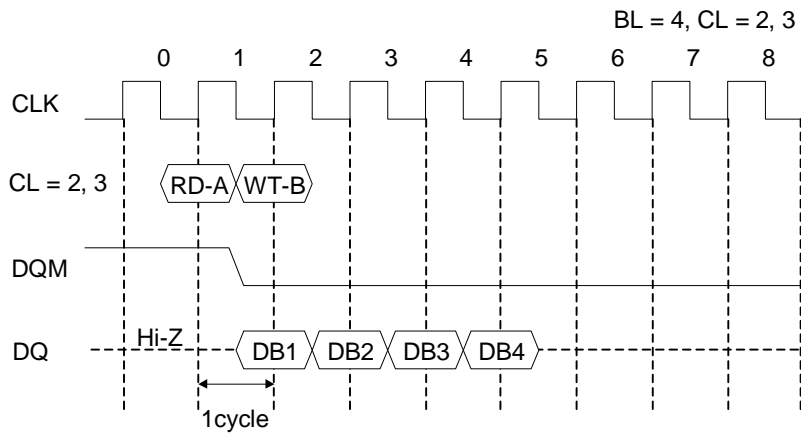
**Write to Write Command Interval**



**Write to Read Command Interval**

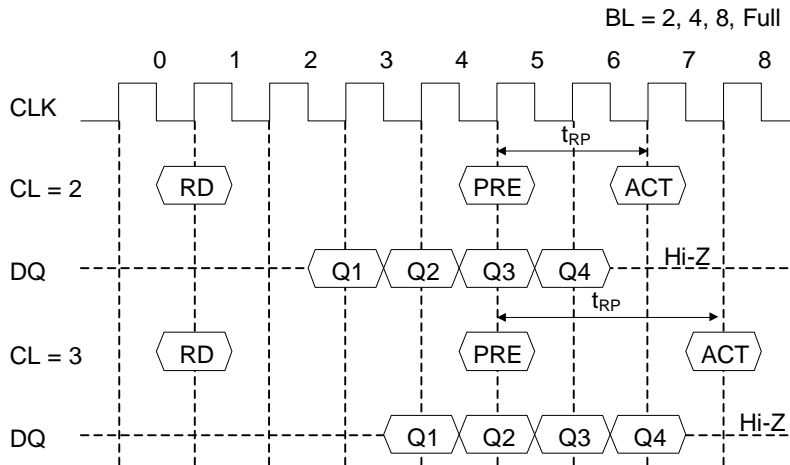


**Read to Write Command Interval**

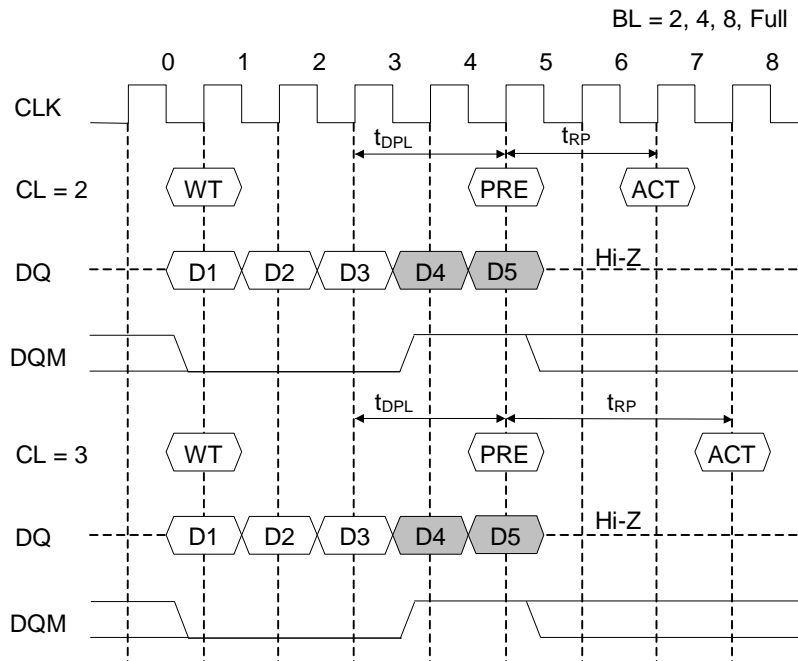


### BURST TERMINATION

#### Burst Read Termination by Precharging in READ Cycle

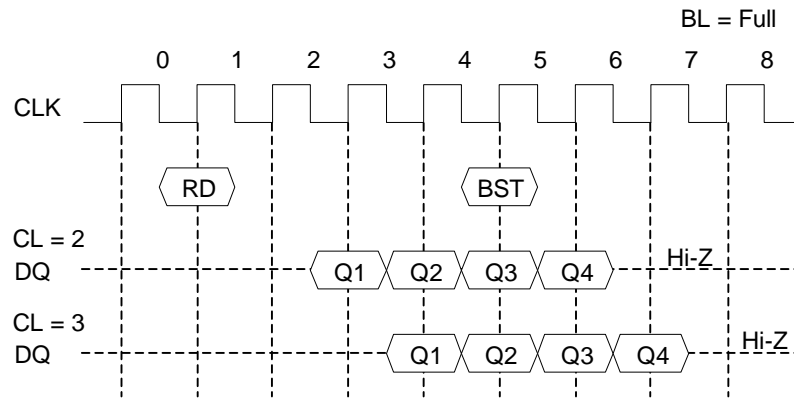


#### Burst Write Termination by Precharging in WRITE Cycle

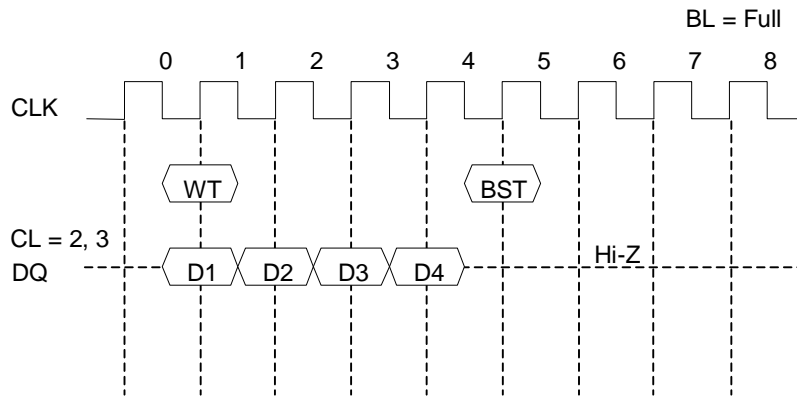


Note: The burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the CLK by  $t_{DPL}$ .

**Read Burst Stop Command**

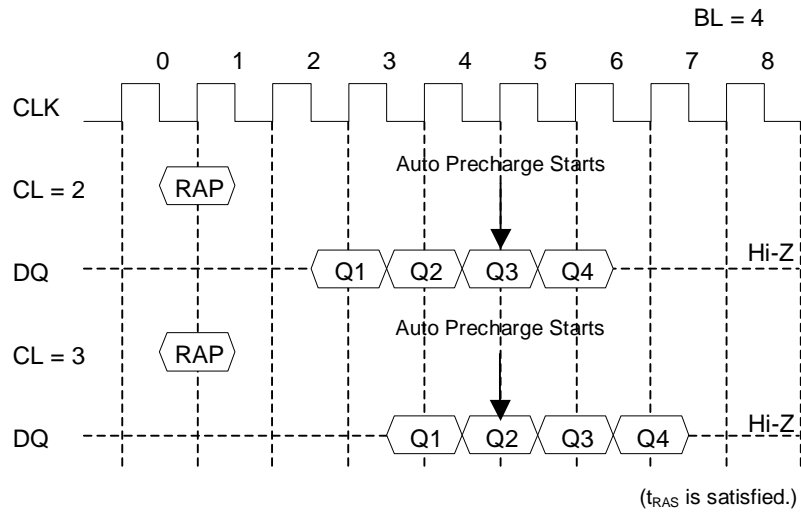


**Write Burst Stop Command**

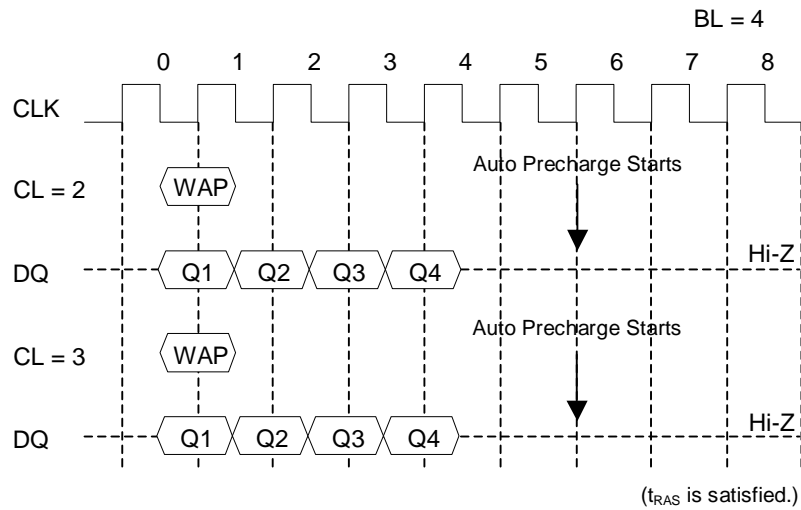


### AUTO PRECHARGE

#### Read with Auto Precharge



#### Write with Auto Precharge



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Power Supply Pin Relative to GND	$V_{CC}$	-0.5 to 4.6	V
Voltage on Input Pin Relative to GND	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5 \leq 4.6$	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	1	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

\*:  $T_a = 25\text{ °C}$

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

( $T_a = 0\text{ to }70\text{ °C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V

### Capacitance

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 25\text{ °C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 to A8, BA)	$C_{IN1}^*$	—	5	pF
Input Capacitance (CLK, CKE, CS, RAS, CAS, WE DQM0 to DQM3)	$C_{IN2}^*$	—	5	pF
Output Capacitance (DQ0 to DQ31)	$C_{OUT}^*$	—	6	pF

\*: This parameter is sampled and not 100% tested.

**DC Characteristics**

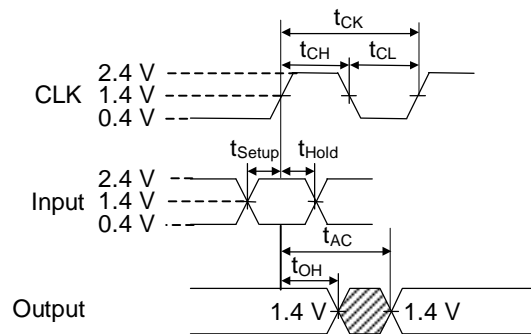
Parameter	Symbol	Test Condition		MS82V08520-8		Unit	Note
		CKE	Other	Min.	Max.		
Output High Voltage	$V_{OH}$	—	$I_{OH} = -2.0 \text{ mA}$	2.4	—	V	
Output Low Voltage	$V_{OL}$	—	$I_{OL} = 2.0 \text{ mA}$	—	0.4	V	
Input Leakage Current	$I_{LI}$	—	—	-10	10	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	—	—	-10	10	$\mu\text{A}$	
Operating Current (1 Bank)	$I_{CC1}$	$CKE \geq V_{IH}$	$t_{CK} = \text{min.}$ $t_{RC} = \text{min.}$ No Burst	—	170	mA	1, 2
Precharge Standby Current in Power Down Mode	$I_{CC2P}$	$CKE \leq V_{IL}$	$t_{CK} = \text{min.}$	—	2	mA	3
	$I_{CC2PS}$	$CKE \leq V_{IL}$	$CLK \leq V_{IL}$ $t_{CK} = \infty$	—	2	mA	2
Precharge Standby Current in Non Power Down Mode	$I_{CC2N}$	$CKE \geq V_{IH}$	$CS \geq V_{IH}$ $t_{CK} = \text{min.}$	—	45	mA	2
	$I_{CC2NS}$	$CKE \geq V_{IH}$	$CLK \leq V_{IL}$ $t_{CK} = \infty$	—	25	mA	
Active Standby Current in Power Down Mode	$I_{CC3P}$	$CKE \leq V_{IL}$	$t_{CK} = \text{min.}$	—	3	mA	3
	$I_{CC3PS}$	$CKE \leq V_{IL}$	$CLK \leq V_{IL}$ $t_{CK} = \infty$	—	3	mA	3
Active Standby Current in Non Power Down Mode	$I_{CC3N}$	$CKE \geq V_{IH}$	$CS \geq V_{IH}$ $t_{CK} = \text{min.}$	—	50	mA	3
	$I_{CC3NS}$	$CKE \geq V_{IH}$	$CLK \leq V_{IL}$ $t_{CK} = \infty$	—	30	mA	3
Operating Current (Burst Mode)	$I_{CC4}$	$CKE \geq V_{IH}$	$t_{CK} = \text{min.}$	$CL=2$	180	mA	1, 2
				$CL=3$	200		
Refresh Current	$I_{CC5}$	$CKE \geq V_{IH}$	$t_{RC} \geq \text{min.}$	—	140	mA	
Self Refresh Current	$I_{CC6}$	$CKE \leq 0.2V$	—	—	3	mA	

- Notes
1. The maximum value of power supply current is obtained with the output open.
  2. Address and data are changed only one time during one cycle.
  3. Address and data are changed only one time during two cycles.

## AC Characteristics

### Test conditions

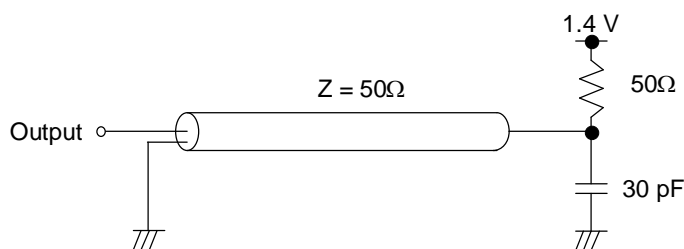
- AC measurements assume  $t_T = 1$  ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- If  $t_T$  is longer than 1 ns, reference level for measuring timing of input signals is  $V_{IH(MIN)}$  and  $V_{IL(MAX)}$ .
- An access time is measured at 1.4 V.
- Input levels at the AC testing are 2.4 V/0.4 V.



## Synchronous Characteristics

Parameter		Symbol	MS82V08520-8		Unit	Note
			Min.	Max.		
Clock Cycle Time	CAS Latency = 3	$t_{CK3}$	8	—	ns	
	CAS Latency = 2	$t_{CK2}$	12	—	ns	
Access Time from CLK	CAS Latency = 3	$t_{AC3}$	—	6.5	ns	1
	CAS Latency = 2	$t_{AC2}$	—	9	ns	1
CLK High Level Width		$t_{CH}$	3	—	ns	
CLK Low Level Width		$t_{CL}$	3	—	ns	
Data-out Hold Time		$t_{OH}$	2	—	ns	
Data-out Low-impedance Time		$t_{LZ}$	0	—	ns	
Data-out High-impedance Time		$t_{HZ}$	—	6	ns	
Data-in Setup Time		$t_{DS}$	2.5	—	ns	
Data-in Hold Time		$t_{DH}$	1	—	ns	
Address Setup Time		$t_{AS}$	2.5	—	ns	
Address Hold Time		$t_{AH}$	1	—	ns	
CKE Setup Time		$t_{CKS}$	2.5	—	ns	
CKE Hold Time		$t_{CKH}$	1	—	ns	
Command (CS, RAS, CAS, WE, DQM) Setup Time		$t_{CMS}$	2.5	—	ns	
Command (CS, RAS, CAS, WE, DQM) Hold Time		$t_{CMH}$	1	—	ns	

Note 1. Output load.

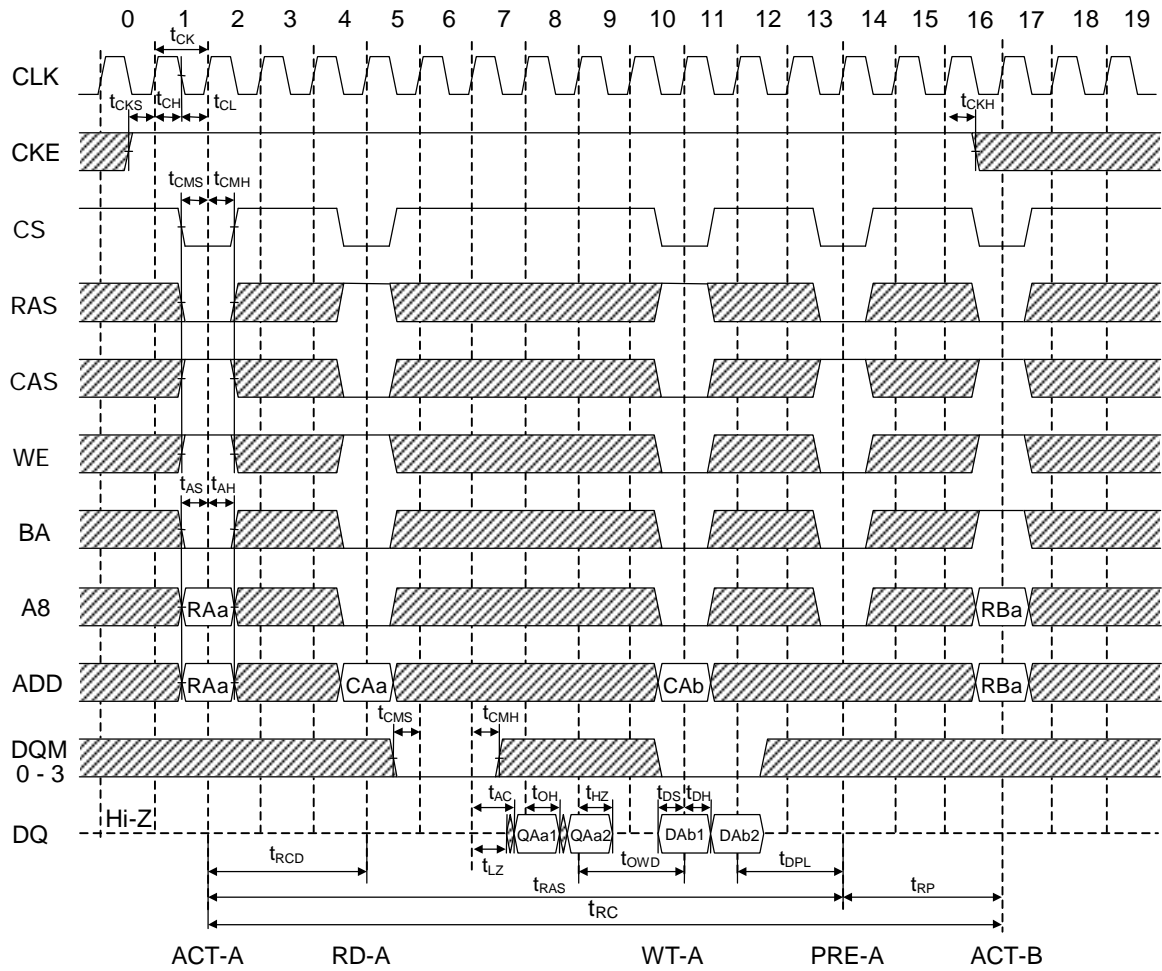


**Asynchronous Characteristics**

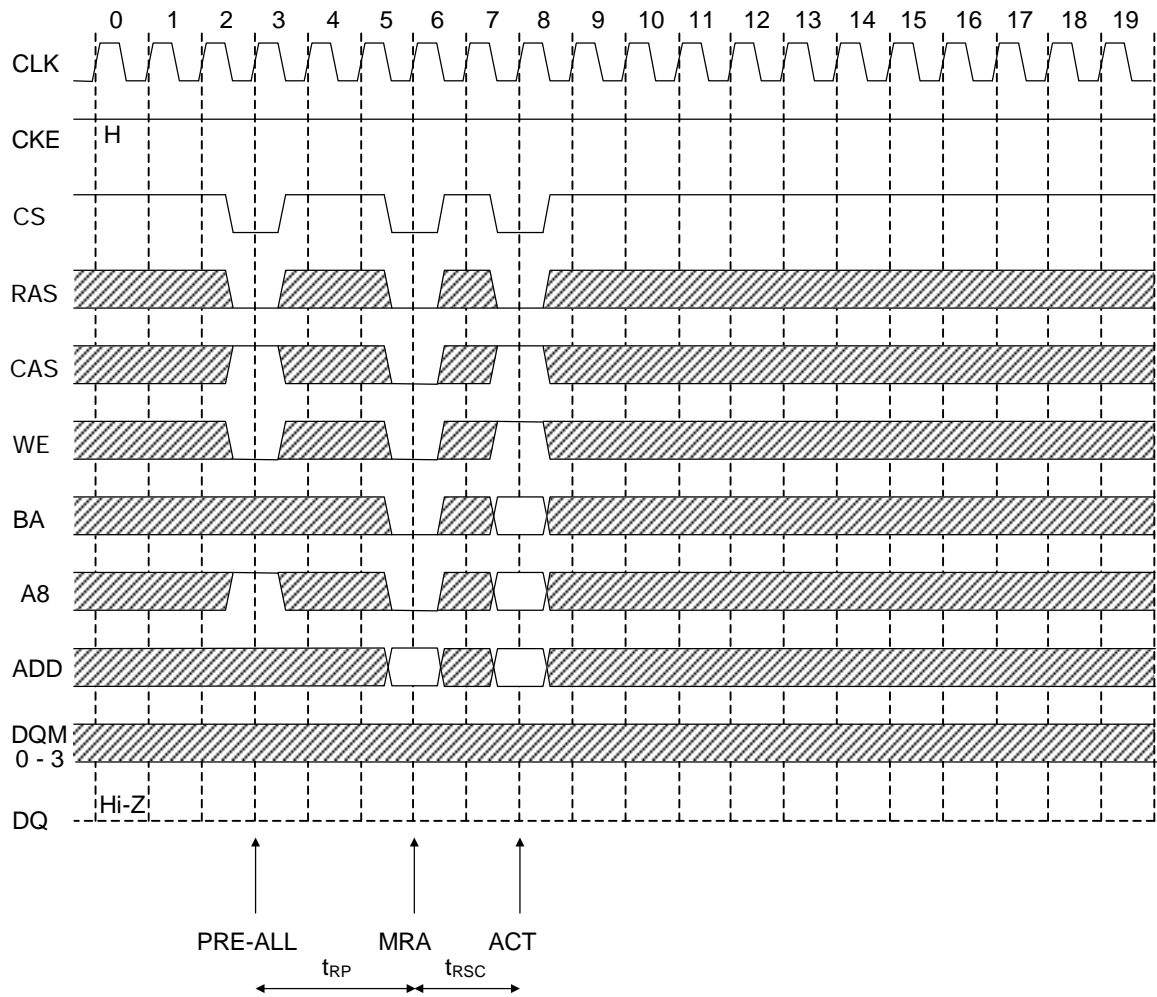
Parameter	Symbol	MS82V08520-8		Unit	Note
		Min.	Max.		
REF to REF/ACT Command Period	$t_{RC}$	72	—	ns	
ACT to PRE Command Period	$t_{RAS}$	48	120k	ns	
PRE to ACT Command Period	$t_{RP}$	24	—	ns	
Delay Time ACT to READ/WRITE Command	$t_{RCD}$	24	—	ns	
ACT (A) to ACT (B) Command Period	$t_{RRD}$	16	—	ns	
READ/WRITE to READ/WRITE Command Period	$t_{CCD}$	8	—	ns	
Data-in to PRE Command Period	$t_{DPL}$	16	—	ns	
Data Output to WRITE Command Input Time	$t_{OWD}$	16	—	ns	
Mode Register Set Cycle Time	$t_{RSC}$	16	—	ns	
Transition Time	$t_T$	1	30	ns	
Refresh Time	$t_{REF}$	—	16	ms	

**TIMING WAVEFORM**

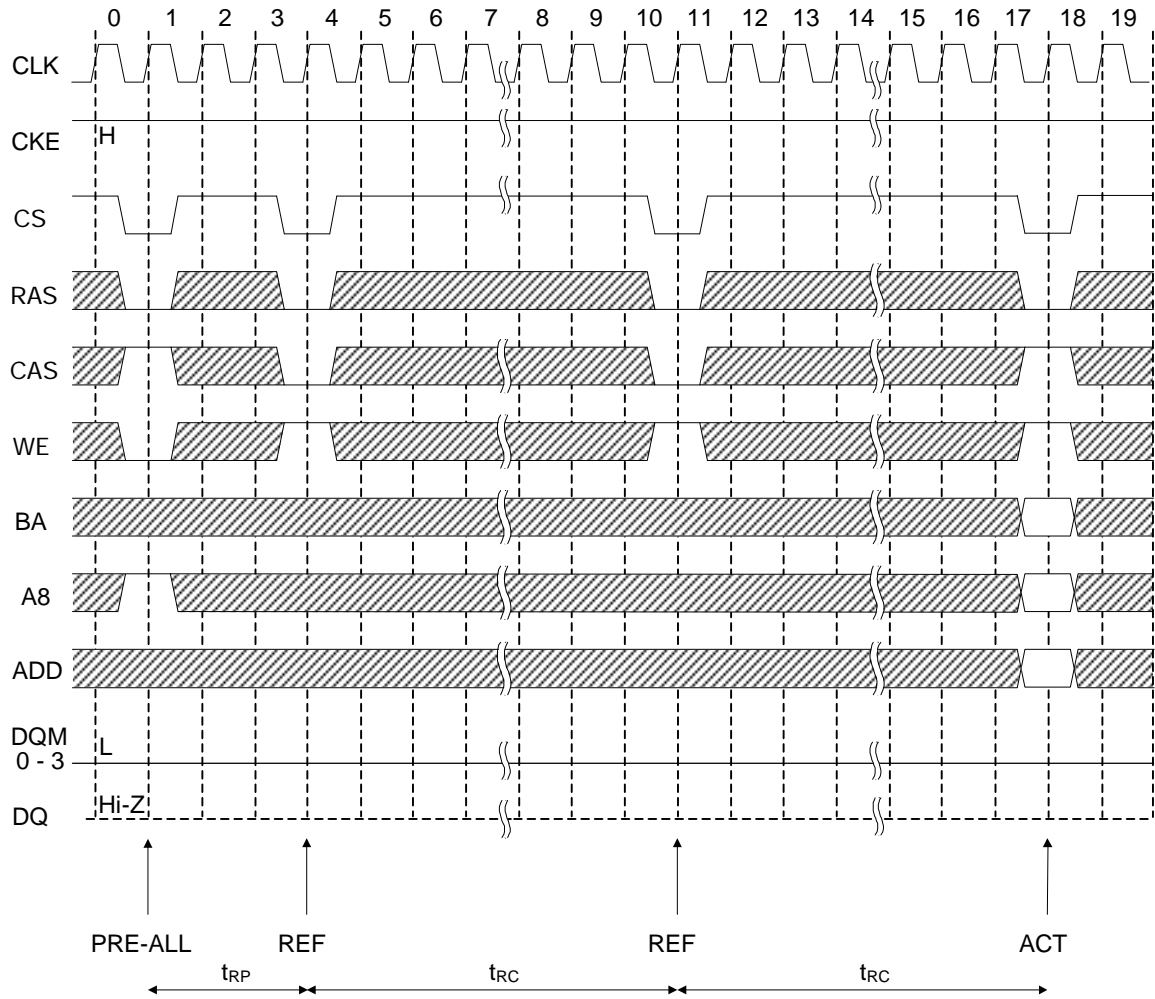
**READ/WRITE Cycle (BL = 2, CL = 3)**



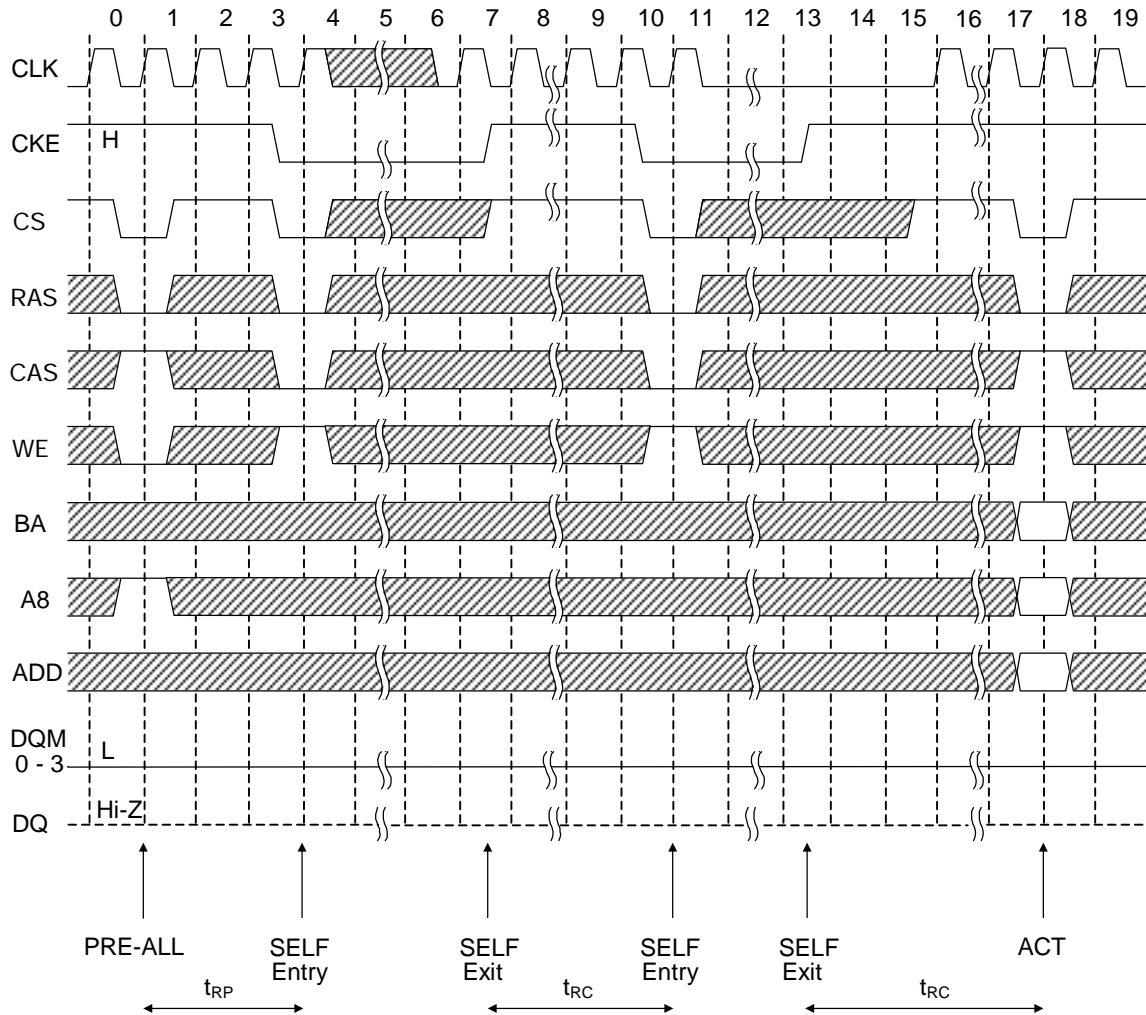
**Mode Register Set**



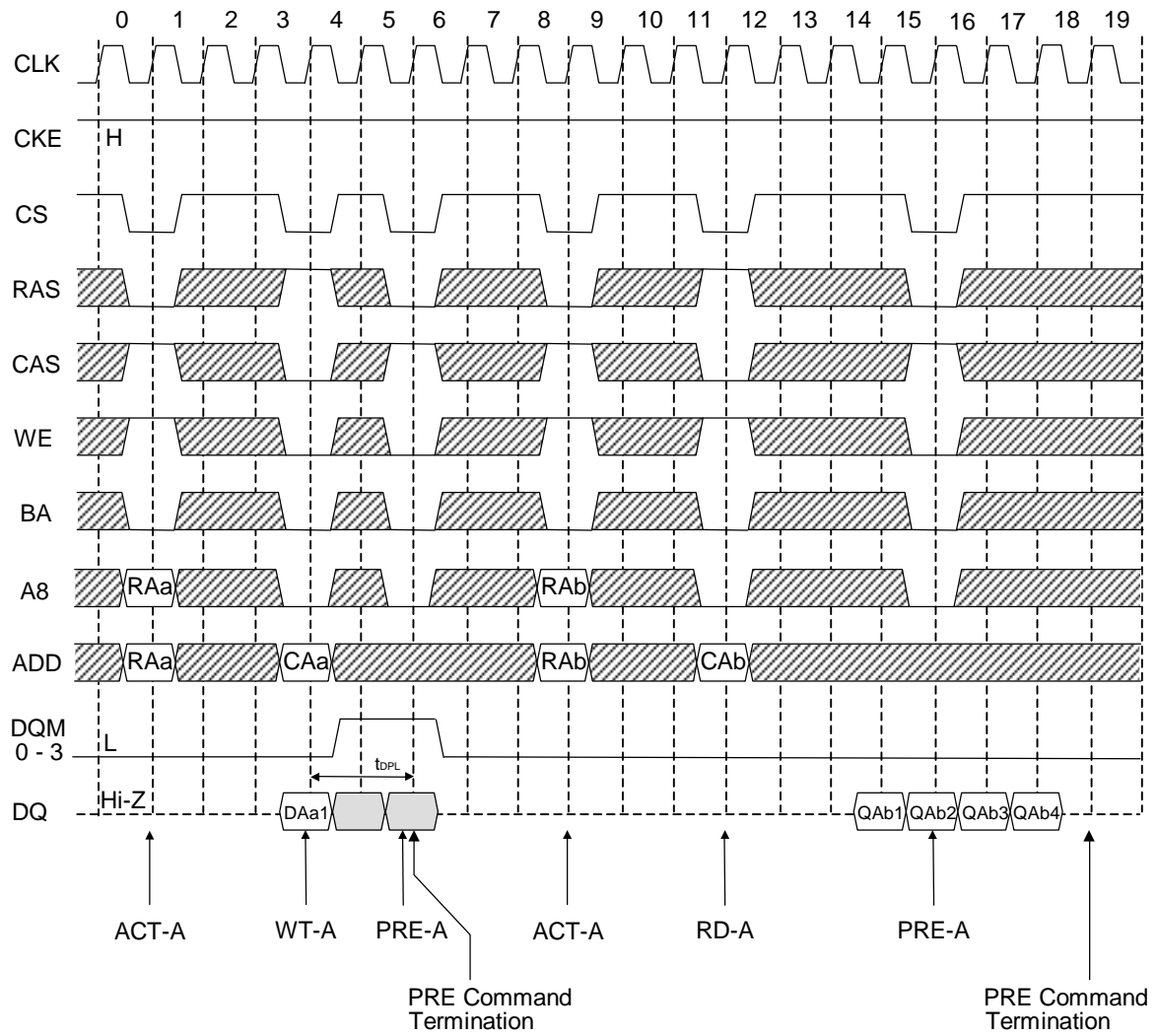
**Auto Refresh**



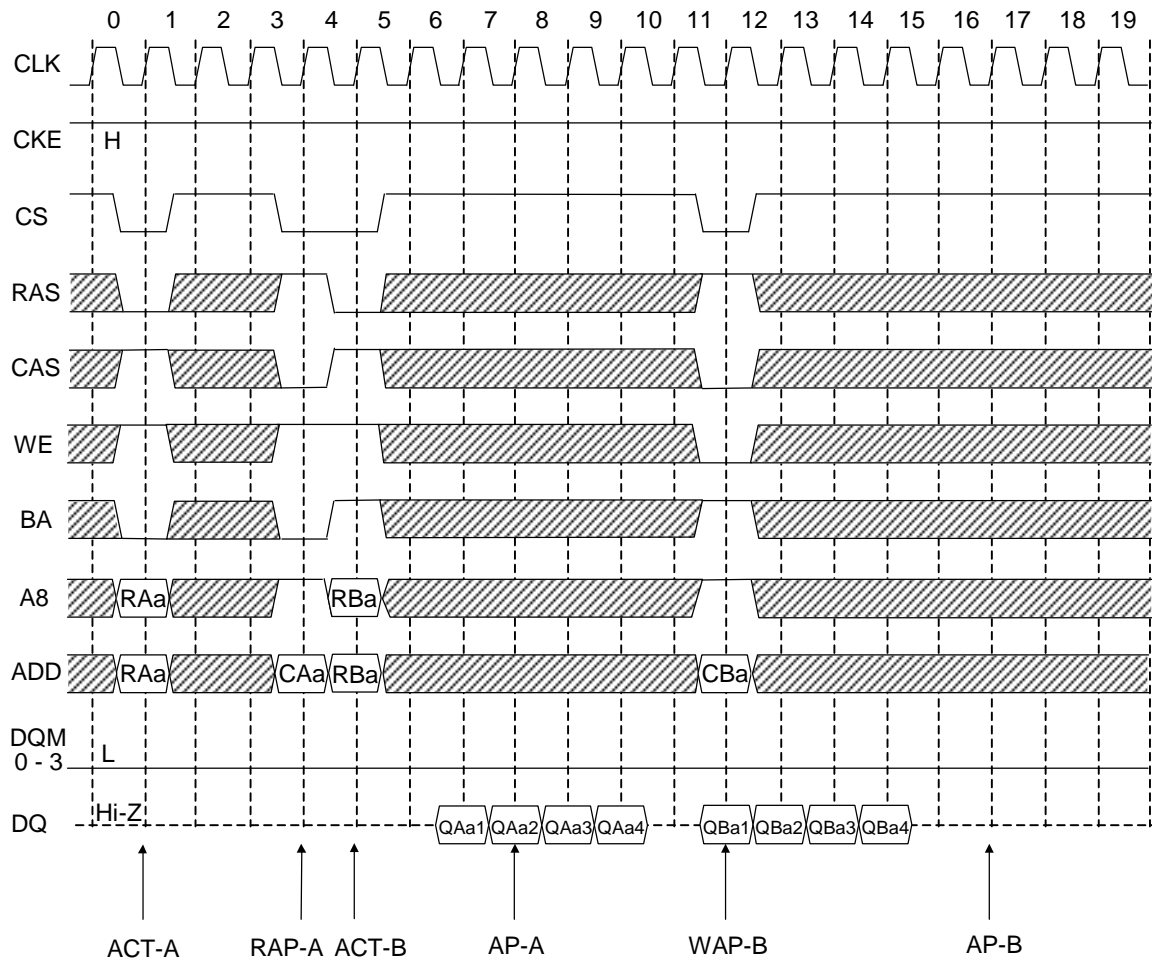
**Self Refresh (Entry and Exit)**



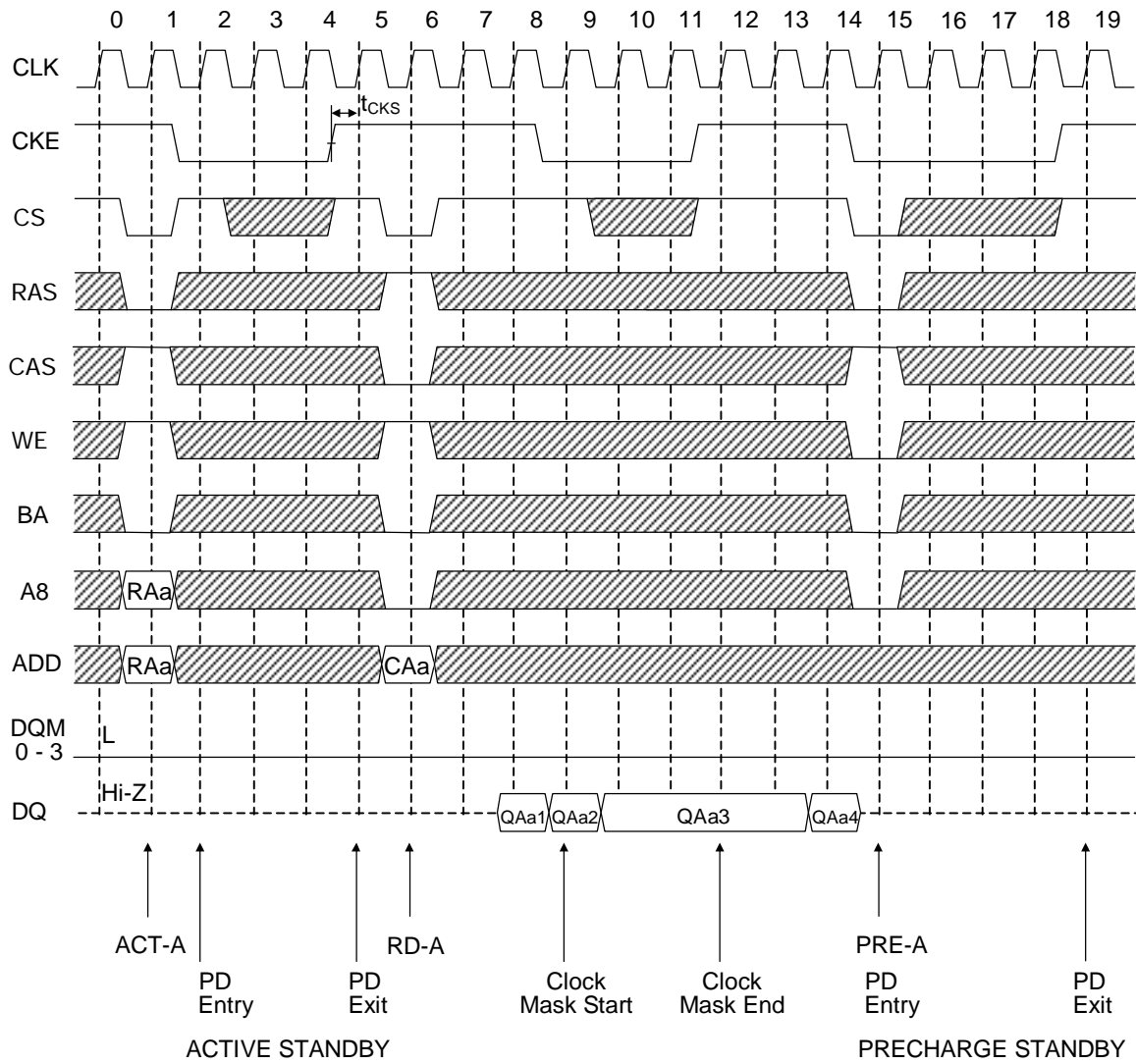
**Burst Termination by Precharging (BL = 8, CL = 3)**



**Auto Precharge (BL = 4, CL = 3)**



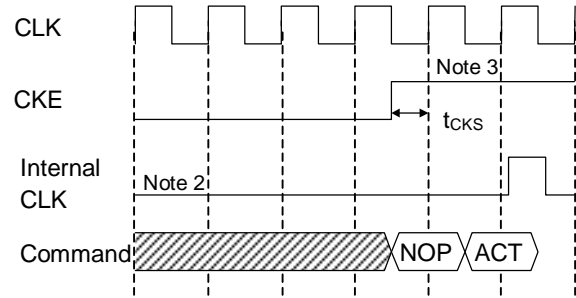
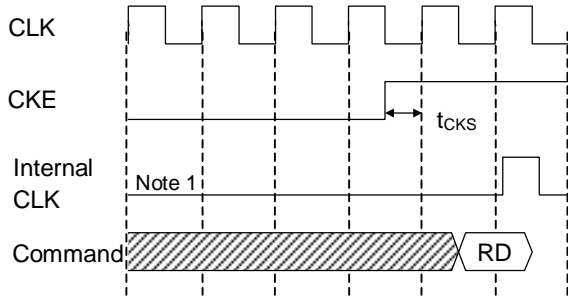
**Power Down Mode and Clock Suspension (BL = 4, CL = 2)**



**CLOCK Suspend Exit & Power Down Exit**

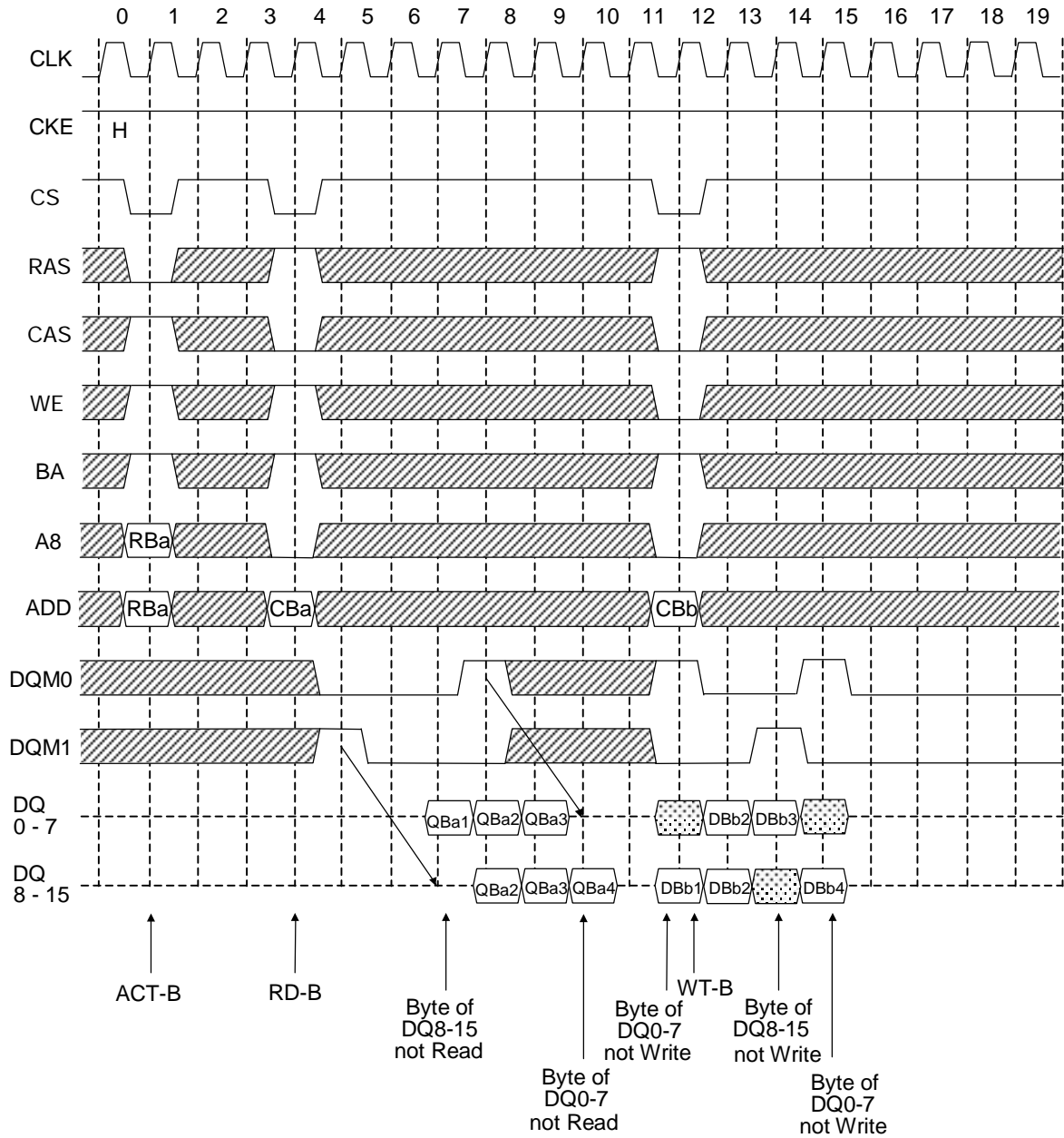
1) Clock Suspend (= Active Power Down) Exit

2) Power Down (= Precharge Power Down) Exit

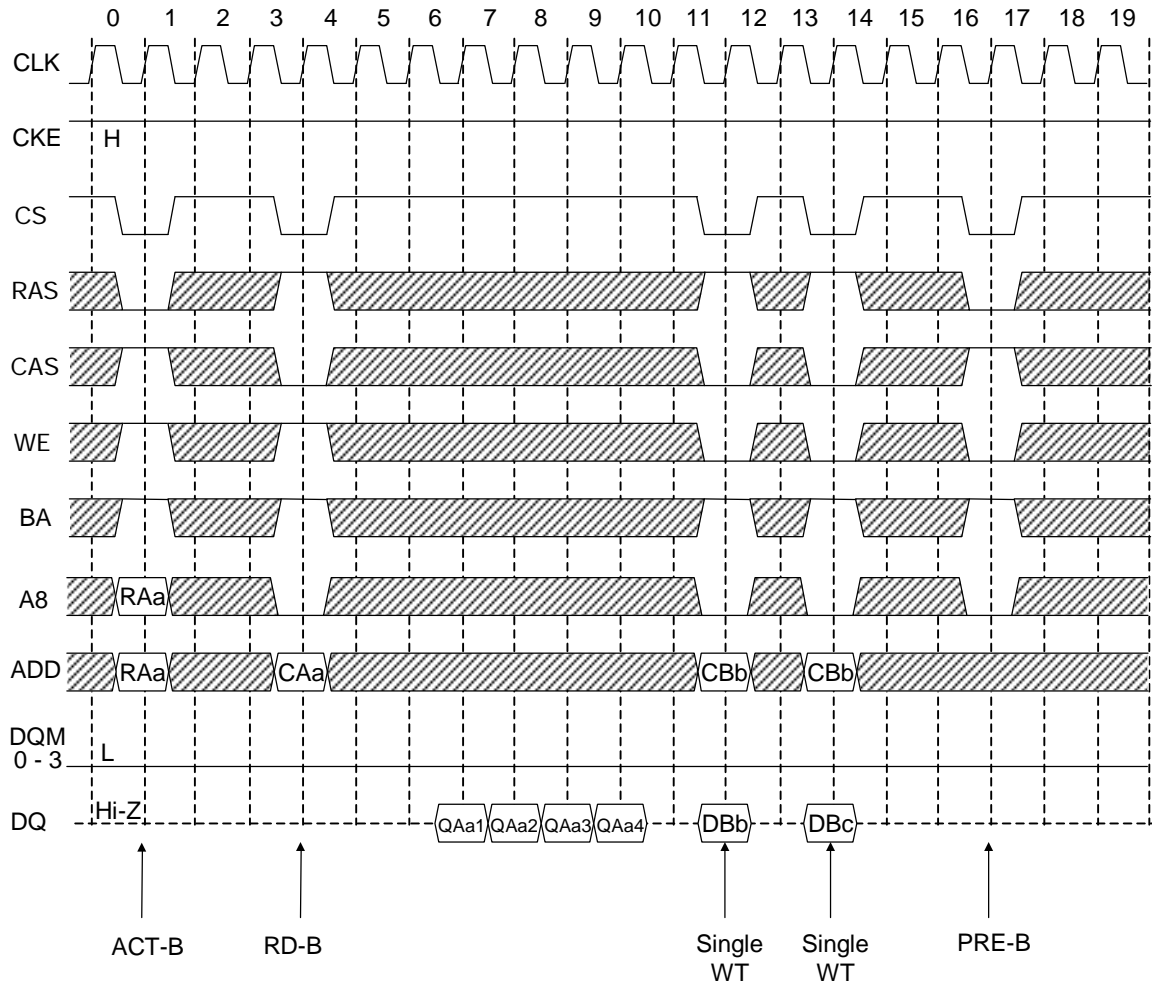


- Notes:
1. Active power down: one or both bank active state.
  2. Precharge power down: both bank precharge state.
  3. NOP should be issued. And new command can be issued after 1 Clock.

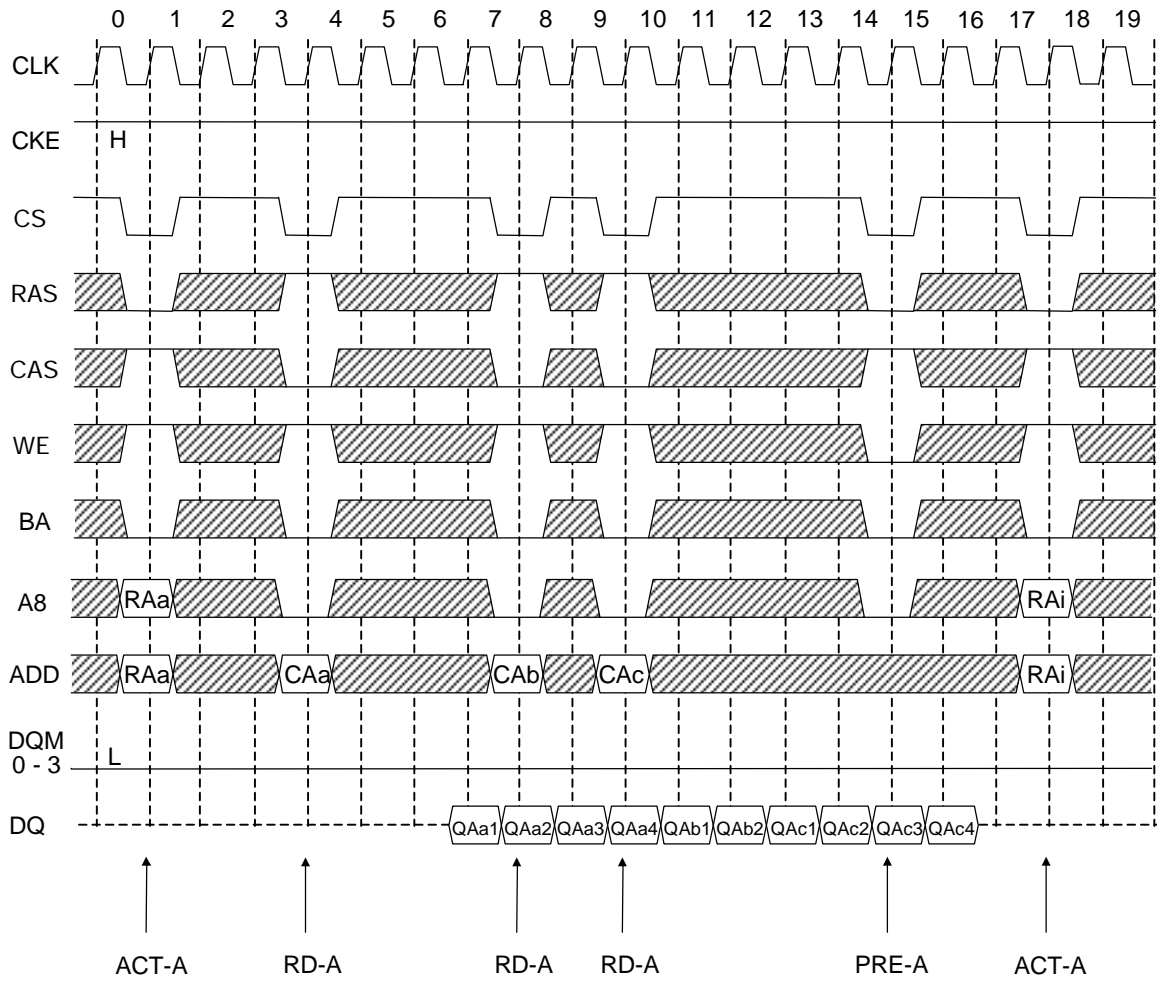
**Byte Read/Write Operation (by DQM) (BL = 4, CL = 3)**



**Burst Read and Single Write (BL = 4, CL = 3)**



**Random Column Read (Continuous Read of Same Bank) (BL = 4, CL = 3)**

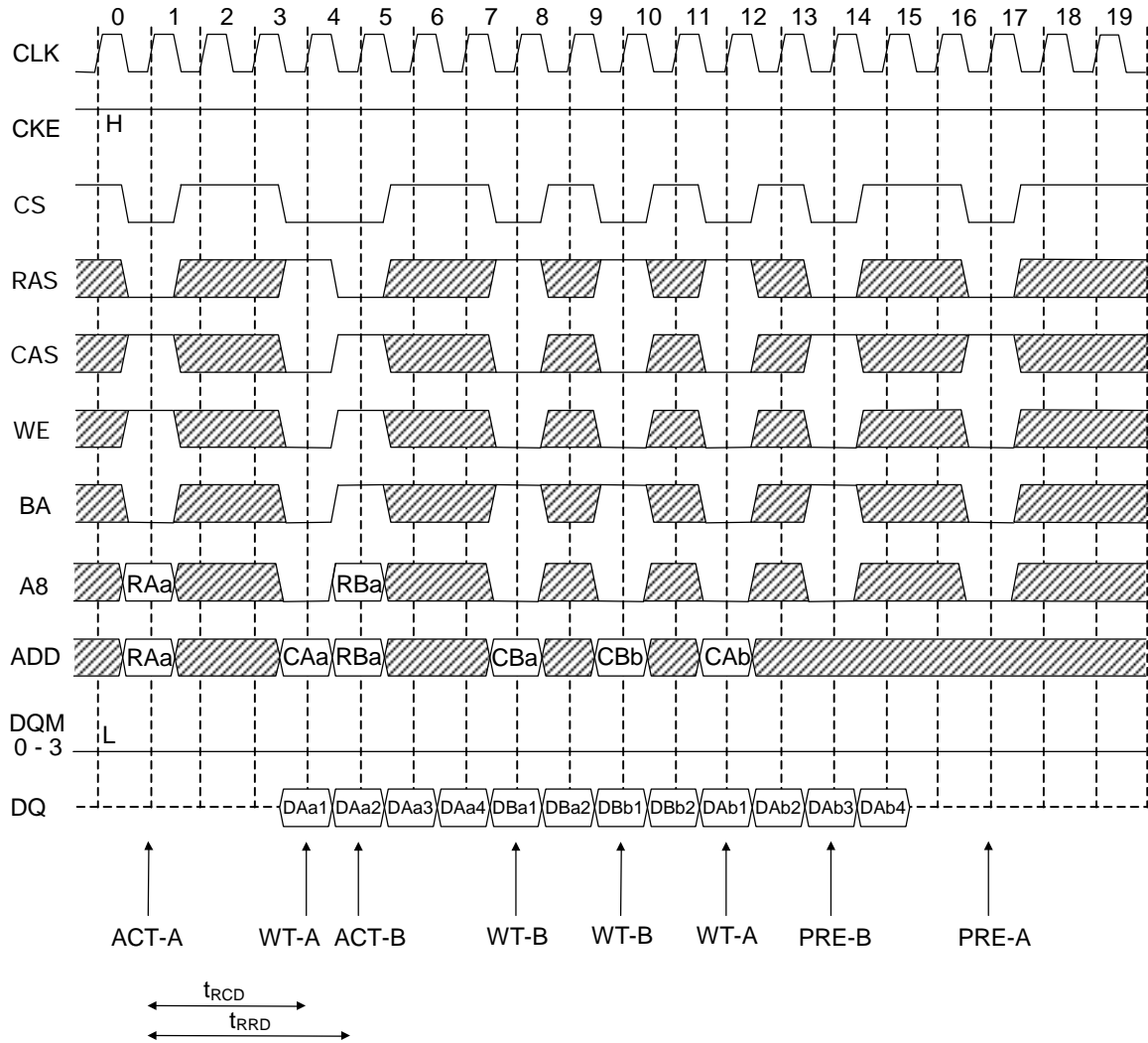


**Random Column Write (Continuous Write of Same Bank) (BL = 4, CL = 3)**



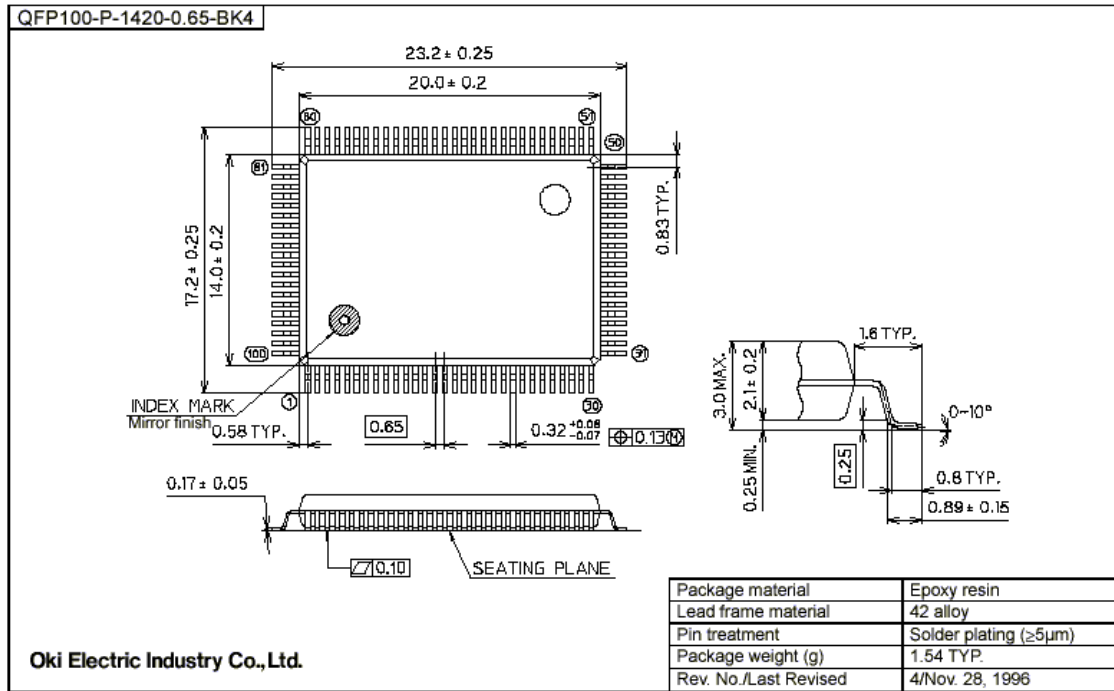


**Interleaved Column Write (BL = 4, CL = 3)**



**PACKAGE DIMENSIONS**

(Unit: mm)



**Notes for Mounting the Surface Mount Type Package**

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDS82V08520-01	Jan. 2003	–	–	Preliminary first edition
FEDS82V08520-01	Feb. 2003	–	–	First edition

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