HD74HC680

12-bit Address Comparator

HITACHI

ADE-205-527 (Z)
1st. Edition
Sep. 2000

Description

The HD74HC680 address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A_1 through A_7 must be low and that inputs A_8 through A_{12} must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The HD74HC680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

Features

- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

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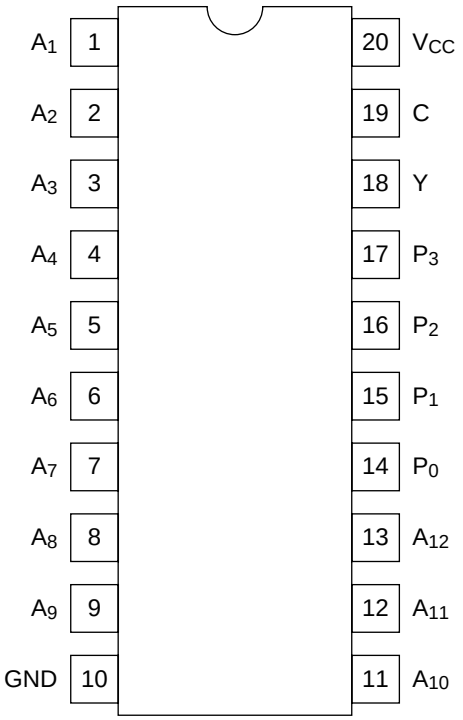
Function Table

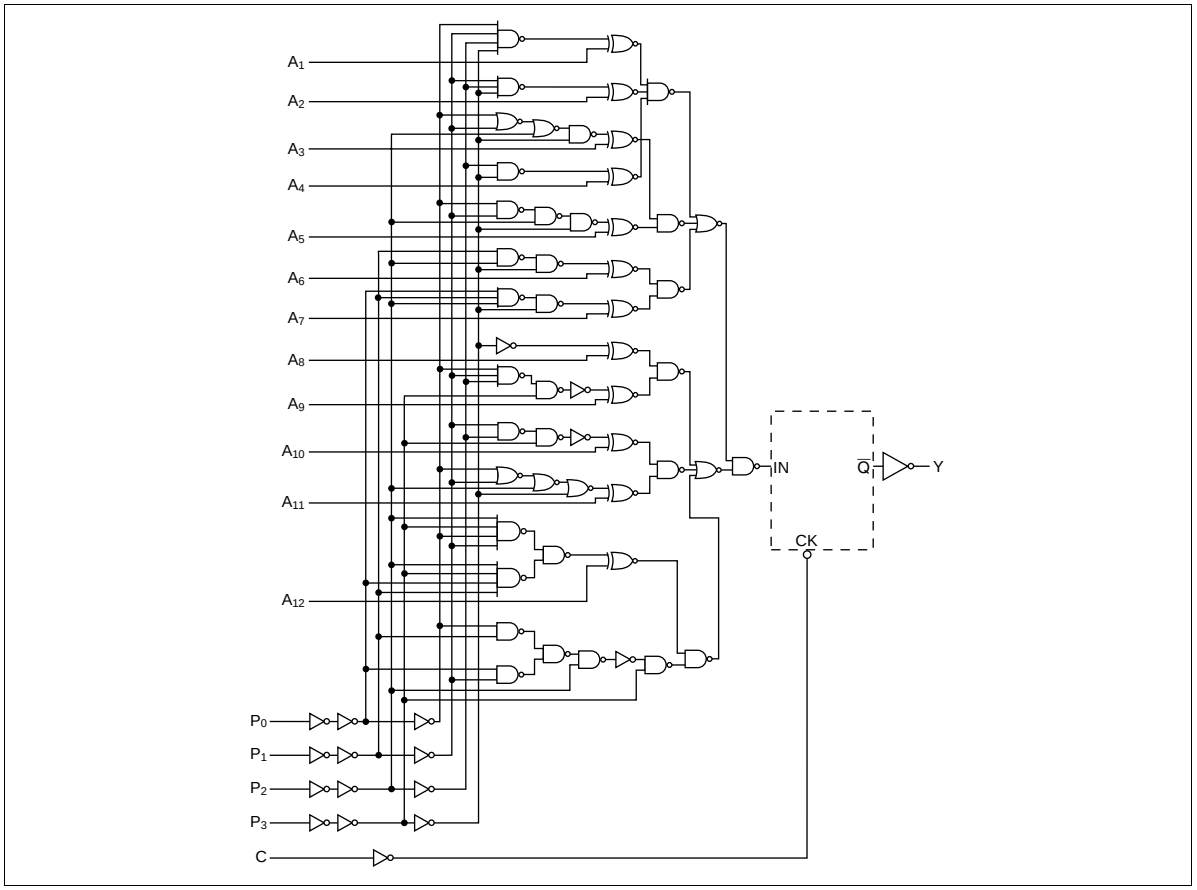
	Inputs																
C	**P_3**	**P_2**	**P_1**	**P_0**	**A_1**	**A_2**	**A_3**	**A_4**	**A_5**	**A_6**	**A_7**	**A_8**	**A_9**	**A_{10}**	**A_{11}**	**A_{12}**	**Output Y**
H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	H
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
H	All other combinations																H
L	Any combination																Latched

Pin Arrangement



(Top view)

Logic Diagram



DC Characteristics

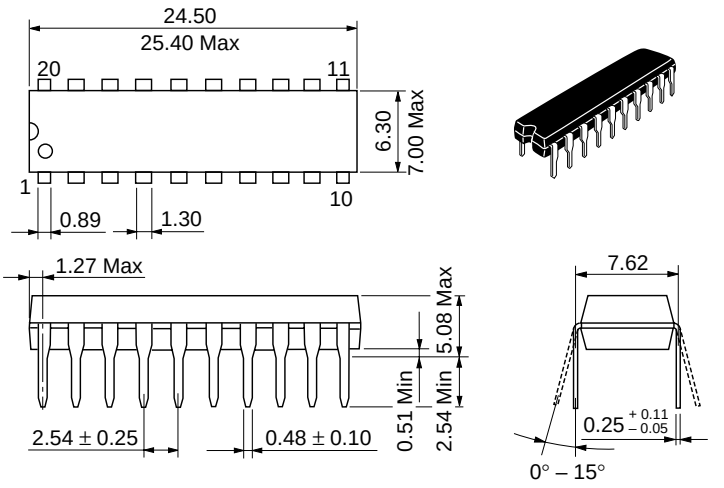
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V_{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—		I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33		I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Propagation delay time	t_{PLH}	2.0	—	—	330	—	410	ns	P to Y
	t_{PHL}	4.5	—	26	66	—	82		
		6.0	—	—	56	—	70		
	t_{PLH}	2.0	—	—	210	—	265	ns	A to Y
	t_{PHL}	4.5	—	19	42	—	53		
		6.0	—	—	36	—	45		
	t_{PLH}	2.0	—	—	150	—	190	ns	C to Y
	t_{PHL}	4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{SU}	2.0	100	—	—	125	—	ns	A to C
		4.5	20	12	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
	t_{THL}	4.5	—	6	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

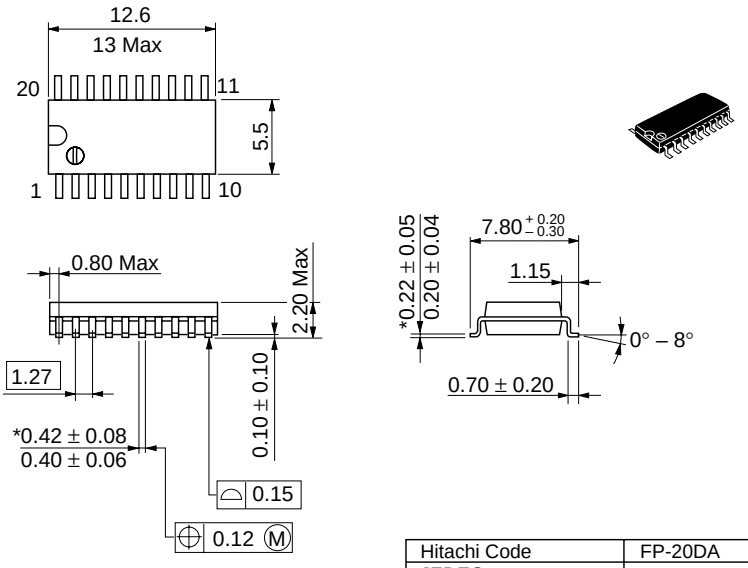
Package Dimensions

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.26 g

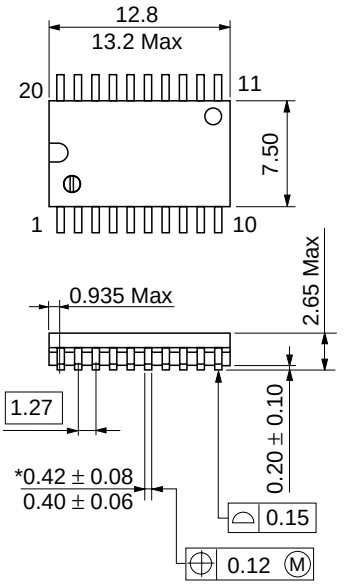
Unit: mm

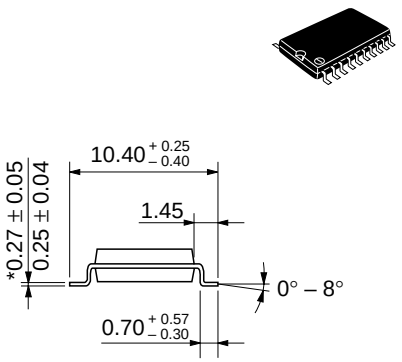


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.31 g

Unit: mm





*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.52 g

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