



# XRD6418

CMOS 10-Bit, 6 MSPS, High Speed  
Analog-to-Digital Converter  
with 8:1 Input Analog Multiplexer

## FEATURES

- 10-Bit Resolution
- 6 MHz Sampling Rate
- 8:1 Analog Input Multiplexer
- Internal S/H Function
- Single 5.0V Power Supply
- 3V or 5V Logic Output Interface
- $V_{IN}$  DC Range: 0V to  $V_{DD}$
- $V_{REF}$  DC Range: 1V to  $V_{DD}$
- Low Power: 65mW (typ)
- Three-State Digital Outputs
- Power Down: 0.8mW (typ) Power Dissipation
- ESD Protection: 2000V Minimum
- For 3.3V Operation Refer to XRD64L18

## APPLICATIONS

- Multiplexed Data Acquisition
- Precision Scanners
- Digital Color Copiers
- Test and Scientific Instruments
- Digital Cameras
- Medical Imaging
- IR Imaging

## BENEFITS

- Complete Analog-to-Digital Converter (ADC) that Requires no External Active Components
- Small Outline Package to Reduce Board Space
- Easy to Use Rugged Design

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## GENERAL DESCRIPTION

The XRD6418 is a 10-bit, 6MSPS, Analog-to-Digital Converter (ADC) with a 8:1 Analog Input Multiplexer for applications that require high speed and high accuracy. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The XRD6418 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the XRD6418 includes an on-chip S/H function that allows the product to digitize analog input signals between AGND and  $AV_{DD}$ . The XRD6418 can be placed into power-down (stand-by)

mode, reducing the power dissipation to 0.8mW (typical) by a digitally controlled pin.

Providing external reference voltages allows easy interface to any input signal range between AGND and  $AV_{DD}$ . This also allows the system to calibrate out zero scale and full scale errors by adjusting  $V_{RT}$  and  $V_{RB}$ . A separate power supply pin,  $DV_{DD}$ , sets the output logic levels for 3V or 5V interface.

This device operates from a single 5.0V supply. Power consumption from a 5.0V supply is typically 65mW at  $F_S=6$ MHz. For 3.3V power supply operation, refer to XRD64L18.

## ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRD6418BIQ	32-LEAD TQFP (7 x 7 x 1.4 mm)	-40°C to +85°C

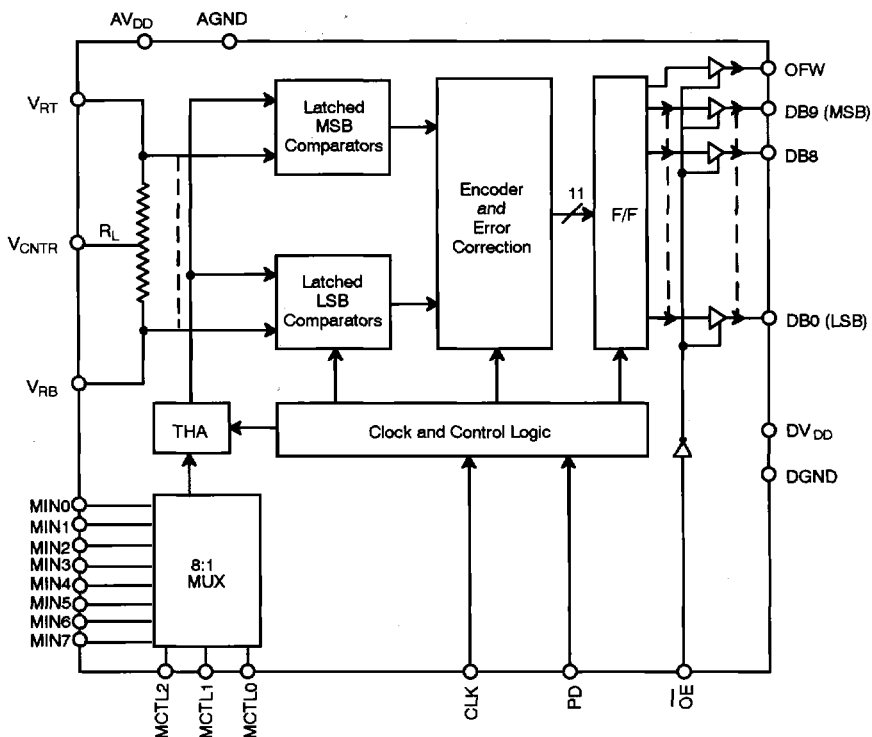
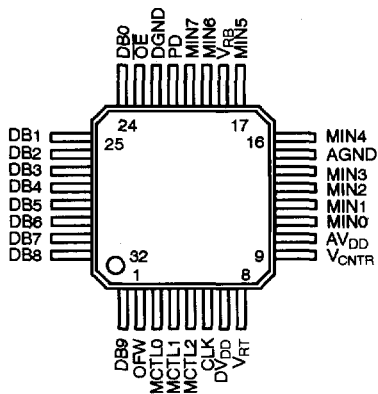


Figure 1. Simplified Block Diagram

## PIN CONFIGURATION



32 Lead TQFP (7 x 7 x 1.4 mm)

**PIN DESCRIPTION**

Pin #	Symbol	Description
1	DB9	Data Output Bit 9 (MSB)
2	OFW	Overflow Output
3	MCTL0	MUX Select Bit 0
4	MCTL1	MUX Select Bit 1
5	MCTL2	MUX Select Bit 2
6	CLK	Sampling Clock Input
7	DV <sub>DD</sub>	Power Supply (Digital)
8	V <sub>RT</sub>	Top of Reference Ladder
9	V <sub>CNTR</sub>	Center of Reference Ladder
10	AV <sub>DD</sub>	Analog Power Supply
11	MIN0	MUX Analog Signal Input 0
12	MIN1	MUX Analog Signal Input 1
13	MIN2	MUX Analog Signal Input 2
14	MIN3	MUX Analog Signal Input 3
15	AGND	Analog Ground
16	MIN4	MUX Analog Signal Input 4
17	MIN5	MUX Analog Signal Input 5
18	V <sub>RB</sub>	Bottom of Reference Ladder
19	MIN6	MUX Analog Signal Input 6
20	MIN7	MUX Analog Signal Input 7
21	PD	Power-Down Control
22	DGND	Ground (Digital)
23	$\overline{OE}$	Output Enable Control
24	DB0	Data Output Bit 0 (LSB)
25	DB1	Data Output Bit 1
26	DB2	Data Output Bit 2
27	DB3	Data Output Bit 3
28	DB4	Data Output Bit 4
29	DB5	Data Output Bit 5
30	DB6	Data Output Bit 6
31	DB7	Data Output Bit 7
32	DB8	Data Output Bit 8

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## ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified:  $AV_{DD} = DV_{DD} = 5.0V$ ,  $F_S = 6MHz$  (50% Duty Cycle),  
 $V_{RT} = 4.0V$ ,  $V_{RB} = 1.0V$ ,  $T_A = 25^\circ C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
<b>Key Features</b>						
n	Resolution	10			Bits	
$F_S$	Maximum Sample Rate	6	7.5		MSPS	
<b>DC Accuracy<sup>1</sup></b>						
DNL	Differential Non-Linearity	-1	$\pm 0.6$	1.0	LSB	Best Fit Line (Max INL - Min INL)/2
INL	Integral Non-Linearity		1	2	LSB	
EZS	Zero Scale Error	0	20	40	mV	$V_{IN}$ can swing from AGND to $AV_{DD}$ ; actual digitized range is set by $V_{RT}$ & $V_{RB}$ .
EFS	Full Scale Error		30	45	mV	
GE	Gain Error	-1	$\pm 0.5$	+1	% $F_S$	
$V_{INPP}$	DC Input Range	AGND		$AV_{DD}$	V	
<b>Reference Voltages</b>						
$V_{RT}$	Top Reference Voltage <sup>2</sup>	1.0	4	$AV_{DD}$	V	$V_{REF} = V_{RT} - V_{RB}$
$V_{RB}$	Bottom Reference Voltage <sup>2</sup>	AGND	1	$AV_{DD}-1$	V	
$V_{REF}$	Differential Ref. Voltage <sup>2</sup>	1.0	3	$AV_{DD}$	V	
$R_L$	Ladder Resistance	1,200	1,400	1,700	$\Omega$	
<b>Analog Input<sup>3</sup></b>						
$V_{IN}$	Input Voltage Range	$V_{RB}$		$V_{RT}$	V	$V_{RB}$ min. = AGND $V_{RT}$ max = $AV_{DD}$
BW	Input Bandwidth (-1dB) <sup>4</sup>		25		MHz	
$C_{IN}$	Input Capacitance Sample <sup>5</sup>		20		pF	CLK = High
$C_{IN}$	Input Capacitance Convert <sup>5</sup>		7		pF	CLK = Low
<b>Analog Multiplexer</b>						
$R_{ON}$	Switch Impedance <sup>3</sup>		60	120	$\Omega$	Function of Input Voltage
$R_{OFF}$	Switch Impedance <sup>3</sup>	5	10		M $\Omega$	
$T_{SW}$	Switching Time <sup>3</sup>		15		ns	$f_{IN} = 6MHz$
$X_t$	Crosstalk <sup>3</sup>		-80		dB	
<b>Conversion Character</b>						
$t_{AP}$	Aperture Delay <sup>3</sup>		8		ns	
$t_{AJ}$	Aperture Jitter <sup>3</sup>		30		ps	
<b>Dynamic</b>						
SNR	Signal-to-Noise Ratio					
	$F_{IN} = 100kHz$		56		dB	
SNDR	SNR and Distortion					
	$F_{IN} = 100kHz$		55		dB	

## ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
<b>Digital Inputs</b>						
$V_{IH}$	Digital Input High Voltage	2.0			V	Between AGND and AV <sub>DD</sub>
$V_{IL}$	Digital Input Low Voltage			0.8	V	
$I_{IN}$	DC Leakage Currents <sup>6</sup>					
	CLK, $\overline{OE}$ , PD		5		$\mu$ A	
	MCTL0, MCTL1, MCTL2		25	40	$\mu$ A	
	Input Capacitance		5		pF	
<b>Digital Outputs</b>						
$V_{OH}$	Output High Voltage	4.5			V	I <sub>SOURCE</sub> = 4mA
$V_{OL}$	Output Low Voltage			0.4	V	I <sub>SINK</sub> = 4mA
$I_{OZ}$	High-Z Leakage	-10		10	$\mu$ A	$\overline{OE}$ = high, or PD = high
$t_{DL}$	Data Valid Delay <sup>3</sup>		12	14	ns	C <sub>L</sub> = 15pF
$t_{DEN}$	Data Enable Delay <sup>3</sup>		14	16	ns	C <sub>L</sub> = 15pF
$t_{DZH}$	Data High-Z Delay <sup>3</sup>		4	6	ns	C <sub>L</sub> = 15pF
	Pipeline Delay (Latency)		2.5		cycles	Time delay between CLK and data output constant
<b>Power Supplies</b>						
$I_{DD(PD)}$	Power Down (I <sub>DD</sub> )		0.16	0.24	mA	PD = high, excluding current through reference ladder
AV <sub>DD</sub>	Operating Voltage <sup>7</sup>	4.5	5.0	5.5	V	
DV <sub>DD</sub>	Logic Power Supply <sup>8</sup>	2.7		5.5	V	
$I_{DD}$	Supply Current (I <sub>DD</sub> )		13	17	mA	PD = low

### Notes:

- <sup>1</sup> Tester measures code transitions by dithering the voltage of the analog input ( $V_{IN}$ ). The difference between the measured and the ideal code width ( $V_{REF}/1024$ ) is the DNL error. The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage. Accuracy is a function of the sampling rate (FS).
- <sup>2</sup> Specified values guarantee functionality. Refer to other parameters for accuracy.
- <sup>3</sup> Guaranteed. Not tested.
- <sup>4</sup> -1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
- <sup>5</sup> See  $V_{IN}$  equivalent circuit. Switched capacitor analog input requires driver with low output resistance.
- <sup>6</sup> All inputs have diodes to AV<sub>DD</sub> and AGND. Input DC currents will not exceed specified limits for any input voltage between AGND and AV<sub>DD</sub>.
- <sup>7</sup> The AGND pin is connected to the silicon substrate. DGND and AGND are connected through junction diodes. See logic output interface section.
- <sup>8</sup> See logic output interface section.

Specifications are subject to change without notice

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## ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)<sup>1, 2, 3</sup>

V <sub>DD</sub> to GND .....	+7.0V	Storage Temperature .....	-65 to +150°C
V <sub>RT</sub> & V <sub>RB</sub> .....	V <sub>DD</sub> +0.5 to GND -0.5V	Package Power Dissipation Rating to 75°C	
V <sub>IN</sub> .....	V <sub>DD</sub> +0.5 to GND -0.5V	TQFP .....	1000mW
All Inputs .....	V <sub>DD</sub> +0.5 to GND -0.5V	Derates above 75°C .....	14mW/°C
All Outputs .....	V <sub>DD</sub> +0.5 to GND -0.5V	Lead Temperature (Soldering 10 seconds) ..	+300°C

### Notes:

- <sup>1</sup> Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- <sup>2</sup> Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
- <sup>3</sup> V<sub>DD</sub> refers to AV<sub>DD</sub> and DV<sub>DD</sub>. GND refers to AGND and DGND.

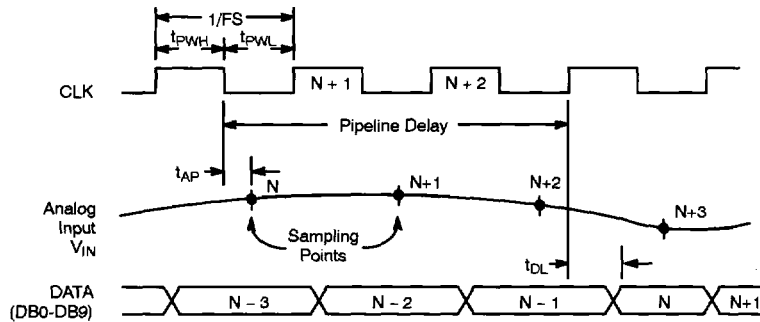


Figure 2. XRD6418 Timing Diagram

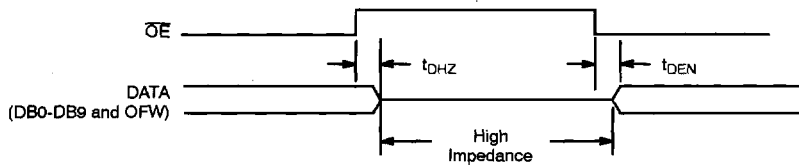
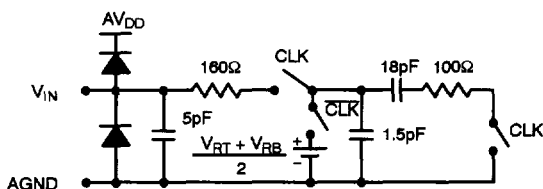


Figure 3. 3-State Timing Diagram

**THEORY OF OPERATION**

**V<sub>IN</sub> Analog Input**

This part has a switched-capacitor-type input circuit. The input impedance changes with the phase of the input clock. V<sub>IN</sub> is sampled at the high-to-low clock transition and the digital data changes at the low-to-high clock transition. The diagram Figure 4. shows an equivalent input circuit.



**Figure 4. Equivalent Input Circuit**

**OFW Overflow (Output)**

This signal indicates when the Analog Input (V<sub>IN</sub>) goes above V<sub>RT</sub>. The pin is normally at a low logic level. When V<sub>IN</sub> > V<sub>RT</sub>, OFW will go high and the data bits (DB0 – DB9) will show full scale (i.e., all 1s).

**OE Output Enable (Input)**

This signal controls the 3-state drivers on the digital outputs DB0 – DB9 and OFW. During normal operation, OE should be held low so that all outputs are enabled. When OE is driven high, DB0 – DB9 and OFW go into high impedance mode. This control operates asynchronous to the clock and will only control the output drivers. The internal output register will get updated if the clock is running while the outputs are in three-state mode.

OE	DB0-DB9	OFW
0	Enabled	Enabled
1	Three-Stated	Three-Stated

**Table 1. Output Enable**

**Power Supply Sequencing**

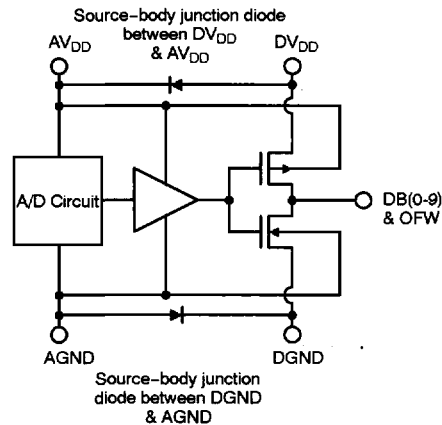
There are no power supply sequencing issues if DV<sub>DD</sub> and AV<sub>DD</sub> of the XRD6418 are driven from the same supply. Best parametric results, however, are obtained when DV<sub>DD</sub> and AV<sub>DD</sub> are driven from separate supplies. When DV<sub>DD</sub> and AV<sub>DD</sub> are driven separately, AV<sub>DD</sub> must come up at the same time or before DV<sub>DD</sub>, and go down at the same time or after DV<sub>DD</sub>. If the power supply sequencing in this case is not followed, then damage may occur to the product due to current flow through the source-body junction diodes between DV<sub>DD</sub> and AV<sub>DD</sub>. A low-threshold Schottky diode placed locally between DV<sub>DD</sub> and AV<sub>DD</sub> can prevent damage to the XRD6418.

**Logic Output Interface**

The digital output drive circuitry of the XRD6418 was designed to operate separately from the analog supplies. The DV<sub>DD</sub> pin of the XRD6418 is a separate power supply dedicated to the logic output drivers. DV<sub>DD</sub> is not connected internally with any of the other power supplies. Figure 5. illustrates the power supply circuitry of the XRD6418.

DV<sub>DD</sub> and DGND connect directly to the digital logic power of the user's system isolating the analog and digital power supplies and grounds. DGND is not common to the XRD6418 substrate. The XRD6418 substrate is common only to the packages' AGND pin. Best spectral performance is obtained when DV<sub>DD</sub> is lowered to 3.3V. See the power supply sequencing section if AV<sub>DD</sub> and DV<sub>DD</sub> are powered separately.

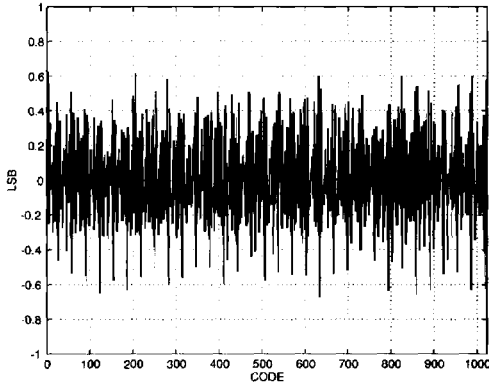
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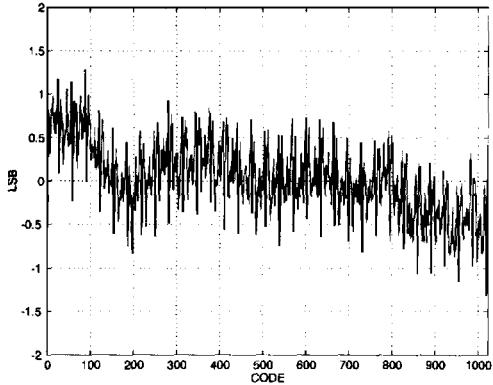
**Figure 5. XRD6418 ADC Power Supply Circuit Allows Separate  $AV_{DD}$  &  $DV_{DD}$  and Separate AGND & DGND**

## FINAL DESIGN CONSIDERATIONS

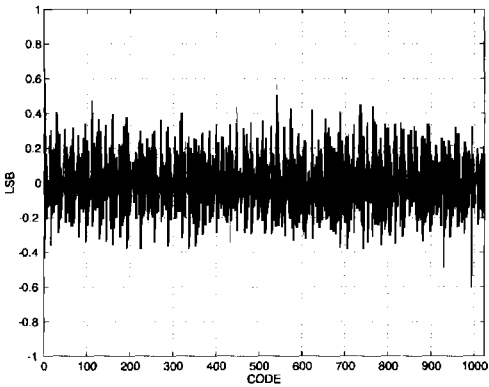
1. Be generous with analog and digital ground planes. Mirror the ground plane with the supply planes. Use a 5 mil power / ground plane separation if a four layer board can be used. The XRD6418 substrate is common to the packages' AGND pin only. DGND and  $DV_{DD}$  are separate supplies dedicated to the output logic drivers of the XRD6418. Connect DGND and  $DV_{DD}$  to the power planes of the system's digital logic.
2. Keep high frequency decoupling capacitors very close to the A/D pins and minimize the loop area included, so less flux will induce less noise.
3. Coupling between logic signals and analog circuitry can easily change a 10-bit system into an 8-bit system or worse. Completely separate them. Watch for coupling opportunities from other sources not immediately associated with the A/D. Don't use switching power supplies in adjacent locations, for example.
4. The DC performance of the XRD6418 is optimized with rise and fall times of CLK edges limited to greater than or equal to 6ns. A resistor in series with the CLK input pin can combine with parasitic capacitance to limit rise and fall times. Select a low jitter clock with a 50% duty cycle for best spectral results.
5. Use very linear passive components in the signal path.
6. Select a driving op amp whose noise, speed, and linearity fits the application. Use a resistor to decouple the output of the driving op amp from the switching input capacitance of the XRD6418.
7. DNL and INL performance is optimized when the  $V_{RB}$  input of the XRD6418 is buffered. If  $V_{RB}$  is connected to the PCB ground plane, it is subject to the noise and ground bounce in that plane. For example,  $V_{RB}$  could be buffered to 50mV above ground and still have a wide reference voltage range set by connecting  $V_{RT}$  to a voltage near  $AV_{DD}$ .
8. Use 50 or 100 $\Omega$  resistors to isolate the XRD6418 digital output pins from a latch or bus connection. This protects the output drivers and reduces the effects of high-speed switching logic signals from degrading the ADC performance. Layout the latch or digital buffers as close to the ADC as possible to minimize trace length.



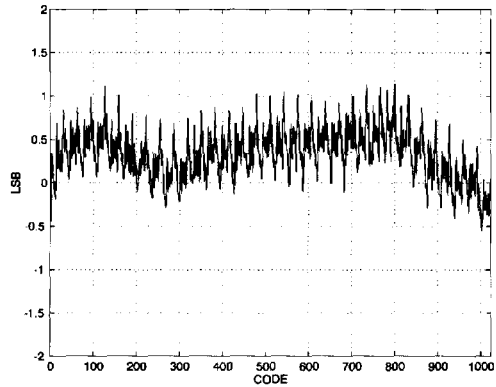
**Figure 6. XRD6418, DNL @ 5MSPS**  
 $DV_{DD} = 5V, AV_{DD} = 5V, V_{RT} = 4V, V_{RB} = 1V$



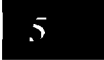
**Figure 7. XRD6418, INL @ 5MSPS**  
 $DV_{DD} = 5V, AV_{DD} = 5V, V_{RT} = 4V, V_{RB} = 1V$

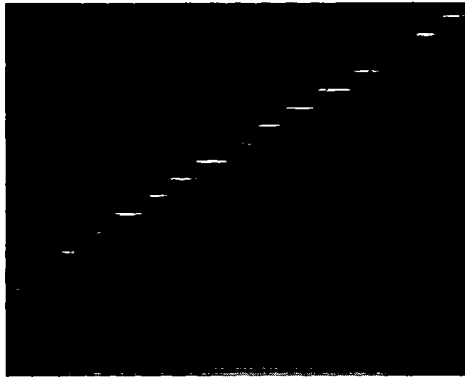


**Figure 8. XRD6418, DNL @ 5MSPS**  
 $DV_{DD} = 3V, AV_{DD} = 5V, V_{RT} = 4.5V, V_{RB} = 0.5V$

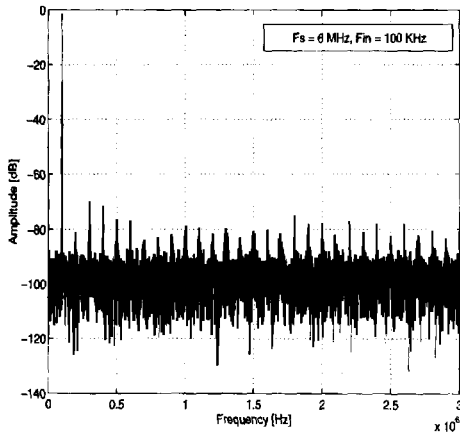


**Figure 9. XRD6418, INL @ 5MSPS**  
 $DV_{DD} = 3V, AV_{DD} = 5V, V_{RT} = 4.5V, V_{RB} = 0.5V$

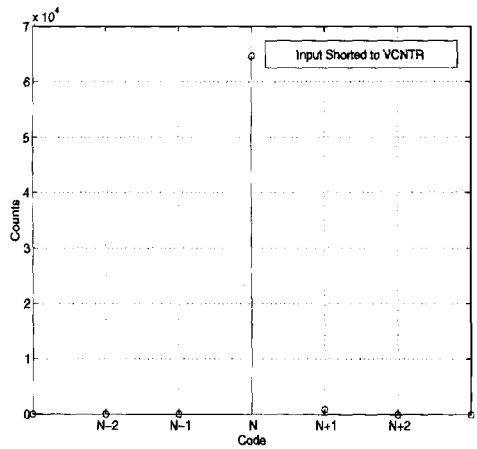




**Figure 10. Crossplot Staircase Output**  
 CLK = (6MSPS,  $t_{r1} = 10\text{ns}$ ),  $V_{REF} = 4\text{V}$



**Figure 11. XRD6418 Spectral Performance**



**Figure 12. XRD6418 Output Noise Histogram**

MCTL2	MCTL1	MCTL0	Selected Analog Input
0	0	0	MIN0
0	0	1	MIN1
0	1	0	MIN2
0	1	1	MIN3
1	0	0	MIN4
1	0	1	MIN5
1	1	0	MIN6
1	1	1	MIN7

**Table 2. Truth Table for Analog Input Selection**

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PD	Device Status
1	Off (Not Operating)
0	On (Operating)

**Table 3. Power Down**