TDC1046
Monolithic Video A/D Converter

6-Bit, 25 Msps

Description

The TDC1046 is a 25 Msps (Megasample per second) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12.5 MHz into 6-bit digital words. Use of a sample-and-hold circuit is not necessary for operation of the TDC1046. All digital inputs and outputs are TTL compatible.

The TDC1046 consists of 63 clocked latching comparators, encoding logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

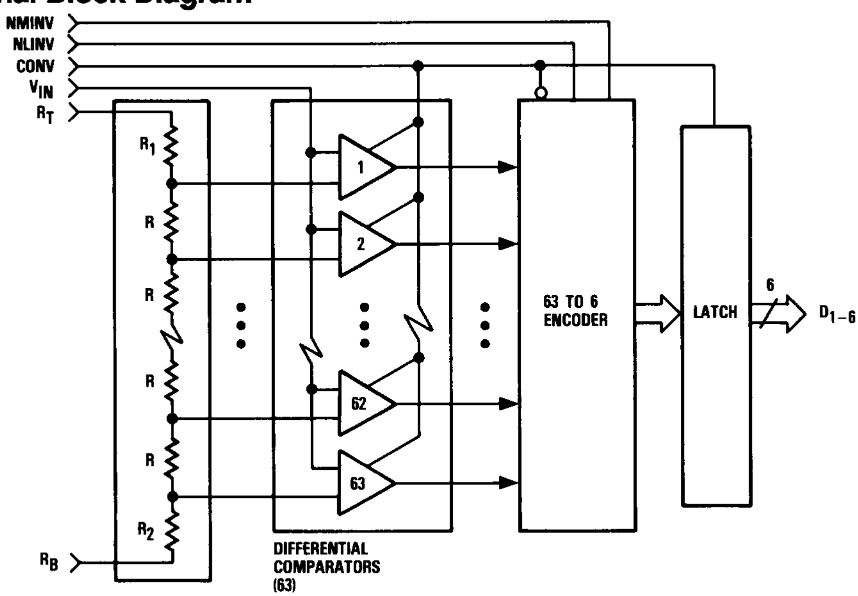
Features

- 6-bit resolution
- 1/4 LSB linearity
- Sample-and-hold circuit not required
- TTL compatible
- 25 Msps conversion rate
- Selectable output format
- Available in an 18-pin CERDIP
- Low cost
- Low analog inut capacitance
- Available per Standard Military Drawing

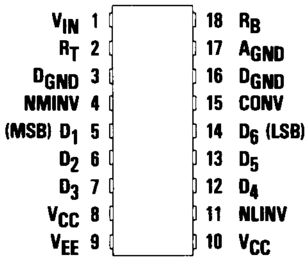
Applications

- Low-cost video digitizing
- Medical imaging
- Data acquisition
- TV special effects
- Video simulators
- Radar data conversion

Functional Block Diagram



Pin Assignments



18 Pin CERDIP – B8 Package

Functional Description

General Information

The TDC1046 has three functional sections: a comparator array, encoding logic, and output latches. The comparator array compares the input signal with 63 reference voltages to produce an N-of-63 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-63 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV. The output latch holds the output constant between updates.

Power

The TDC1046 operates from two supply voltages, +5.0V and −5.2V. The return for I_{CC}, the current drawn from the +5.0V supply, is D_{GND}. The return for I_{EE}, the current drawn from the −5.2V supply, is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1046 converts analog signals in the range $V_{RB} \leq V_{IN} \leq V_{RT}$ into digital form. V_{RB} (the voltage applied to R_B at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to R_T at the top of the reference resistor chain) should be between +0.1V and −1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain ($V_{RT} - V_{RB}$) must be between 0.8V and 1.2V. The nominal voltages are $V_{RT} = 0.00V$ and $V_{RB} = -1.00V$. These voltages may be varied dynamically up to 12.5MHz. Due to variation in the reference currents with clock and input signals, R_T and R_B should be low-impedance-to-ground points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are exercised dynamically (as in an Automatic Gain Control circuit), a low-impedance reference source is required.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the ***Output Coding Table***. These pins are active LOW as signified by the prefix "N" in the signal name. They may be tied to V_{CC} for a logic "1" and D_{GND} for a logic "0."

Convert

The TDC1046 requires a CONVert (CONV) signal. A sample is taken (the comparators are latched) within 5ns (t_{STO}) after a rising edge on the CONV pin. This time is t_{STO}, Sampling Time Offset. The 63 to 6 encoding is performed on the falling edge of the CONV signal. The coded result is transferred to the output latches on the next rising edge. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal.

Analog Input

The TDC1046 uses strobed latching comparators which cause the input impedance to vary with the signal level, as comparator input transistors are cut-off or become active. For optimal performance, the source impedance of the driving circuit must be less than 50 Ohms. The input signal will not damage the TDC1046 if it remains within the range of V_{EE} to +0.5V. If the input signal is at a voltage between V_{RT} and V_{RB}, the output will be a binary number between 0 and 63 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1046 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. Data is guaranteed to be valid after a maximum delay time (t_D) after the rising edge of CONV. For optimum performance, 2.2 kOhm pull-up resistors are recommended.

Package Interconnections

Signal Type	Signal Name	Function	Value	B8 Package Pins
Power	V_{CC}	Positive Supply Voltage	+5.0V	8, 10
	V_{EE}	Negative Supply Voltage	−5.2V	9
	D_{GND}	Digital Ground	0.0V	3, 16
	A_{GND}	Analog Ground	0.0V	17
Reference	V_{RT}	Reference Resistor (Top)	0.0V	2
	V_{RB}	Reference Resistor (Bottom)	−1.0V	18
Controls	NMINV	Not Most Significant Bit INVert	TTL	4
	NLINV	Not Least Significant Bit INVert	TTL	11
Convert	CONV	Convert	TTL	15
Analog Input	V_{IN}	Analog Signal Input	0V to −1V	1
Outputs	D_1	MSB Output	TTL	5
	D_2		TTL	6
	D_3		TTL	7
	D_4		TTL	12
	D_5		TTL	13
	D_6	LSB Output	TTL	14

Output Coding Table [1]

Range	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV=1	0	0	1
15.8730mV Step	NLINV=1	0	1	0
0.0000V	000000	111111	100000	011111
−0.0159V	000001	111110	100001	011110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.4921V	011111	100000	111111	000000
−0.5079V	100000	011111	000000	111111
−0.5238V	100001	011110	000001	111110
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
−0.9841V	111110	000001	011110	100001
−1.0000V	111111	000000	011111	100000

Note: 1. Voltages are code midpoints when calibrated (see *Calibration* section).

Figure 1. Timing Diagram

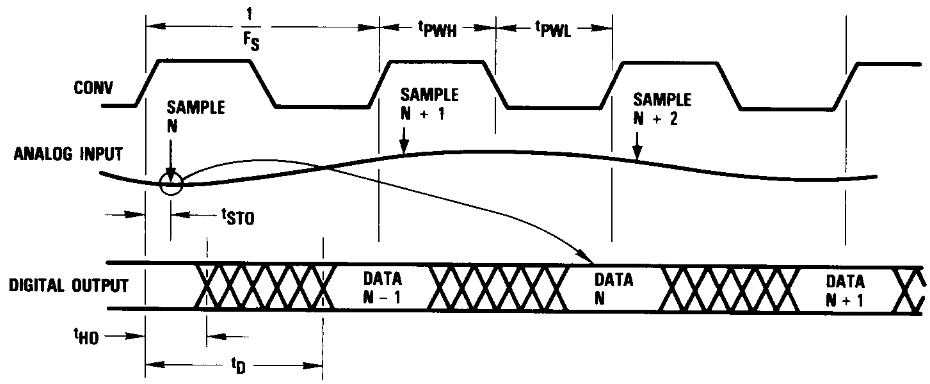
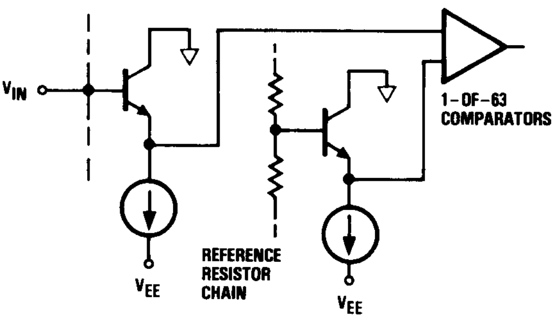
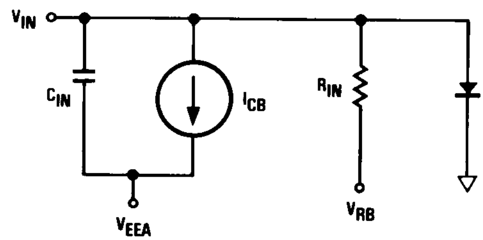


Figure 2. Simplified Analog Input Equivalent Circuit





C_{IN} IS A NONLINEAR JUNCTION CAPACITANCE
V_{RB} IS A VOLTAGE EQUAL TO THE VOLTAGE ON PIN R_B

Figure 3. Digital Input Equivalent Circuit

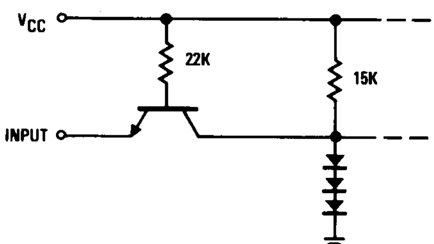
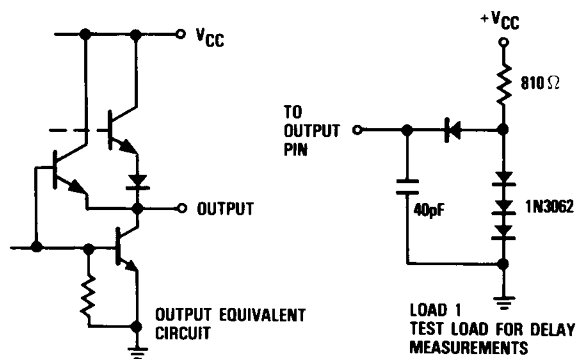


Figure 4. Output Circuits



Absolute maximum ratings (beyond which the device will be damaged)[1]

Supply voltages

V_{CC} (measured to D_{GND})	−0.5 to +7.0V
V_{EE} (measured to A_{GND})	+0.5 to −7.0V
A_{GND} (measured to D_{GND})	−0.5 to +0.5V

Input voltages

CONV, NMINV, NLINV (measured to D_{GND})	−0.5 to +5.5V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})	+0.5 to V_{EE}
V_{RT} (measured to V_{RB})	+1.2 to −1.2V

Output

Applied voltage (measured to D_{GND})	−0.5 to 5.5V[2]
Applied current, externally forced	−1.0 to 6.0mA[3,4]
Short circuit duration (single output in high state to ground)	1 sec

Temperature

Operating, case	−55 to +125°C
junction	+175°C
Lead, soldering (10 seconds)	+300°C
Storage	−65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating conditions

		Temperature Range						
		Standard			Extended			
Parameter		Min	Nom	Max	Min	Nom	Max	Units
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width (LOW)	15			15			ns
t_{PWH}	CONV Pulse Width (HIGH)	17			17			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			−0.4			−0.4	mA
V_{RT}	Most Positive Reference Input[1]	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Input[1]	−0.9	−1.0	−1.1	−0.9	−1.0	−1.1	V
$V_{RT}-V_{RB}$	Voltage Reference Differential	0.8		1.2	0.8		1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
T_A	Ambient Temperature, Still Air	0		70				
T_C	Case Temperature				−55		125	°C

Note:

1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specified range.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Standard Max	Extended Min	Extended Max	Units
I_{CC}	Positive Supply Current	V_{CC} = MAX, static[1]		20		25	mA
I_{EE}	Negative Supply Current	V_{EE} = MAX, static[1]					
		T_A = 0°C to 70°C		-95			mA
		T_A = 70°C		-75			mA
		T_C = -55°C to 125°C				-150	mA
		T_C = 125°C				-75	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = NOM		10		15	mA
R_{REF}	Total Reference Resistance	$V_{RT} - V_{RB}$ = MAX	100		66		Ohms
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = NOM, V_{IN} = V_{RB}	40		40		kOhms
C_{IN}	Input Capacitance			30		30	pF
I_{CB}	Input Constant Bias Current	V_{EE} = MAX		105		180	μA
I_{IL}	Input Current, Logic LOW	V_{CC} = MAX, V_I = 0.5V CONV		-0.4		-0.6	mA
		NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = MAX, V_I = 2.4V		50		50	μA
I_I	Input Current, Max Input Voltage	V_{CC} = MAX, V_I = 5.5V		1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = MIN, I_{OL} = 2 mA		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = MIN, I_{OH} = MAX	2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, One pin to ground, one second duration, output HIGH		-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz		15		15	pF

Note:

1. Worst case, all digital inputs and outputs LOW.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Standard Max	Extended Min	Extended Max	Units
F_S	Maximum Conversion Rate	V_{CC} = MIN, V_{EE} = MIN	25		25		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = MIN, V_{EE} = MIN		5		10	ns
t_D	Output Delay	V_{CC} = MIN, V_{EE} = MIN, Load 1		30		35	ns
t_{HO}	Output Hold Time	V_{CC} = MAX, V_{EE} = MAX, Load 1	5		5		ns

System performance characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Standard Max	Extended Min	Extended Max	Units
E_{LI}	Linearity Error Integral, Independent	V_{RT}, V_{RB} = Nom		0.4		0.4	%
E_{LD}	Linearity Error Differential			0.4		0.4	%
CS	Code Size	V_{RT}, V_{RB} = Nom	50	150	50	150	% Nominal
E_{OT}	Offset Error, Top	$V_{IN} = V_{RT}$		+50		+50	mV
E_{OB}	Offset Error, Bottom	$V_{IN} = V_{RB}$		−30		−30	mV
T_{CO}	Temperature Coefficient (Offset Voltage)			±20		±20	μV/°C
BW	Bandwidth, Full Power Input		12.5		12.5		MHz
t_{TR}	Transient Response, Full-Scale			10		10	ns
SNR	Signal-to-Noise Ratio	12.5MHz Bandwidth, 25Msps Conversion Rate					
	Peak Signal/RMS Noise	1MHz Input	42		36		dB
		12.5MHz Input	40		32		dB
	RMS Signal/RMS Noise	1MHz Input	33		33		dB
		12.5MHz Input	31		29		dB
E_{AP}	Aperture Error			30		30	ps

Calibration

To calibrate the TDC1046, adjust V_{RT} and V_{RB} to set the 1st and 63rd thresholds to the desired voltages. In the *Functional Block Diagram*, note that R_1 is greater than R, ensuring calibration with a positive voltage on R_T. Assuming a 0V to −1V desired range, continuously strobe the converter with −0.0079V on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply −0.9921V and adjust V_{RB} for toggling between codes 62 and 63. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with a buffer offset control. R_B is a convenient point for gain adjust that is not in the analog signal path. These techniques are employed in *Figure 5*.

Typical Interface Circuit

The TDC1046 does not require a special input buffer amplifier to drive the analog input because of its low analog input capacitance. A terminated low-impedance transmission line (<100 Ohms) connected to the V_{IN} terminals of the TDC1046 is sufficient if the input voltage levels match those of the A/D converter.

However, many driver circuits lack sufficient offset control, drive current, or gain control. The *Typical Interface Circuit (Figure 5)* shows a simple buffer amplifier and voltage reference circuit that may be used with the TDC1046. U2 is a wide-band operational amplifier with a gain factor of −2. A small value resistor, R12, serves to help isolate the input capacitance of the A/D converter from the amplifier output and insure frequency stability. The pulse and frequency response of the buffer amplifier are optimized by variable capacitor C12.

The reference voltage for the TDC1046 is generated by amplifier U3 and PNP transistor Q1 which supplies the reference current. System gain is adjusted by varying R9 which controls the reference voltage level to the A/D converter.

Input voltage range and input impedance for the circuit are determined by resistors R1 and R2. Formulas for calculating values for these input resistors are:

$$R1 = \frac{1}{\left(\frac{2VR}{Z_{IN}}\right) - \frac{1}{1000}}$$

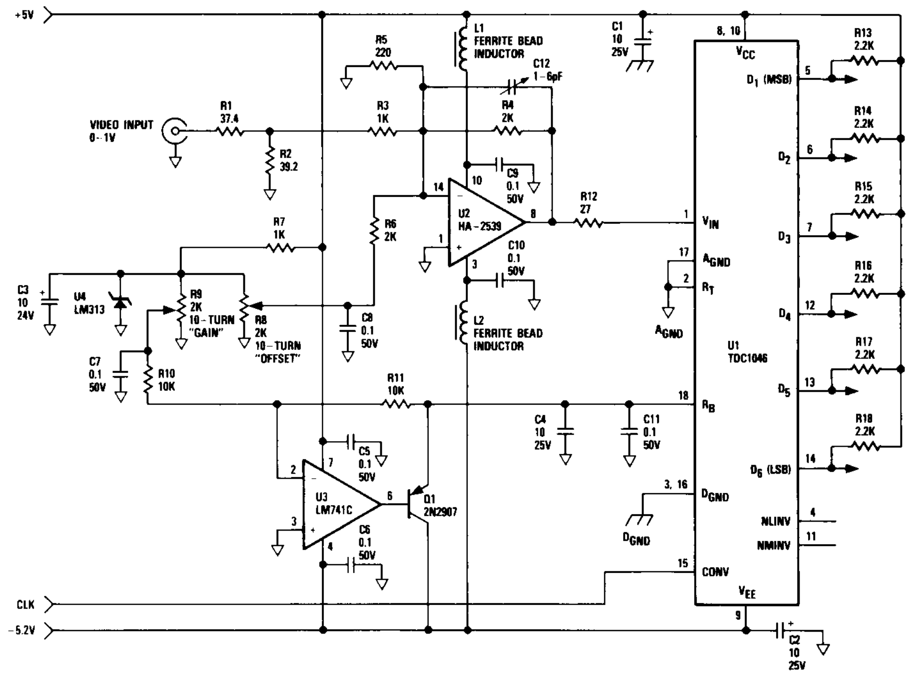
Typical Interface Circuit (cont.)

and

$$R2 = Z_{IN} - \left(\frac{1000\ R1}{1000 + R1}\right)$$

where VR is the input voltage range of the circuit, Z_{IN} is the input impedance of the circuit, and the constant 1000 comes from the value of R3. As shown, the circuit is set up for 1Vp-p 75 Ohm video input.

Figure 5. Typical Interface Circuit



Standard Military Drawing

These devices are also available as products manufactured, tested, and screened in compliance with Standard Military Drawings (SMDs). The nearest vendor equivalent product is shown below; however, the applicable SMD is the sole controlling document defining the SMD product.

Standard Military Drawing	Nearest Equivalent TRW Product No.	Package
5962-87786-01VA	TDC1046B8V	18 Pin CERDIP

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1046B8C	STD–T_A=0°C to 70°C	Commercial	18 Pin CERDIP	1046B8C
TDC1046B8V	EXT–T_C= –55°C to 125°C	MIL-STD-883	18 Pin CERDIP	1046B8V
5962-87786-01VA	EXT–T_C= –55°C to 125°C	Per Standard Military Drawing	18 Pin CERDIP	5962-87786 01VA

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