Integrated Device Technology, Inc.

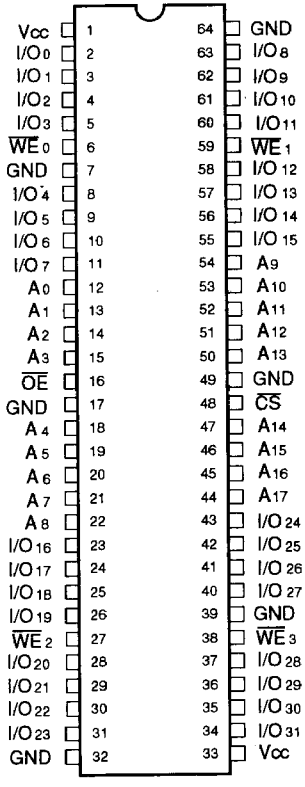
256K x 32 BiCMOS/CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4077

FEATURES:

- High density 8 megabit static RAM module
- Low profile 64 pin sidebraze DIP (Dual In-line Package)
- Very fast access time: 15ns (max.)
- Surface mounted leadless chip carrier (LCC) components on an multilayer ceramic substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Multiple GND pins and decoupling capacitors for maximum noise immunity

PIN CONFIGURATION



2814 drw 01

DIP
TOP VIEW

DESCRIPTION:

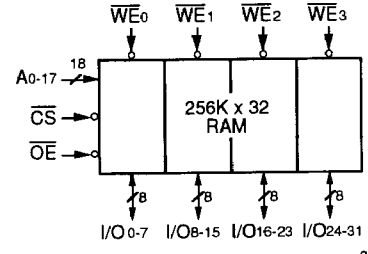
The IDT7M4077 is a 256K x 32 static RAM module constructed on a multilayer ceramic substrate using eight 256Kx4 static RAMs in leadless chip carrier (LCC) packages. Availability of four write enable lines (one for each group of two RAMs) provides byte write capability. The IDT7M4077 is available with access time as fast as 15ns with minimal power consumption.

The IDT7M4077 is packaged in a 64 pin sidebraze DIP (Dual In-line Package). The DIP configuration allows 64 pins to be placed on a package 3.5 inches long, 0.6 inches wide and 0.31 inches thick.

All inputs and outputs of the IDT7M4077 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2814 drw 02

PIN NAMES

I/O0–31	Data Inputs/Outputs
A0–17	Addresses
CS	Chip Select
WE0–3	Write Enables
OE	Output Enable
Vcc	Power
GND	Ground

2814 tbl 01

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2814 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2814 tbl 03

1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2814 tbl 04

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
$C_{I/O}$	I/O Capacitance (Data)	$V_{(IN)}$ = 0V	15	pF
C_{IN1}	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	90	pF
C_{IN2}	Input Capacitance ($\overline{WE}$)	$V_{(IN)}$ = 0V	35	pF

NOTE: 2814 tbl 05

1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2814 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI}\|$	Input Leakage ($\overline{WE}$)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2814 tbl 07

Symbol	Parameter	Test Conditions	7M4077(1, 2) Military Max.	7M4077(1, 2) Comm. Max.	7M4077(3) Military Max.	7M4077(3) Comm. Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL}, V_{CC} = Max.; Output Open	1760	1600	1500	1200	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	720	600	600	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	400	320	320	80	mA

2814 tbl 08

NOTES:

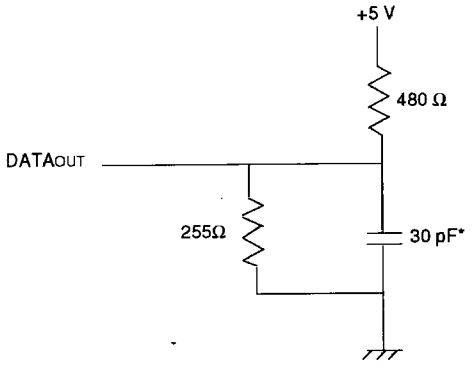
1. Preliminary specifications only.
2. 15-20ns versions only.
3. 25-55ns versions only.

7-15-2

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

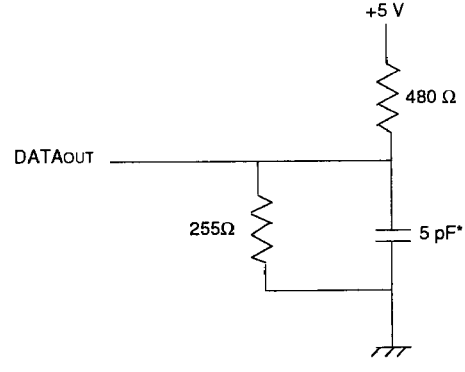
2814 tbl 09



2814 drw 03

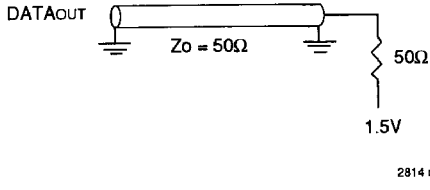
*Includes scope and jig.

Figure 1. Output Load



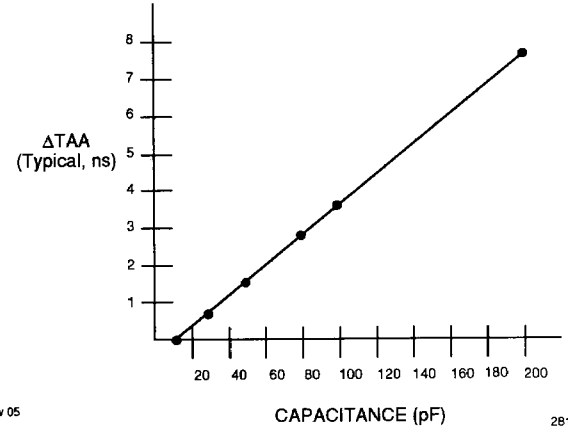
2814 drw 04

Figure 1. Output Load
(for tOLZ, tCHZ, tCLZ, tWHZ, tOW)



2814 drw 05

Figure 3. Alternate Output Load



2814 drw 06

Figure 4. Alternate Lumped Capacitive Load, Typical Derating

7-15-3

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	7M4077SxxC, 7M4077SxxCB						Unit
		-15[2]		-17[2]		-20[2]		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	15	—	17	—	20	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	—	20	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	8	—	8	—	10	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	8	—	8	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	15	—	17	—	20	—	ns
t_{CW}	Chip Select to End of Write	12	—	15	—	17	—	ns
t_{AW}	Address Valid to End of Write	12	—	15	—	17	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	17	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	8	—	10	—	13	ns
t_{DW}	Data to Write Time Overlap	10	—	10	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	ns

2814 tbl 10

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	7M4077SxxC, 7M4077SxxCB										Unit
		-25		-30		-35		-45		-55		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	3	—	3	—	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	15	—	18	—	23	—	25	—	25	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	17	—	20	—	25	—	30	—	30	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	12	—	15	—	20	—	25	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	—	45	—	55	ns
Write Cycle												
t_{WC}	Write Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	30	—	40	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	18	—	20	—	23	—	25	—	25	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	25	—	30	—	30	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

2814 tbl 11

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. Preliminary specifications only.

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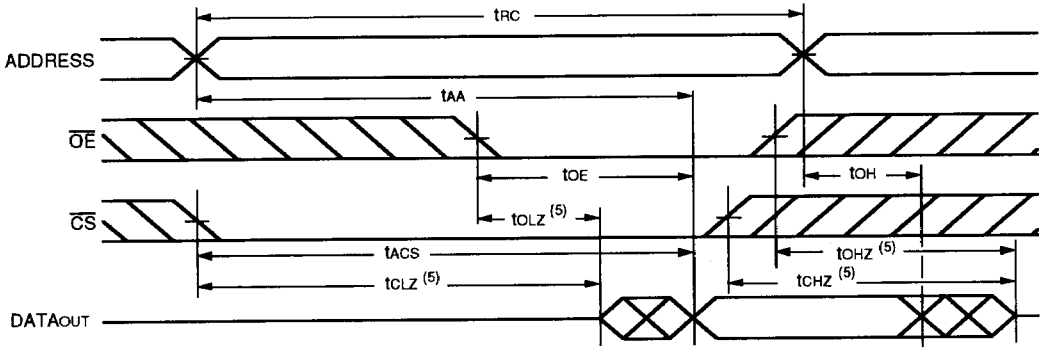
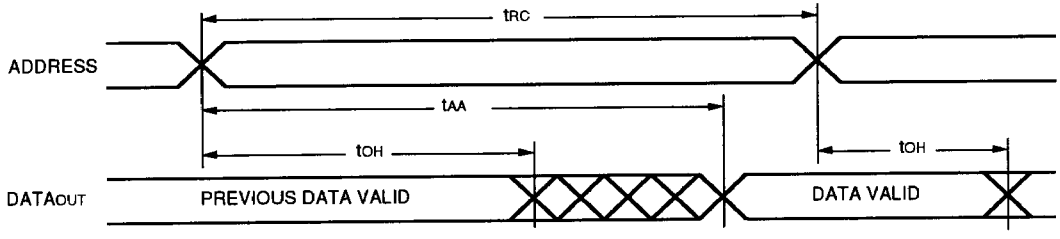
TIMING WAVEFORM OF READ CYCLE NO. 1(1,3,4)



2814 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2814 drw 08

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

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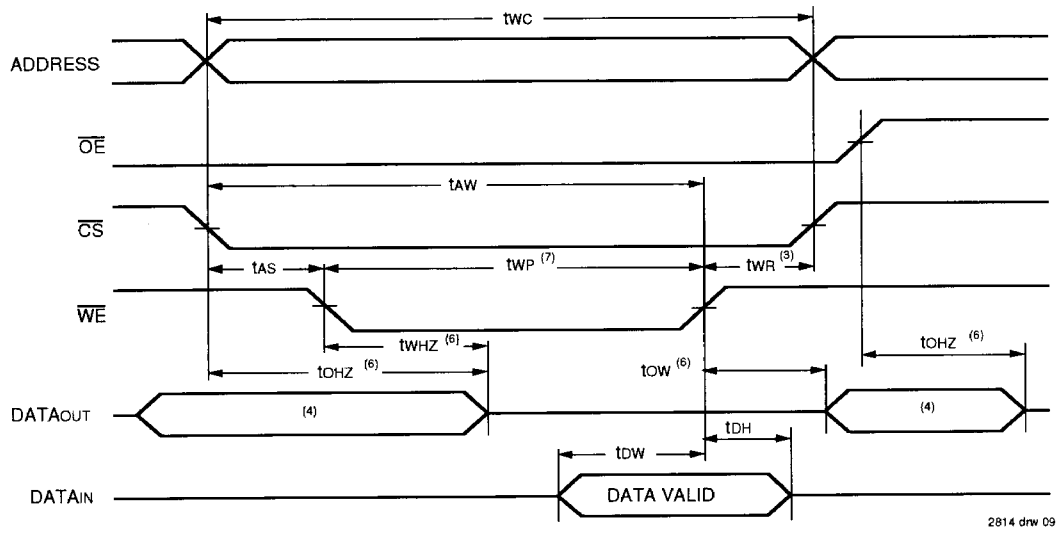
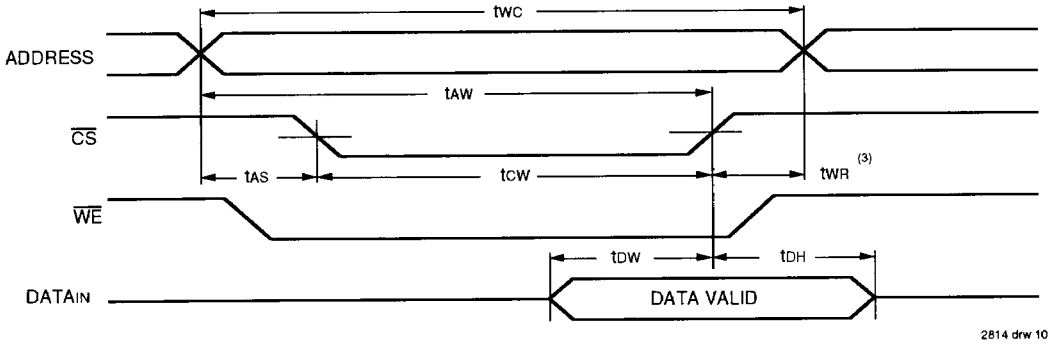
7-15-6

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,2,3,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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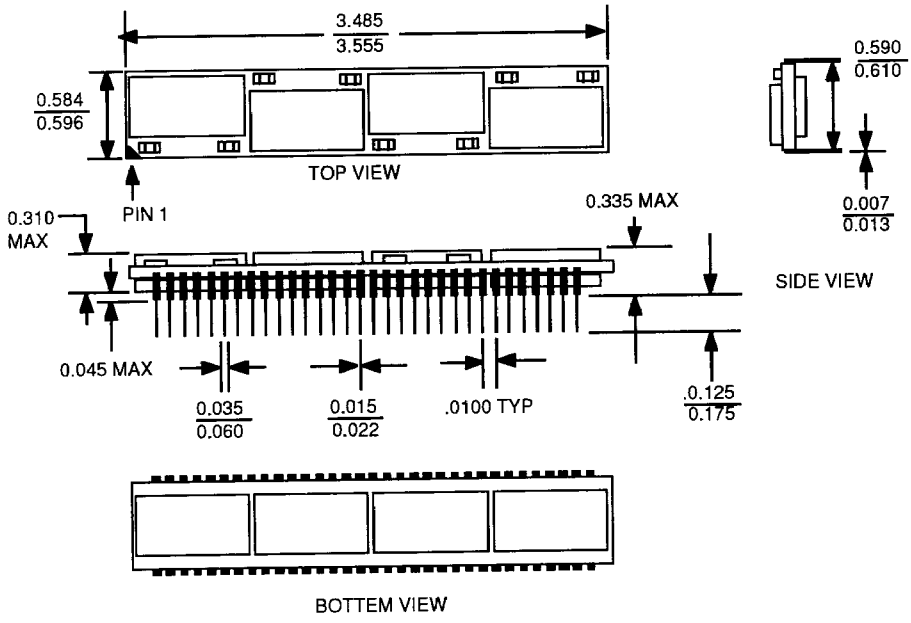
PACKAGE DIMENSIONS



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