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ISO 9002
Registered

PRELIMINARY

MSISAM27LS00

256-Bit TTL Compatible CMOS RAM

DISTINCTIVE CHARACTERSTICS

- High Speed
- Internal CMOS Circuitry for Optmium
  Performance over temperature and voltage
- Available with Tri-state outputs

GENERAL DESCRIPTION

The MSISAM27LS00 is a fully decoded CMOS Static Random Access Memory implemented in 1.2 m technology. This is fully compatible with the bipolar AM27LS00 but offers significant improvement in speed and power dissipation. The MSISAM27LS00 is organised as 256-words by 1 bit memory with an 8-bit binary address field and separate data in and data out lines. The memory has 3 active LOW chipselect inputs and threestate outputs. All inputs are buffered to present an input load of 0.5 TTL unit loads

Read/Write operation is controlled by an active LOW write enable input. When the write-enable is LOW and the chip is selected the data in the data input pin is written into the location specified by the address inputs. The output is disabled during the period nWE is LOW. READ operation is done by having the chip selected and nWE high. Data stored in the location specified by the address inputs is read out and appears at the Data Output pin.

MODE SELECT TABLE

Input nCS	nWE	DI	Data Output Status DO(tn+1)	Mode
X	X	X	Output Disabled	No Selection
L	L	L	Disabled	Write "0"
L	L	H	Disabled	Write "1"
L	H	X	Selected Bit	Read

H = HIGH
L = LOW
X = DON'T CARE

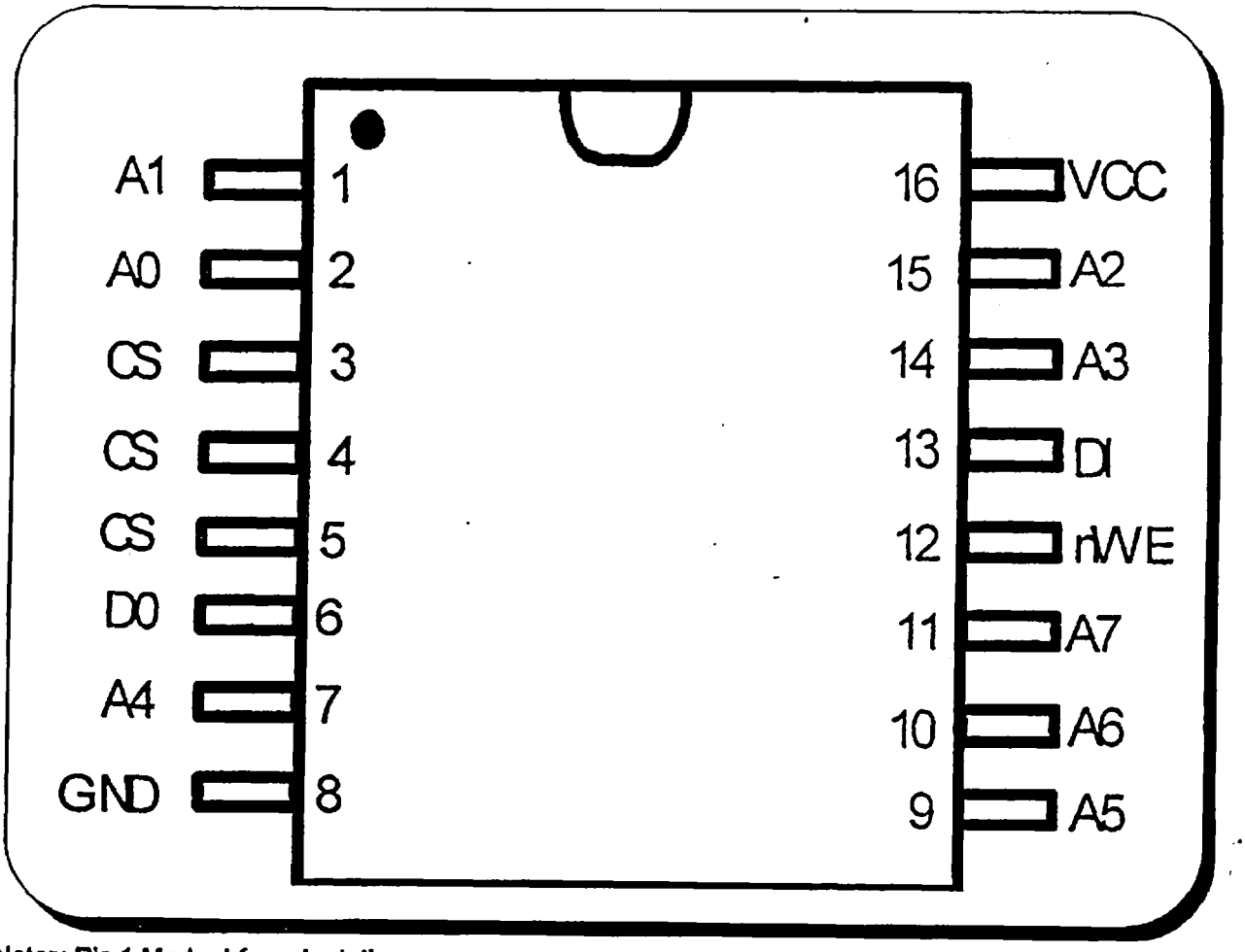
PRODUCT SELECTOR GUIDE

Part Number	MSISAM27LS00APC	MSISAM27LS00PC
Access time	35 ns	45 ns
Temperature range	0-70 deg C	0-70 deg C

Note: For burn-in order with "B" as the last letter after PC and APC

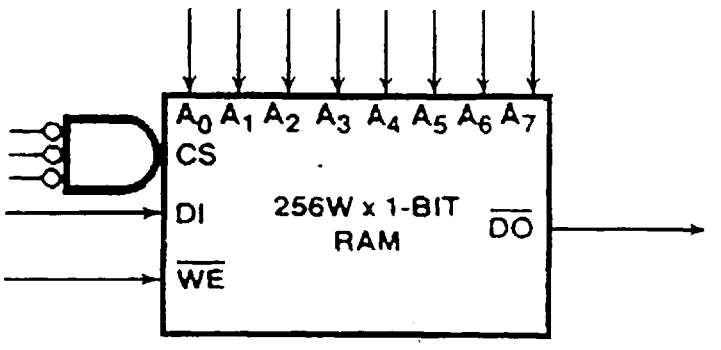
MSISS003

CONNECTION DIAGRAM



Notes: Pin 1 Marked for orientation.
CS & nWE are true when LOW.

LOGIC SYMBOL



LS00020

V_{CC} = Power Supply
GND = Ground

ABSOLUTE MAXIMUM RATINGS

Storage Temperature———— -55 to +150° C

Ambient Temperature
with Power Applied———— -10 to +85 °C

Supply Voltage to Ground potential
(pin 16 to pin 8 continuous)—— -0.5 V to +7.0 V

DC Voltage applied to Outputs
for High Output state———— -0.5V to VCC^{max}

DC Input Voltage———— -0.5V to VCC

Output Current, into outputs———— 30 ma

DC Input Current———— -30 ma to +5 ma

OPERATING RANGES

Temperature———— 0 to 70 ° C

Supply Voltage———— +4.75 V to 5.25 V

Operating ranges define those limits between which functionality of the device is guaranteed

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits are not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

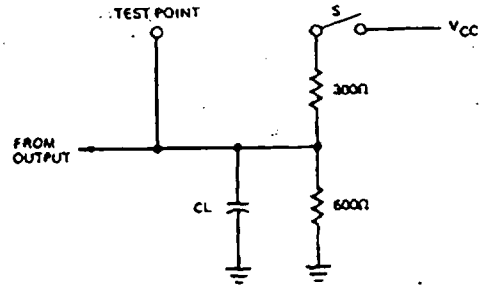
DC CHARACTERSTICS (over operating range unless otherwise specified)

Parameter Symbol	Parameter Description	Test Conditions	Min	Tyo (Note 1)	Max	Units
VOH	Output High Voltage	VCC=Min IOH = -5.2 ma Vin=VIH or VIL	2.4	3.2		Volts
V_{OL}	Output LOw Voltage	VCC=Min IOL= 16 ma VIN = VIH or VIL		0.3	0.45	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input logical HIGH Voltage for all inputs	2			Volts
V_{IL}	Input LOW Voltage	Guaranteed linput Logical LOW Voltage for all inputs			0.8	Volts
I_{IH}	Input High Current	Vcc = Max, Vin =2.7V		<1	20	uA
IIL	Input Low Current	Vcc= Max, Vin = 0.40V		< 1 uA	-0.25	mA
Isc (Note 2)	Output Short Circuit Current	Vcc + Max, Vout = 0.0V	-40	-90	-150	mA
Icc	Power Supply Current	All Inputs = Gnd 'A' Version Vcc = Max Standard		< 1 <1	115 70	mA
VcL	Input Clamp Voltage	Vcc = Min, Iin = -18mA		-0.850	- 1.2	Volts
I CEX	Output Leakage Current	Vcs = VIH, or VnWE = VIL, VOUT = 2.4V Vcs = VIH, or VnWE = VIL, VOUT=0.4V, Vcc= Max (Note 2)	 -30	0 0	30	UA UA

Notes: 1. Typical limits are at VCC = 5.0V and TA= 25 Deg.C
2. This applies to three state devices only.
3. These are aabsolute voltages with respuct to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Operating Specification with adequate time for temperature stabilisation and transverse air flow exceeding 400 linear feet per minute.

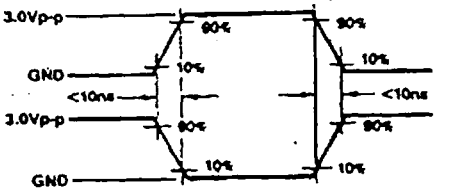
Conformance testing performed instantaneously where TA=TC=TJ== OJA= 44-59Deg. c/w (with moving air) for ceramic DIPs.
OjC=10-170 c/w for flat pacck or leadless chip carriers.

SWITCHING TEST* CIRCUIT



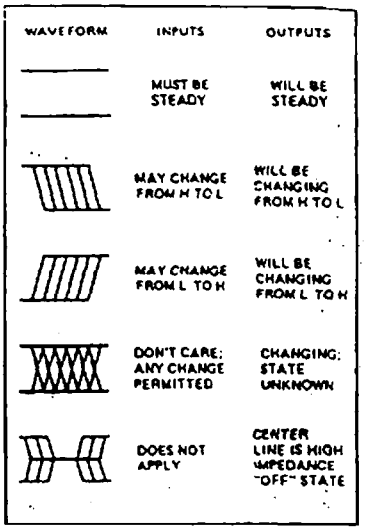
TC000210

SWITCHING TEST WAVEFORM



TW000030

KEY TO SWITCHING WAVEFORMS



SWITCHING CHARACTERSTICS (Over operating Range unless otherwise specified)

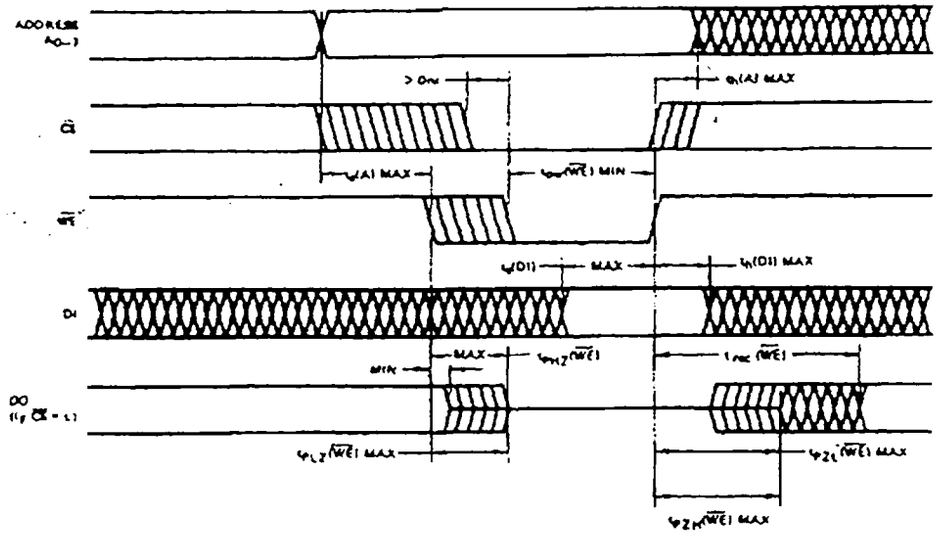
No	Parameter Symbol	Parameter Description	MSIS27C00A Min	Max	MSIS27C00 Min	Max	Units
1 2	t_{PLH} t_{PHL}	Delay from Address to output	-	35		45	nS
3	t_{PZH}(nCS) t_{PZL} (nCS)	Delay from chip selcet(LOW) to Active output and correct data		25		25	ns
4	t_{PZH}(nWE) t_{PZL} (nWE)	Dealy from write enable (HIGH) to Active output and Correct data		35		45	ns
5	t_s(A)	Setup Time Address(Prior to initiation of Write)	0		0		ns
6	t_h(A)	Hold time address(after termination of Write)	0		0		ns
7	t_s(DI)	Setup Time Data Input (Prior to termination of Write)	25		30		ns
8	t_h(DI)	Hold Time Data Input (After termination of Write)	0		0		ns
9	t_{pw}((nWE)	Minimum Write Eanble Pulse Width to Inusre Write	25		30		ns
10	t_{PHZ}(nCS) t_{PLZ}(nCS)	Delay from Chip Select (HIGH) to Inactive Output (Hi-Z)		25		25	ns
12	t_{PLZ}(nWE) t_{PHZ}(nWE)	Dealy from Write Eanble (LOW) to inactive Output (Hi-Z)		30		30	ns

Notes:

1. Typical inputs are at VCC=5.0V and TA=25 °C
2. Output is preconditioned to insure corrcet data is present on al outputs when write is terminated (No write recovery Glitch)
3. t_{PLH}(A) and t_{PHL}(A) are tested with S (switch) closed and CL=50pF with both input and output timing refrenced to 1.5 V
4. t_{PZH}(nWE) and t_{PZH}9NCS) are measured with S open, CL=50pF and both input and output timing refrenced to 1.5 t_{PZL}(nWE) and t_{PZL}(nCS) are measured with S closed, CL=50pF and both input and output timing refrenced to 1.5 V. t_{PHZ}(nW and t_{PHZ}(nWE) are measured with S open , CL < or = 5pF and are measured between the 1.5 V level on the input and V_{OH}-500 mV level on the output. t_{PLZ}(nWE) and t_{PLZ}(nCS) are measured with S closed and CL < or = and are measu between the 1.5 V level on the input and V_{OL} + 500 mV on the output

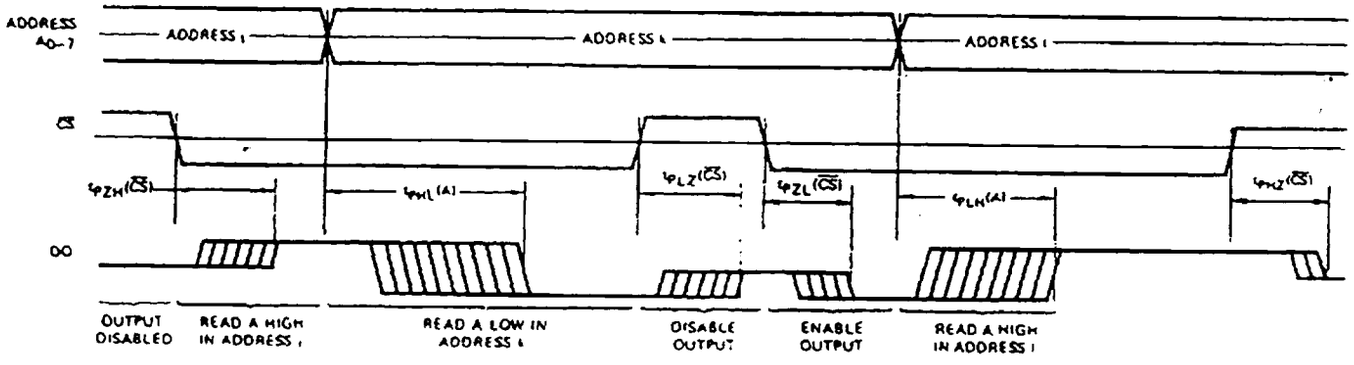
SWITCHING WAVEFORMS

WRITE MODE



Write cycle timing: The cycle is initiated bu an address change. After ts(A) max, the write cycle may begin. The chip select mus be LOW for writing. Following the write pulse th(A) max must be allowed before the address may be changed again. The outpu will be inactive(floating at tristate) while the Write Enable is LOW. Ordinarily, the chip select should be LOW during the entir write pulse.

READ MODE



Switching delays from address and chip select inputs to the data output. For the MSIS27C00 / 00A the disabled output is "OFF" represented by a single centerline.