To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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PRELIMINARY DATA SHEET

RENESAS

GaAs INTEGRATED CIRCUIT

μPG506P, μPG508P

Ku BAND PRESCALER CHIPS

μPG506P and μPG508P are GaAs prescalers and both devices are available in chip form. μPG506P is dynamic frequency divider which can operate up to 14 GHz. μPG508P is dynamic divider which can operate up to 13 GHz. The division ratio for μPG506P is 1/8, while 1/4 for μPG508P. These devices are suitable for frequency synthesizer of microwave applications systems and measurement equipment. Both use the BFL (Buffered FET Logic) circuit as the basic circuit.

FEATURES

- Wide operating frequency range: 8 to 14 GHz (μPG506P)
  8 to 13 GHz (μPG508P) @T_a = +25 °C
- Guaranteed performance over an ambient temperature range of T_a = −25 to +75 °C
- Low Phase Noise

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, V_{SS1} = 0 V)

Supply Voltage	$V_{DD}-V_{SS1}$	+5	V
Supply Voltage	$V_{SS2}-V_{SS1}$	−5	V
Input Power	P_{in}	+13	dBm
Total Power Dissipation	P_t*1	1.5	W
Operating Case Temperature Range	T_c*2	−65 to +125	°C
Storage Temperature	T_{stg}	−65 to +175	°C

*1 Mounted with AuSn hard solder
*2 The temperature of base material beside the chip

The information in this document is subject to change without notice.

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ELECTRICAL CHARACTERISTICS (T_a = 25 °C)*3

μPG506P (T_a = 25 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Supply Current (1)	I_{DD}	70	105	140	mA		V_{DD} = +3.8 V V_{SS1} = 0 V V_{SS2} = −2.2 V
Supply Current (2)	I_{SS1}	26	35	44	mA		
Supply Current (3)	I_{SS2}	44	70	96	mA		
Upper Limit of Input Frequency	$f_{in(u)}$	14			GHz	P_{in} = +6 dBm	
Lower Limit of Input Frequency	$f_{in(l)}$			8	GHz	P_{in} = +6 dBm	
Input Power	P_{in}	+2		+10	dBm	f_{in} = 8 to 13 GHz	
Output Power	P_{out}	0	+2		dBm	f_{in} = 14 GHz	

μPG506P (T_a = −25 to +75 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Supply Current (1)	I_{DD}		105		mA		V_{DD} = +3.8 V V_{SS1} = 0 V V_{SS2} = −2.2 V
Supply Current (2)	I_{SS1}		35		mA		
Supply Current (3)	I_{SS2}		70		mA		
Upper Limit of Input Frequency	$f_{in(u)}$	13.2			GHz	P_{in} = +6 dBm	
Lower Limit of Input Frequency	$f_{in(l)}$			8.2	GHz	P_{in} = +6 dBm	
Input Power	P_{in}	+2		+10	dBm	f = 9.2 to 12.2 GHz	
Output Power	P_{out}	−1	+1		dBm	f_{in} = 13.2 GHz	

μPG508P (T_a = 25 °C)

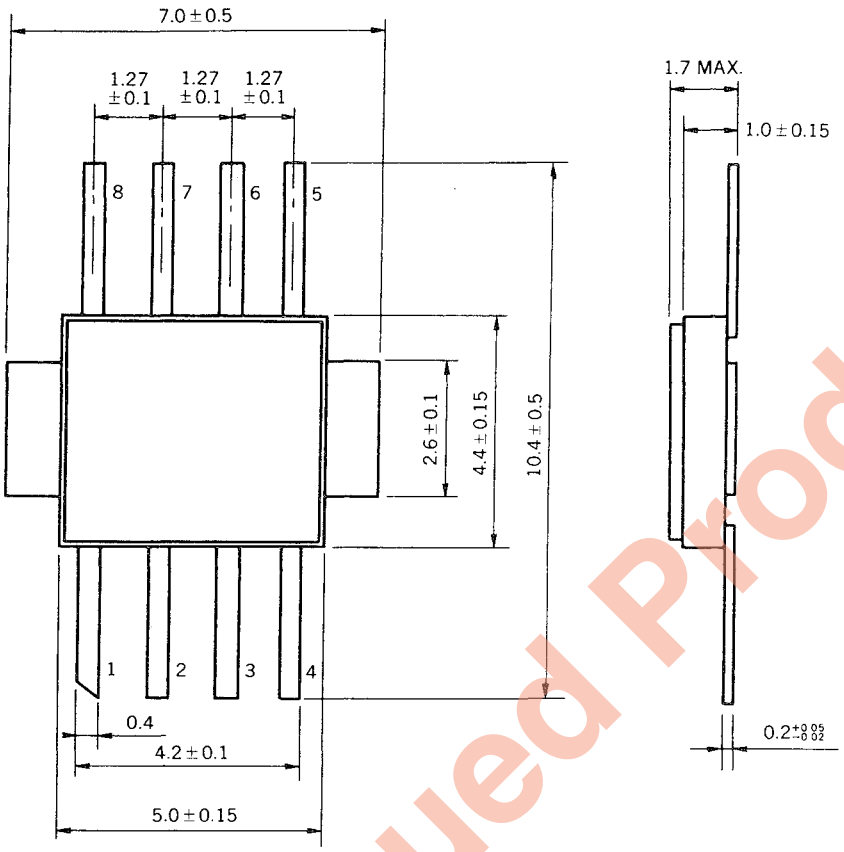
CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Supply Current (1)	I_{DD}		100	140	mA		V_{DD} = +3.8 V V_{SS1} = 0 V V_{SS2} = −2.2 V
Supply Current (2)	I_{SS1}		33	44	mA		
Supply Current (3)	I_{SS2}		67	96	mA		
Upper Limit of Input Frequency	$f_{in(u)}$	13			GHz	P_{in} = +6 dBm	
Lower Limit of Input Frequency	$f_{in(l)}$			8	GHz	P_{in} = +6 dBm	
Input Power	P_{in}	+6		+10	dBm	f_{in} = 8 to 13 GHz	
Otuput Power	P_{out}	0	+2		dBm	f_{in} = 13 GHz	

μPG508P (T_a = −25 to +75 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Supply Current (1)	I_{DD}		100		mA		V_{DD} = +3.8 V V_{SS1} = 0 V V_{SS2} = −2.2 V
Supply Current (2)	I_{SS1}		33		mA		
Supply Current (3)	I_{SS2}		67		mA		
Upper Limit of Input Frequency	$f_{in(u)}$	12.2			GHz	P_{in} = +6 dBm	
Lower Limit of Input Frequency	$f_{in(l)}$			8.5	GHz	P_{in} = +6 dBm	
Input Power	P_{in}	+6		+10	dBm	f = 8.5 to 12.2 GHz	
Output Power	P_{out}	−1	+1		dBm	f_{in} = 12.2 GHz	

*3 These characteristics are based on performance of devices mounted in the standard package shown in Fig. 1.

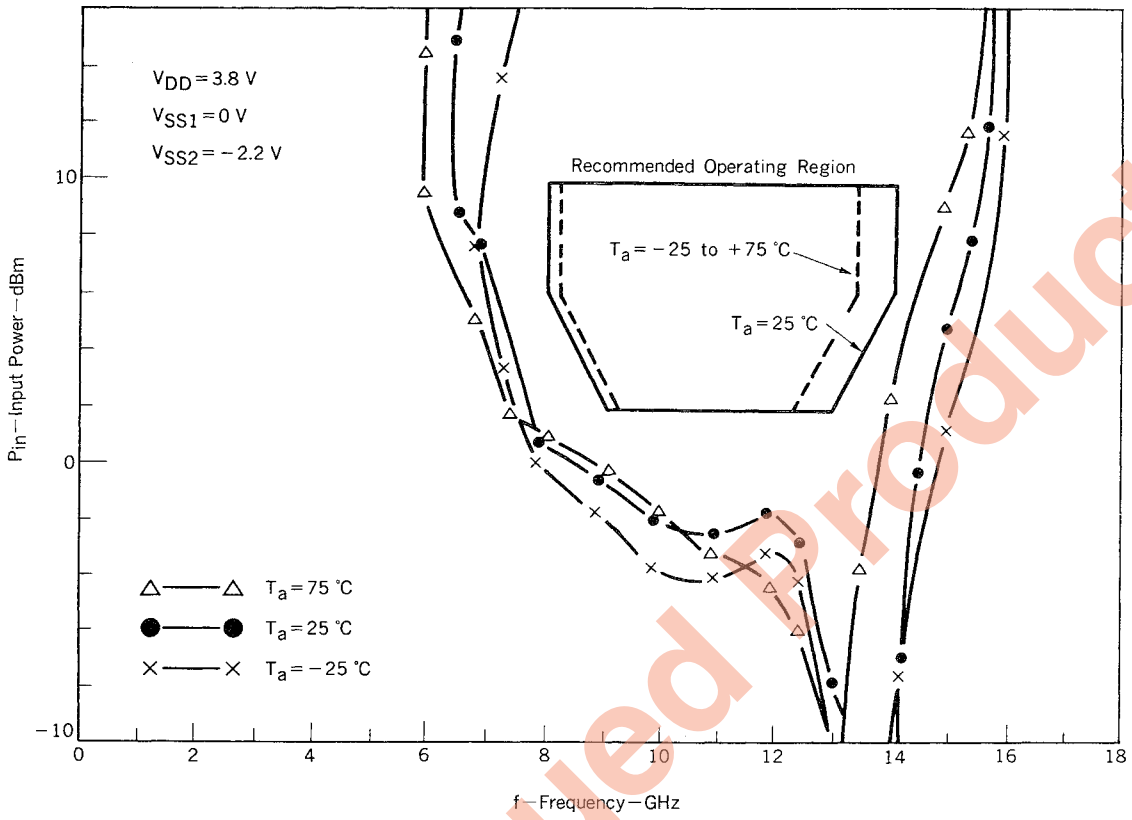
Fig. 1 8 pin ceramic flat package

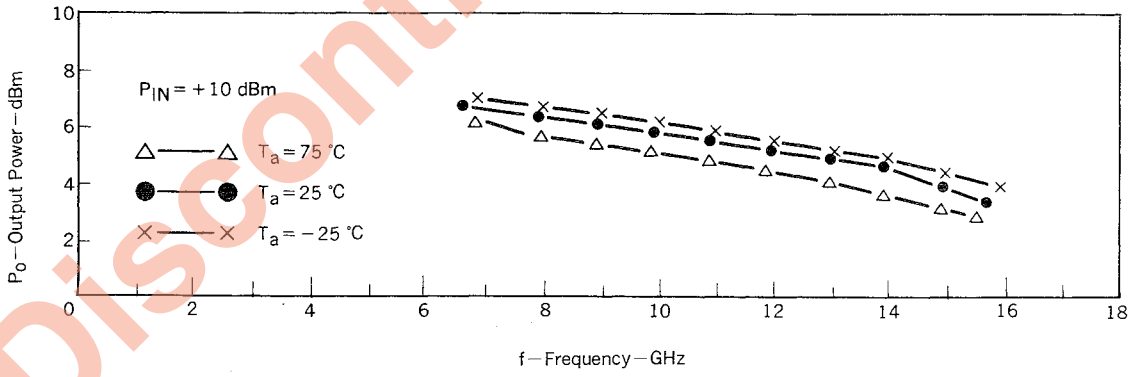


1: OUTPUT
2: V_{SS1}
3: Non Connection
4: V_{DD}
5: INPUT
6: V_{GG1}
7: V_{GG2} } Normally Open
8: V_{SS2}
FLANGE: GND

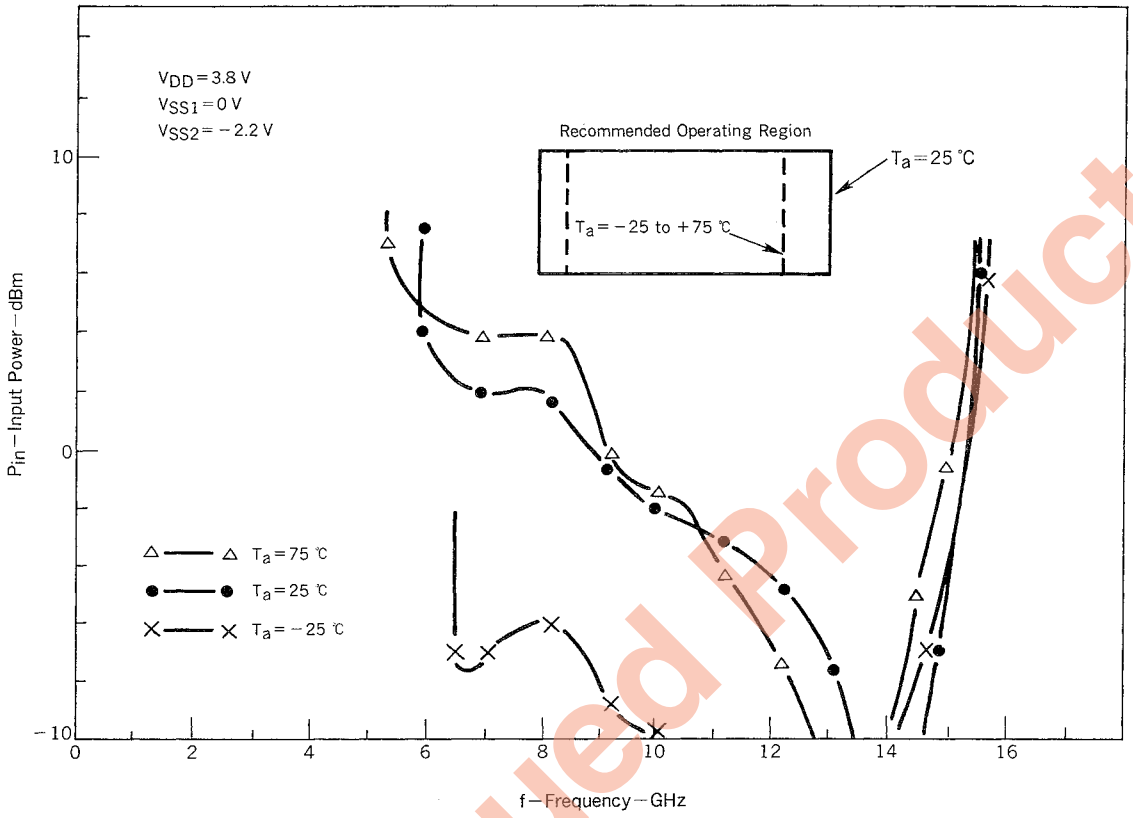
TYPICAL CHARACTERISTICS

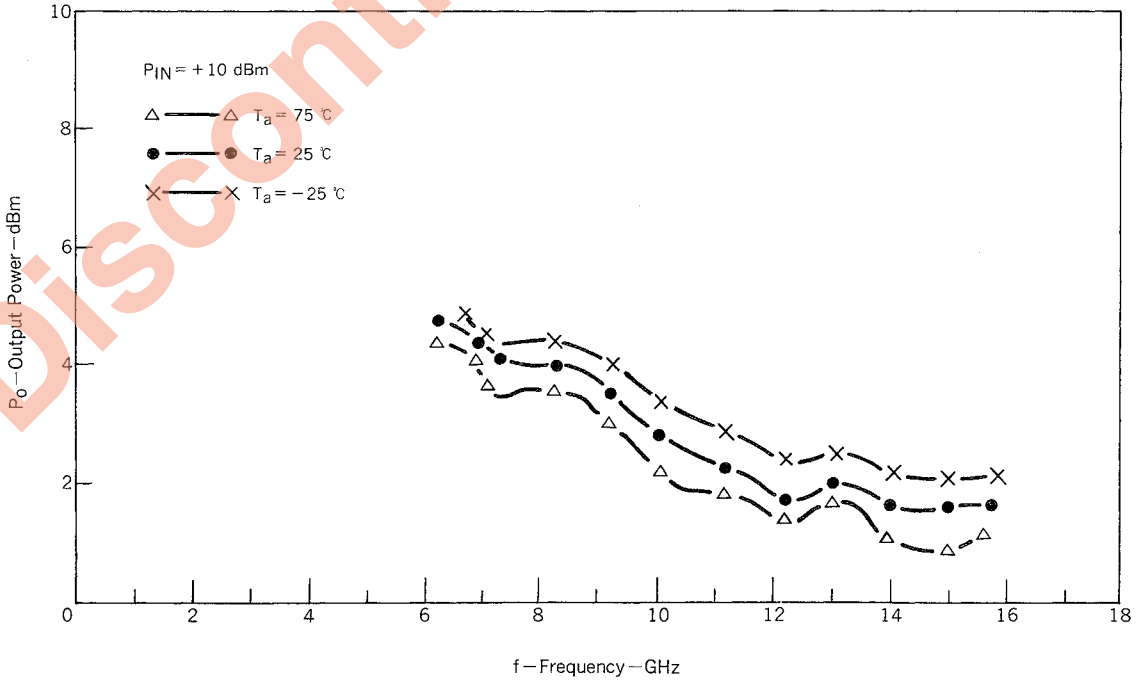
μPG506P





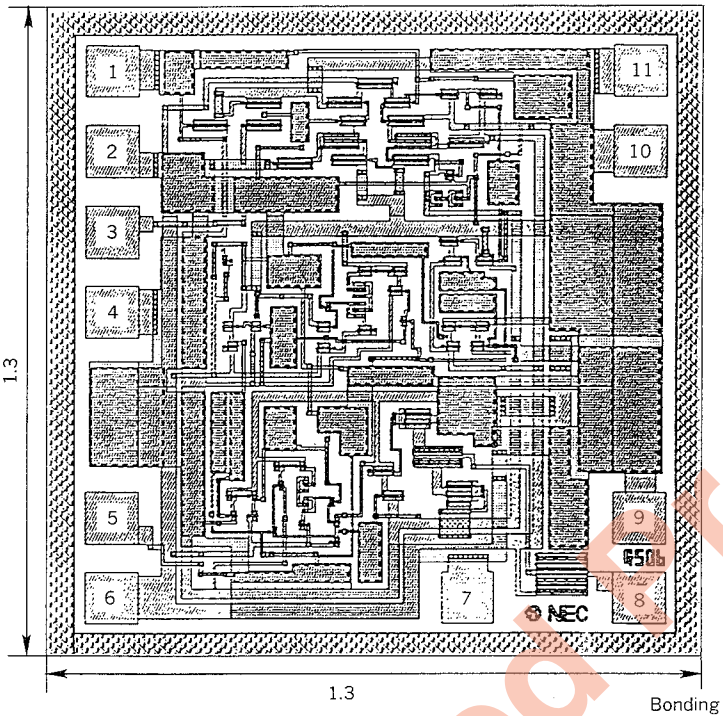
μPG508P





CHIP DIMENSIONS (Unit: mm)

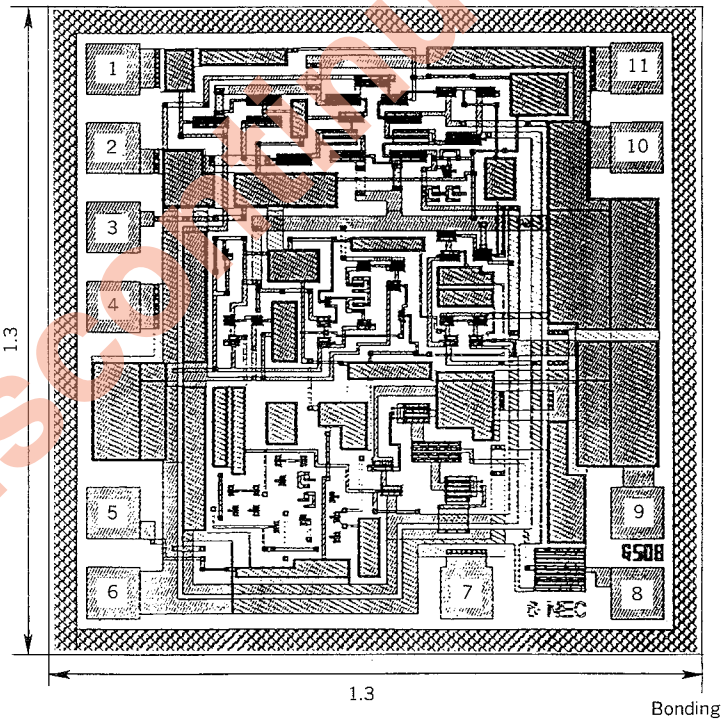
μPG506P



1 IN
2 GND
3 V_{GG1}
4 GND
5 V_{GG2}
6 V_{SS2}
7 GND
8 OUT
9 V_{SS1}
10 V_{DD}
11 GND

Bonding Pad size: 100 × 100 μm
t = 0.14

μPG508P



1 IN
2 GND
3 V_{GG1}
4 GND
5 V_{GG2}
6 V_{SS2}
7 GND
8 OUT
9 V_{SS1}
10 V_{DD}
11 GND

Bonding Pad size: 100 × 100 μm
t = 0.14

RECOMMENDED CHIP ASSEMBLY CONDITIONS

Die Attachment

Atmosphere	: N_2 gas
Temperature	: 320 ± 5 °C
AuSn Preform	: 0.5 x 0.5 x 0.05^t (mm), 2 pcs.
	*The hard solder such as AuSi or AuGe which has higher melting point than AuSn should not be used.
Base Material	: CuW, Cu, KV
	* Other material should not be used.

Epoxy Die Attach is not recommended.

Bonding

Machine	: TCB
	* USB is not recommended
Wire	: 30 μm diameter Au wire
Temperature	: 260 ± 5 °C
Strength	: 31 ± 3 g
Atmosphere	: N_2 gas

QUALITY ASSURANCE (Refer to GET-30116)

1. 100 % Tests

1-1 100 % DC and RF Probe

1-2 Visual inspection
MIL-STD-883/Method 2010 Condition B

2. Tests on Sampling Basis

2-1 Bond Pull Tests (In case of recommended chip handling)
MIL-STD-883 Method 2011
5 samples/wafer and 20 points tested
Accept 0/Reject 1

2-2 Tests in Standard Pakage
Test the electrical characteristics of chips assembled into the standard package used for μPG506B and μPG508B.
5 samples/wafer tested
DC and RF measurement Accept 1/Reject 2

3. WARRANTEE

NEC has a responsibility of quality assurance for the products within 180 days after delivered to customers where these are handled properly and stored in the desicater with the flow of dry N_2 gas.

4. CAUTION

4-1 Take great care to prevent static electricity.

4-2 Be sure that Die Attach is performed in N_2 atmosphere.

〔MEMO〕

M4 92.6