MC-41256A8
262,144 x 8-Bit
Dynamic NMOS RAM Module

Description

The MC-41256A8 is a 262,144-word by 8-bit NMOS RAM module designed to operate from a single + 5-volt power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-41256A8 is functionally equivalent to eight μPD41256 standard 256K DRAMs. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period.

Single Inline Memory Module (SIMM™) packaging enhances reliability and reduces the size, weight and cost of a system. The MC-41256A8 includes eight μPD41256s in PLCC packages and eight power supply decoupling capacitors.

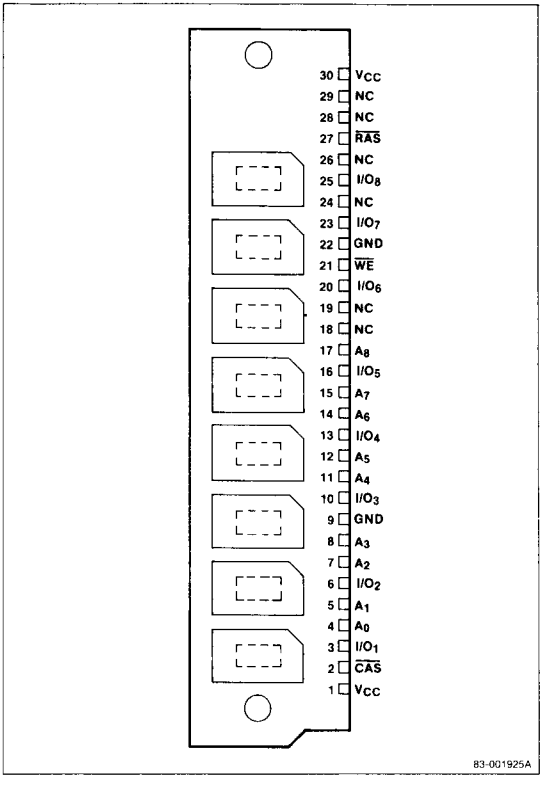
SIMM is a trademark of Wang Laboratories.

Features

- 262,144-word by 8-bit organization
- Single + 5-volt power supply
- Standard 30-pin SIMM packaging
- Eight 256K DRAMs in high-density PLCC packaging
- Eight power supply decoupling capacitors
- Low power dissipation of 220 mW max (standby)
- TTL-compatible inputs and outputs
- 256 refresh cycles every 4 ms
- Page mode

Pin Configuration

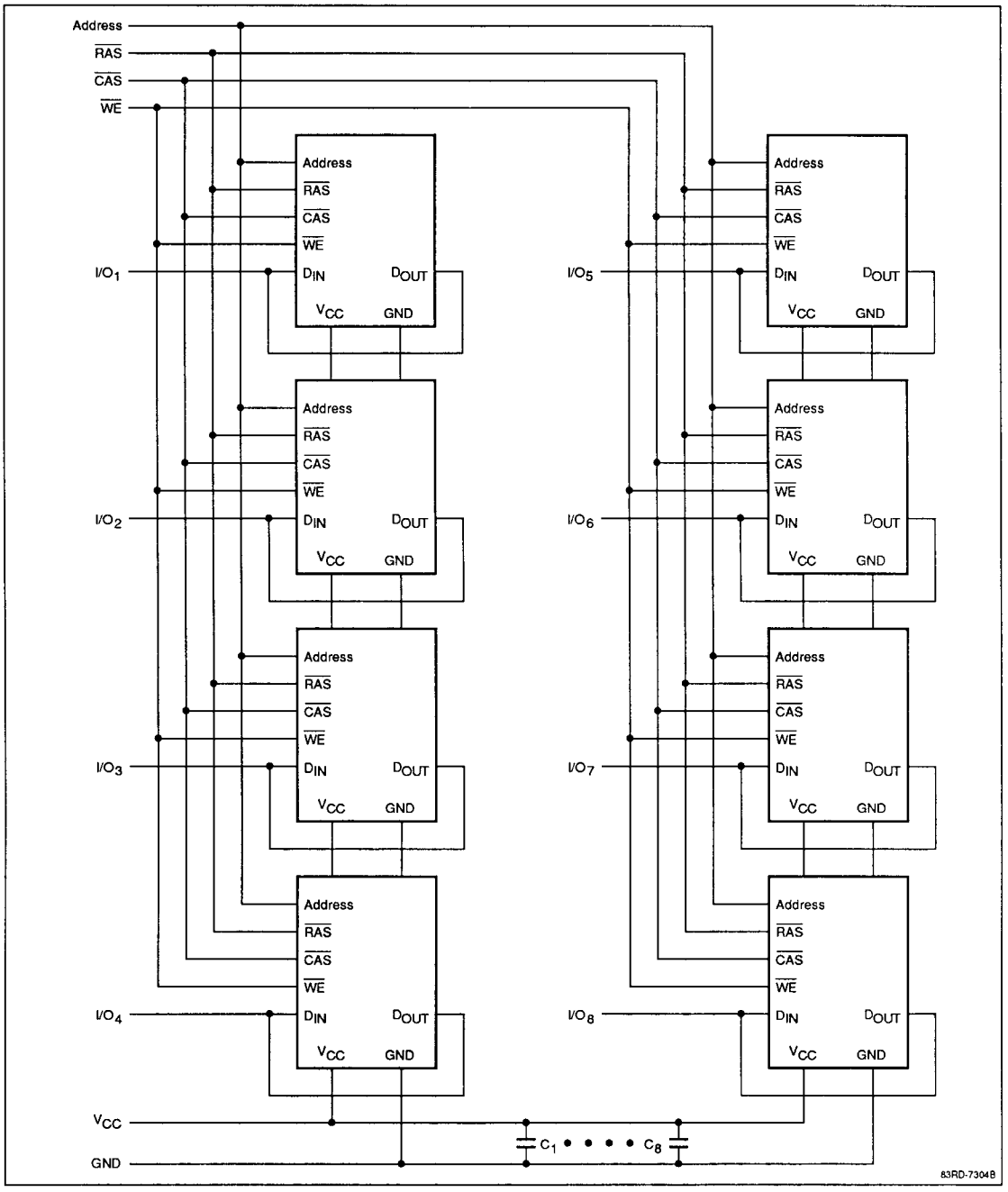
30-Pin SIMM



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_8	Common data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{IA}	55	pF	A_0 - A_8
	C_{IR}	70	pF	$\overline{RAS}$, $\overline{WE}$
	C_{IC}	70	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}	17	pF	For I/O_1 - I/O_8: $\overline{CAS}$ = V_{IH} to disable D_{OUT}

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) V_{CC} = +5.0 V ±5% for the −80 version.

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Ordering Information

Part Number	Access Time (max)	Read/Write Cycle Time (min)	Page Cycle Time (min)	Package
MC-41256A8B-80	80 ns	160 ns	70 ns	30-pin socket-mountable SIMM
B-10	100 ns	200 ns	100 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			40.0	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high-Z
Input leakage current	I_{IL}	−80		80	μA	V_{IN} = 0 V to V_{CC}; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

Notes:

(1) V_{CC} = +5.0 V ±5% for the −80 version.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		MC-41256A8-80		MC-41256A8-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.75	5.25	4.5	5.5	V	
Operating supply current, average	I_{CC1}		720		640	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} (min); I_O = 0 mA (Note 5)
Operating supply current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		640		520	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} (min); I_O = 0 mA (Note 5)

AC Characteristics (cont)

Parameter	Symbol	MC-41256A8-80 Min	MC-41256A8-80 Max	MC-41256A8-10 Min	MC-41256A8-10 Max	Unit	Test Conditions
Operating supply current, page cycle, average	I_{CC4}		560		480	mA	$\overline{RAS} \le V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min); I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		640		520	mA	$\overline{CAS} \le V_{IL}$; $\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I/O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	180		200		ns	(Note 6)
Page cycle time	t_{PC}	70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		50	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	16,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	20		40		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	10		10		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		75		ns	
Write command pulse width	t_{WP}	20		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		25		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		75		ns	

AC Characteristics (cont)

Parameter	Symbol	MC-41256A8-80 Min	MC-41256A8-80 Max	MC-41256A8-10 Min	MC-41256A8-10 Max	Unit	Test Conditions
Refresh period	t_{REF}		4		4	ms	Addresses A_0 - A_7
$\overline{WE}$ command setup time	t_{WCS}	0		0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	20		20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Output load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$.

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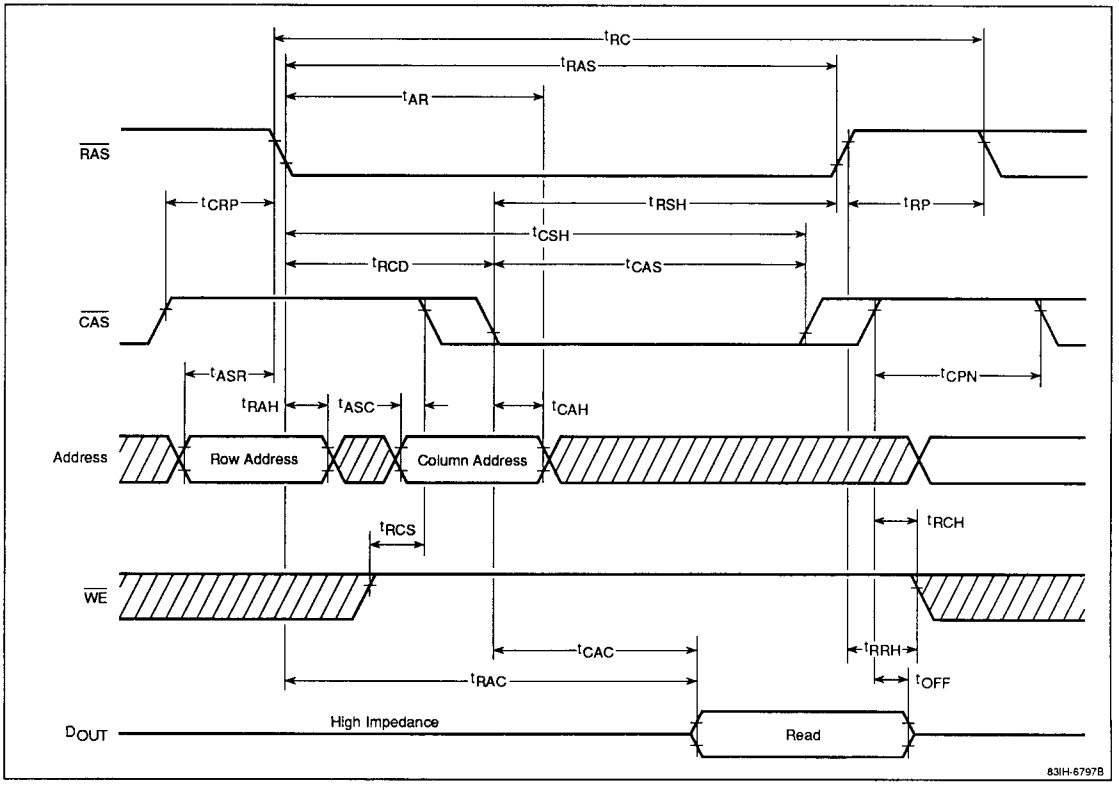
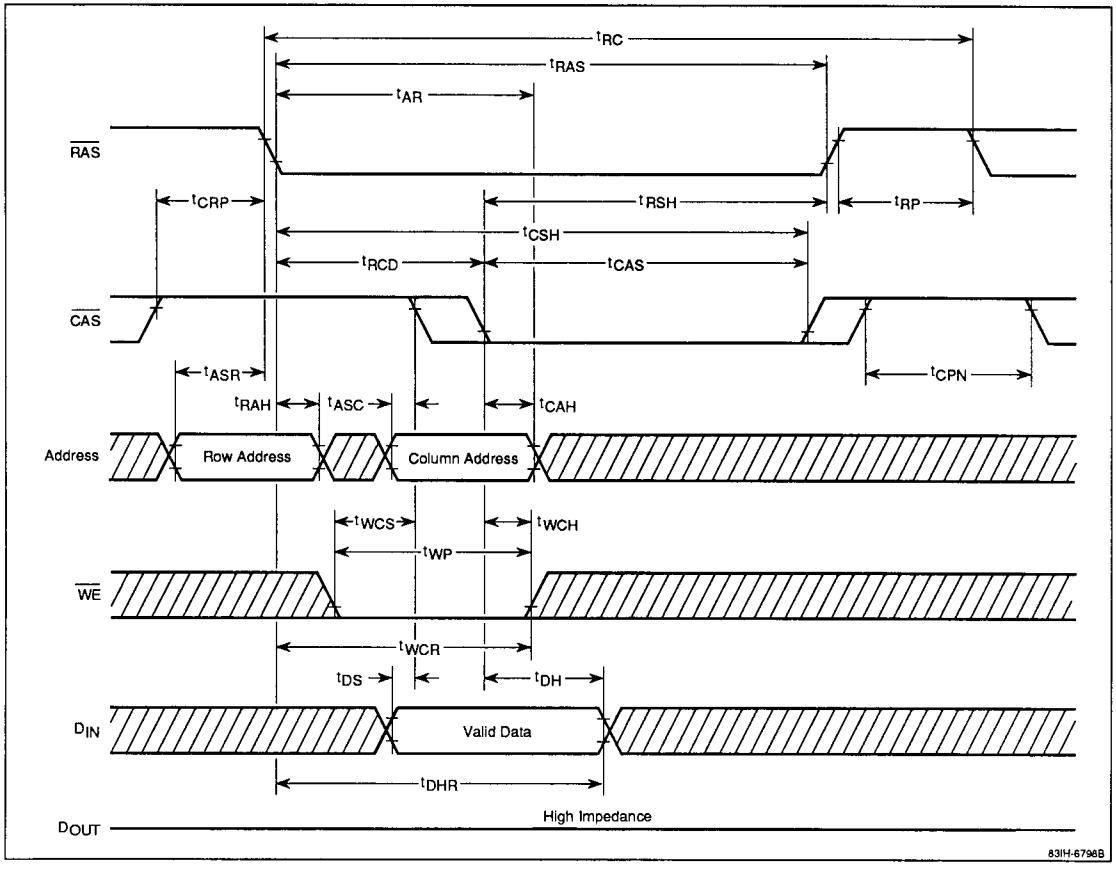
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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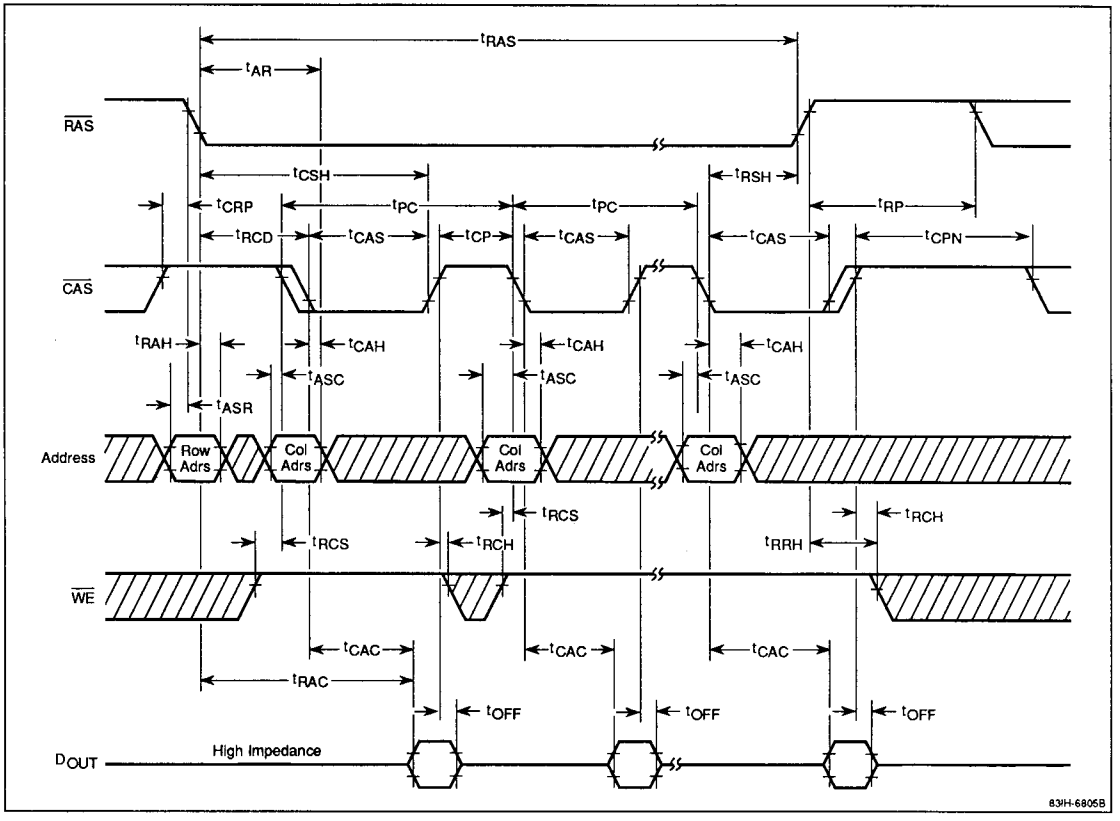
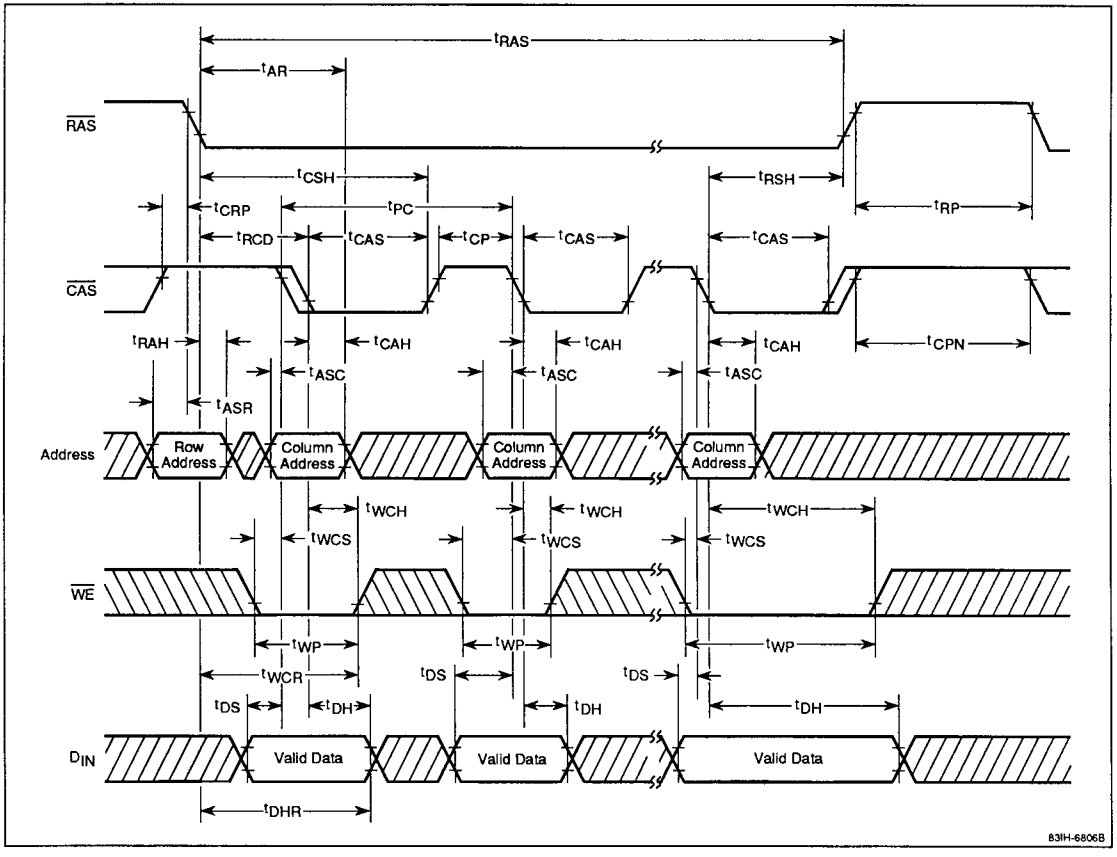
Timing Waveforms (cont)

Page Read Cycle



Timing Waveforms (cont)

Page Early Write Cycle



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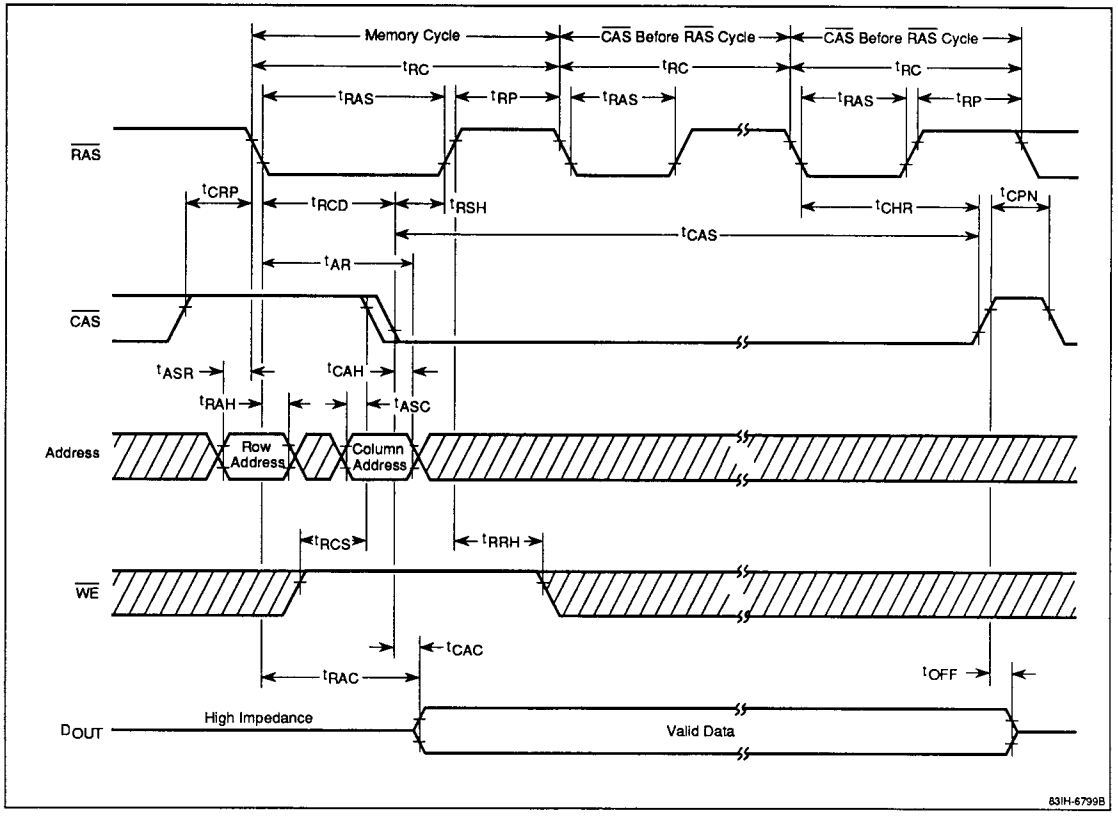
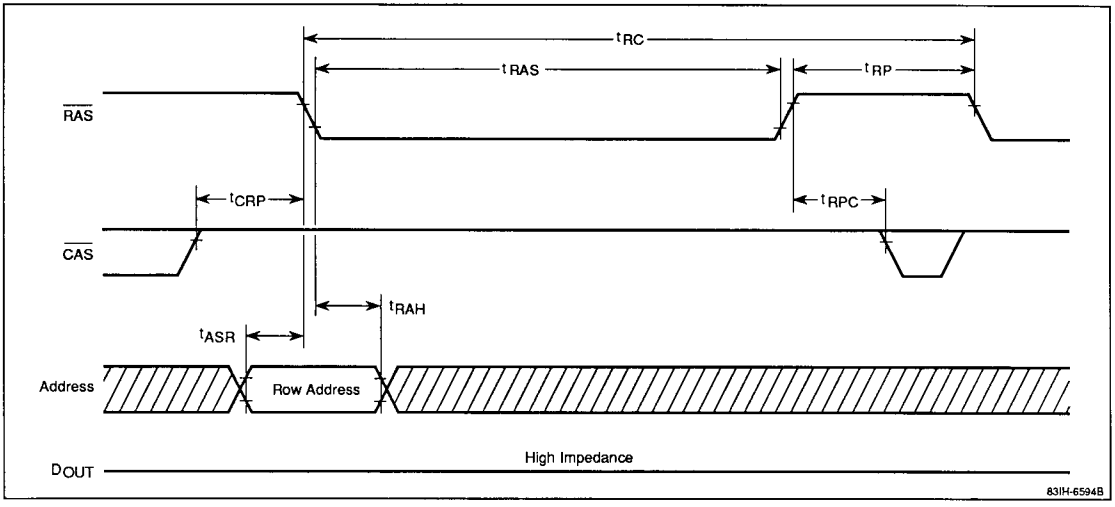
Timing Waveforms (cont)

Hidden Refresh Cycle

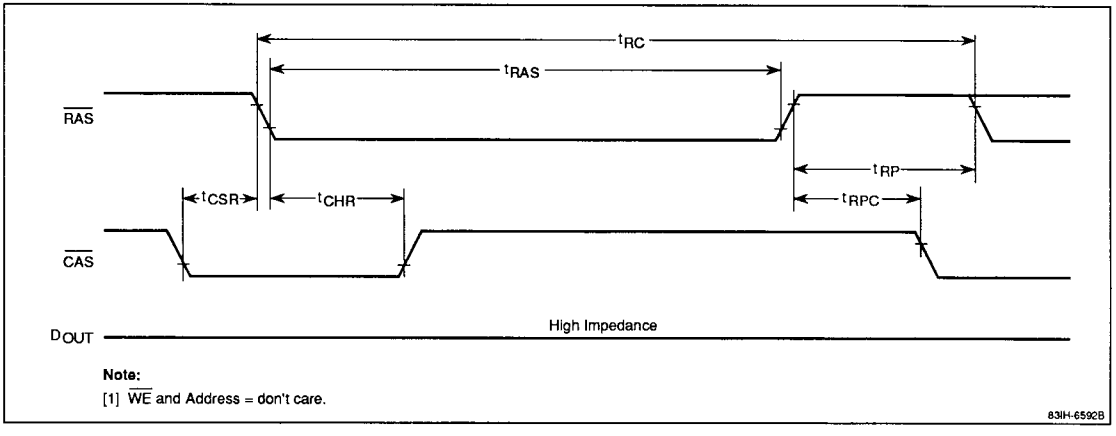


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$ and Address = don't care.

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