MOTOROLA

Quad Driver

Military 100E512

Product Preview

ELECTRICALLY TESTED PER:
100E512

The 100E512 is a quad driver with two pairs of OR/NOR outputs form each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the 100E511 is designed specifically for this purpose, and offers lower skew than the E512.

- 600 ps Max. Propagation Delay
- Common Enable Input
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
D_0 - D_3	Data Inputs
$\overline{EN}$	Enable Inputs
Q_{na} - Qnb	True Outputs
$\overline{Q_{na}}$ - $\overline{Qnb}$	Inverting Outputs

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

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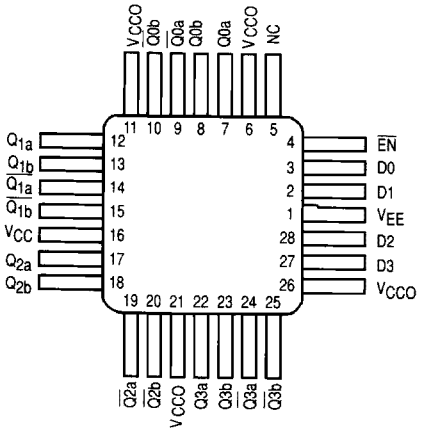
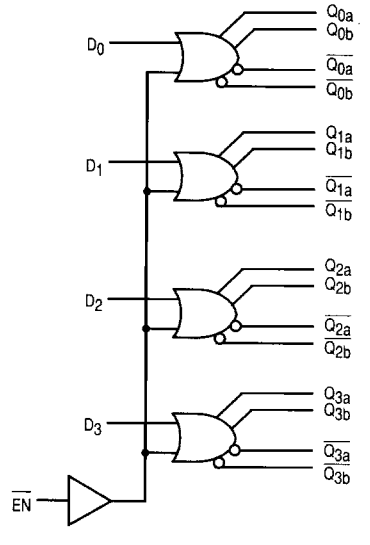


LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current							µA	
	D		200		200		200		
	$\overline{EN}$		150		150		150		
I_{EE}	Power Supply Current	47	56	54	65	47	56	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D	200	600	200	600	200	600	ps	
	$\overline{EN}$	275	675	275	675	275	675	ps	
t_{Skew}	Within-device Skew								
	Dn to Qn, $\overline{Qn}$	80		80		80		ps	(Note 1)
	Dna to Qnb	40		40		40		ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	275	700	275	700	275	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

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