Si2504
High Speed 12-Bit SAR

Siliconix incorporated

FEATURES

- High Speed (40 MHz typ.)
- Low Quiescent Power (I_{CC} < 10μA)
- Three-State Outputs
- Expandable Via Cascading
- Can Be Short-Cycled

BENEFITS

- Reduced Conversion Time
- Reduced Power Consumption
- Allows In-Circuit Trims
- Facilitates Higher Resolution A/D Converters
- Optimizes Conversion Time

APPLICATIONS

- High-Speed A/D Converters
- Low-Power Data Acquisition Systems
- Laser-Trimmed A/D Converters
- High Resolution A/D Converters
- Variable-Resolution Systems

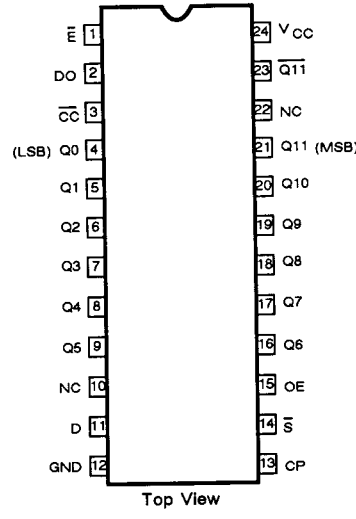
DESCRIPTION

The Si2504 is a high-speed, low power CMOS 12-Bit SAR (successive approximation register) that contains all of the necessary digital control and storage to build a 12-Bit successive-approximation A/D converter when combined with a 12-Bit D/A converter and a comparator. The register can be cascaded for applications requiring more than 12 bits of resolution, and may be short-cycled to reduce the conversion time in lower-resolution applications. Applications include custom and/or hybrid A/D converters with resolutions from 8 to 12 bits, and up to 24 bits when cascading two devices. The 12 data outputs have 3-state output buffers, allowing the SAR to be placed in a high-impedance mode, allowing the D/A converter in an A/D system to be trimmed without contending with the output of the SAR.

The Si2504 is built in a 2 micron silicon-gate CMOS process, alowing high speed operation at reduced power, with TTL-compatible data inputs and outputs. It is available in a 0.600" wide 24-pin plastic DIP for operation over the commercial, C suffix (0 to 70°C) temperature range. The Si2504 is also available in die form, inspected to MIL-STD-883, method 2010, visual B.

PIN CONFIGURATION

Dual-In-Line Package

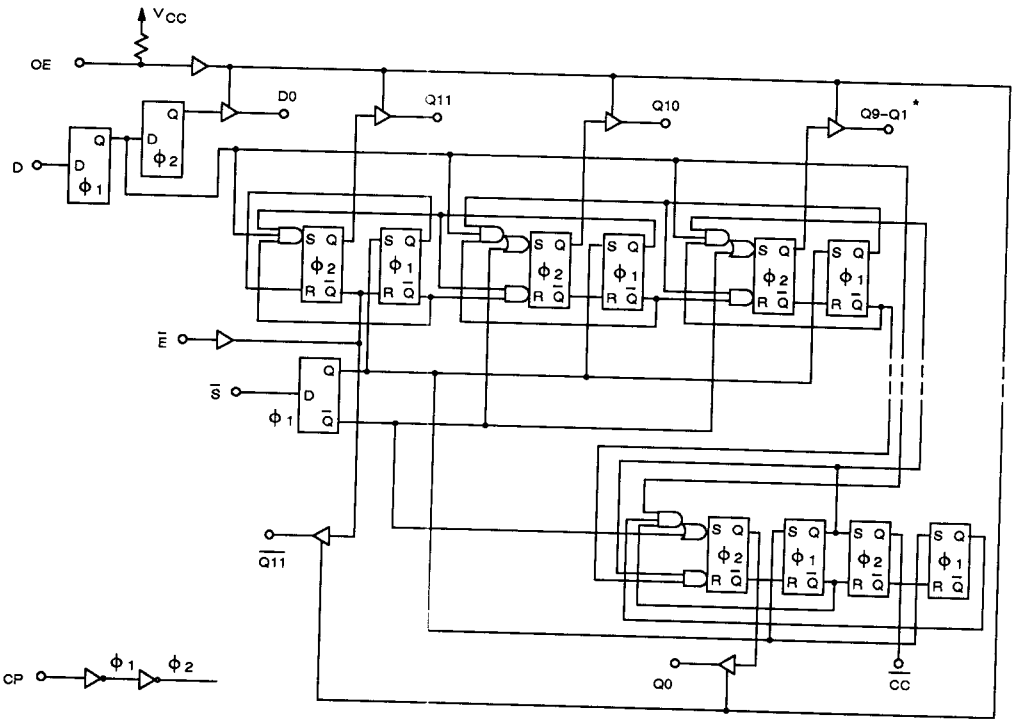


Top View

Order Numbers:
Si2504CJ
Plastic DIP

Si2504 Dice

FUNCTIONAL BLOCK DIAGRAM



* Cell logic is repeated for stages Q9 to Q1.

ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND

V_{CC} ..... -0.3 V to 7 V

Voltage Applied to Outputs ..... -0.3 V to V_{CC} + 0.3 V

Output Current ..... 10 mA

Input Voltage ..... -0.3 V to V_{CC} + 0.3 V

Input Current ..... -30 to 5 mA

Storage Temperature ..... -65 to 125°C

Operating Temperature ..... 0 to 70°C

Power Dissipation (Package)*
24-Pin Plastic DIP** ..... 1000 mW

* All leads welded or soldered to PC board.
** Derate 11.0 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_{CC} = 5 V ±10%	LIMITS 1=25 °C 2=70 °C 3=0 °C		C SUFFIX MIN [b]	C SUFFIX MAX [b]	UNIT
			TEMP	TYP [c]			
STATIC							
High Level Output Voltage	V_{OH}	I_{OH} = -2 mA	1,2,3		3		V
Low Level Output Voltage	V_{OL}	I_{OL} = 6 mA	1,2,3			0.4	V
High Level Input Voltage	V_{INH}	V_{CC} = 5.5 V	1,2,3		2.4		V
Low Level Input Voltage	V_{INL}	V_{CC} = 4.5 V	1,2,3			0.6	V
Pull-Up Resistance (OE only)	R_{pup}		1,2,3	500	100	900	kΩ
Input Leakage Current (except OE)	I_{IN}	$V_{IH} = V_{CC}$, V_{IL} = GND, V_{CC} = 5.5 V	1,2,3		-1	1	µA
Output OFF State Leakage Current (except $\overline{CC}$)	I_{OZ}	OE = 0 V, $V_{OUT} = V_{CC}$ or GND, V_{CC} = 5.5 V	1,2,3		-1	1	µA
Static Supply Current	I_Q	$I_{OH} = I_{OL}$ = 0 A	1,2,3			10	µA
Output Short Circuit [d] Current	I_{SC}	V_{CC} = 5.5 V, V_{OUT} = 0 V	1,2,3	-30			mA
Supply Current	I_{CC}	V_{IN} = 0 V or 5 V, f_{CLOCK} = 16.67 MHz	1,2,3			17	mA
DYNAMIC							
Turn OFF Delay CP to Output LOW	t_{PD-}	C_L = 15 pF; Outputs Q11, $\overline{Q11}$	1	22		44	ns
		C_L = 15 pF; Outputs Except Q11, $\overline{Q11}$	1	15		44	ns
Turn OFF Delay CP to Output HIGH	t_{PD+}	C_L = 15 pF	1	15		44	ns
Data Setup Time	$t_{S(D)}$	C_L = 15 pF	1	4	-10	10	ns
Start Input Setup Time	$t_{S(\overline{S})}$	C_L = 15 pF	1	16	0	25	ns
Turn OFF Delay $\overline{E}$ to Q11 HIGH	$t_{PD+(\overline{E})}$	C_L = 15 pF; CP = HIGH, $\overline{S}$ = LOW	1	10		44	ns
Turn ON Delay $\overline{E}$ to Q11 LOW	$t_{PD-(\overline{E})}$	C_L = 15 pF; CP = HIGH, $\overline{S}$ = LOW	1	30		44	ns
Bus Release Time OE to Outputs High Impedance	t_{OER}	C_L = 15 pF; R_L = 3 kΩ	1	40		44	ns
Bus Access Time OE to Outputs V_{IH} or V_{IL}	t_{OEA}	C_L = 15 pF; R_L = 3 kΩ	1	22		44	ns

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_{CC} = 5 V ±10%	LIMITS 1=25 °C 2=70 °C 3=0 °C		C SUFFIX		UNIT
			TEMP	TYP [c]	MIN [b]	MAX [b]	
DYNAMIC (Cont'd)							
Minimum Low Clock Pulse	$t_{PWL(CP)}$		1	23	30		ns
Minimum High Clock Pulse	$t_{PWH(CP)}$		1	10	30		ns
Maximum Clock Frequency	f_{MAX}		1	40		16.67	MHz

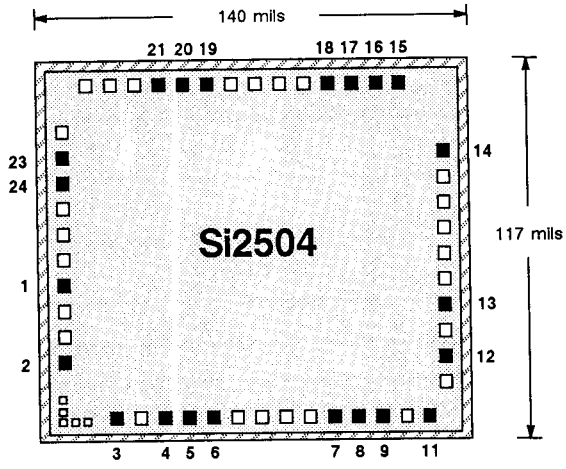
DIE SORT LIMITS

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_{CC} = 5 V ±10%	LIMITS 1=25 °C		C SUFFIX		UNIT
			TEMP	TYP [c]	MIN [b]	MAX [b]	
STATIC							
High Level Output Voltage	V_{OH}	I_{OH} = -2 mA	1		3		V
Low Level Output Voltage	V_{OL}	I_{OL} = 6 mA	1			0.4	V
High Level Input Voltage	V_{INH}	V_{CC} = 5.5 V	1		2.4		V
Low Level Input Voltage	V_{INL}	V_{CC} = 4.5 V	1			0.6	V
Pull-Up Resistance (OE only)	R_{pup}		1	500	100	900	kΩ
Input Leakage Current (except OE)	I_{IN}	$V_H = V_{CC}$, V_{IL} = GND V_{CC} = 5.5 V	1		-1.0	1.0	µA
Output OFF State Leakage Current (except $\overline{CC}$)	I_{OZ}	OE = 0 V, $V_{OUT} = V_{CC}$ or GND V_{CC} = 5.5 V	1		-1.0	1.0	µA
Static Supply Current	I_Q	$I_{OH} = I_{OL}$ = 0 V	1			10.0	µA
Output Short Circuit [d] Current	I_{SC}	V_{CC} = Max, V_{OUT} = 0 V	1	-30			mA

NOTES:

a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. No more than one output should be short circuited at one time. Duration of short circuit should be less than 1 s.

DIE TOPOGRAPHY

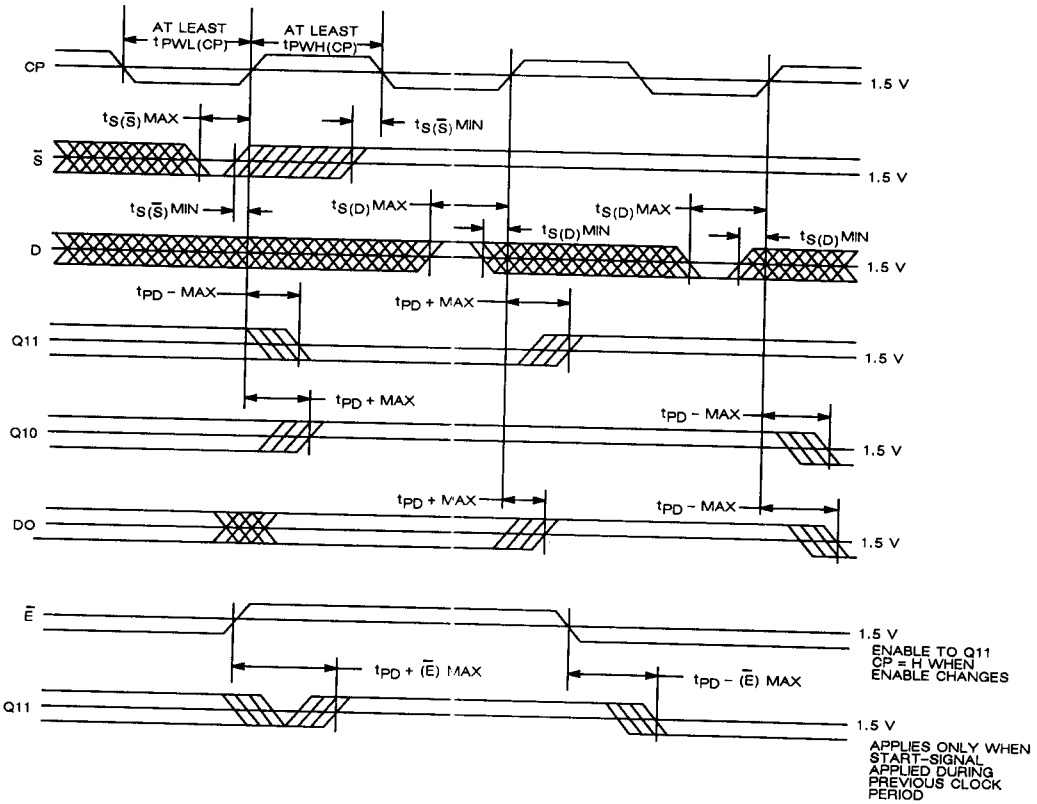


TRUTH TABLE

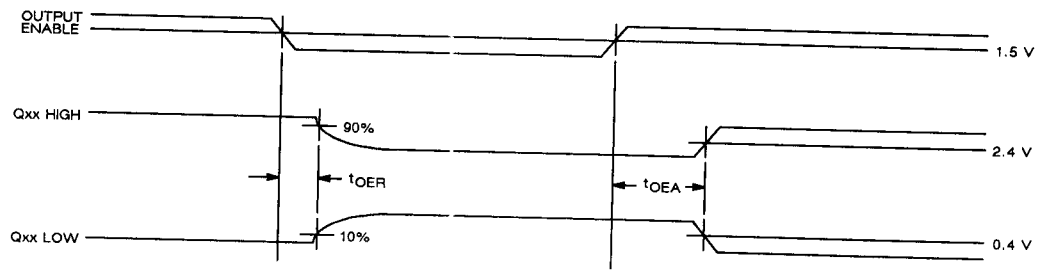
TIME	INPUTS				OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	OE	DO	Q_{11}	Q_{10}	Q_9	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	H	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	H	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	H	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	H	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	H	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	H	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	H	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	H	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	H	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	H	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	H	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	H	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	H	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	H	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	X	X	X	L	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	NC

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, NC = No Change, Z = HIGH Impedance

SWITCHING TIME WAVEFORMS

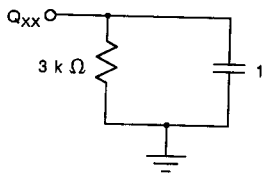


SWITCHING TIME WAVEFORMS (OUTPUT ENABLE)

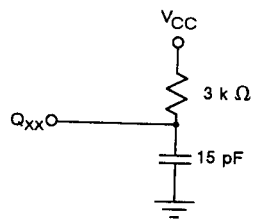


TEST CONDITIONS:

V_{OH} to HIGH - Z or
HIGH - Z to V_{OH}



V_{OL} to HIGH - Z or
HIGH - Z to V_{OL}



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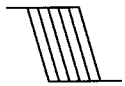
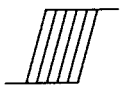
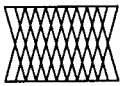
DEFINITIONS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
———		
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

KEY TO TIMING DIAGRAM

t_{PD} - The propagation delay from the clock signal LOW --> HIGH transition to an output signal HIGH --> LOW transition.

t_{PD} + The propagation delay from the clock signal LOW --> HIGH transition to an output signal LOW --> HIGH transition.

t_{PD} - ($\overline{E}$) The propagation delay from the Enable signal HIGH --> LOW transition to the Q11 output signal HIGH --> LOW transition.

t_{PD} + ($\overline{E}$) The propagation delay from the Enable signal LOW --> HIGH transition to the Q11 output signal LOW --> HIGH transition.

$t_{S(D)}$ The set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max and t_s min before the clock.

$t_{S(\overline{S})}$ The set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or the time required for a HIGH level to be present on $\overline{S}$ before the HIGH to LOW clock transition to prevent resetting.

$t_{PW(CP)}$ The minimum clock pulse width (LOW or HIGH) required for proper register operation.

t_{OER} The delay from OE to a 10% change in the outputs when loaded with 3 kΩ and 15 pF.

t_{OEA} The delay from OE to an output crossing 2.4 V or 0.4 V when loaded with 3 kΩ and 15 pF.

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock changes from HIGH-to-LOW, and a set of slave latches, that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter. It accepts data at the D input of the register and sends the data to the appropriate slave latch. This data appears at the register output and the DO output on the Si2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW, ready for the next iteration and so on for each successive bit conversion cycle.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during a full clock LOW-to-HIGH transition. The register synchronously resets the state Q11 LOW, and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal must be removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the Q11 register bit. The Q10 register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the Q10 register bit and Q9 is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

OPERATION (Cont'd)

In order to allow one's or two's complement conversion, the complementary output of the most significant register bit is made available.

An active LOW enable input ($\overline{E}$) allows devices to be cascaded together to form a longer register. This is done by paralleling the clock, D and $\overline{S}$ inputs and connecting the $\overline{CC}$ output to the $\overline{E}$ input of the next less significant device. When the Start signal resets the registers, the $\overline{CC}$ and $\overline{E}$ signals go HIGH, starting conversion in the MS Device and inhibiting the next less significant device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level. If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

The Q and DO outputs may be forced into a high impedance state **by bringing OE LOW**. This allows busing on common microprocessor buses or laser trimming of hybrid circuits without damaging the Si2504.

APPLICATION HINTS

1. The register can be used with current switches that require either a LOW voltage level or a HIGH voltage level to turn the switch on. If current switches are used which turn on with a LOW logic level, the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a HIGH logic level then the digital output is active HIGH; a logic "1" is represented as a HIGH voltage level.

2. For a maximum digital error of ±1/2 LSB the comparator must be biased. If current switches that require a LOW logic level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a HIGH logic level to turn ON then the comparator must be biased -1/2 LSB.

3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion. Additional data input gating should be used to eliminate the possibility of false BCD coding.

4. The register can be used to perform 2's complement conversion by offsetting the comparator 1/2 full range +1/2 LSB and using $\overline{Q11}$ as the sign bit.

5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the Start input the OR function of $\overline{CC}$ and the appropriate register output.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
1	$\overline{E}$	Register ENABLE. This input is used to expand the length of the register and when HIGH forces the Q11 register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (GND).
2	DO	The serial DATA OUTPUT.
3	$\overline{CC}$	CONVERSION COMPLETE output. This output remains HIGH during conversion and goes LOW when a conversion is complete.
4–9	Q0–Q5	Register OUTPUTS. The six least significant bits of the register. Q0 is the LSB.

PIN DESCRIPTION (Cont'd)

PIN NUMBER	SYMBOL	DESCRIPTION
10	NC	No connection.
11	D	Serial DATA Input.
12	GND	Ground.
13	CP	CLOCK PULSE Input.
14	$\overline{S}$	START input. Holding this input LOW for at least one clock period will reset the register to Q11 = LOW and Q0 – Q10 = HIGH. A LOW of one clock period is not necessary if it meets the set-up time requirements of the $\overline{S}$ input.
15	OE	OUTPUT ENABLE input. A LOW on this input will disable the Q11 – Q0, $\overline{Q11}$ outputs putting them in a HIGH IMPEDANCE state. This input has an internal pull-up and needs no connection for normal operation.
16–21	Q6–Q11	Register OUTPUTS. The six most significant bits of the register. Q11 is the MSB.
22	NC	No Connection.
23	$\overline{Q11}$	Complementary output of the MSB register.
24	V_{CC}	Positive power supply input.