HARRIS SEMICONDUCTOR

HS-65C262RH/RRH
HS-65T262RRH

Radiation Hardened 16K x 1 CMOS RAM

December 1992

Features

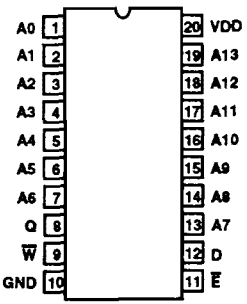
- Radiation Hardened EPI-CMOS
  - Total Dose 2 x 10^5 RAD(Si)
  - Transient Upset > 5 x 10^8 RAD(Si)/s
  - Latch-up Free > 1 x 10^{12} RAD(Si)/s
- Single Event Upset Resistant Option
- Low Standby Current 200µA (Max)
- Low Operating Current 6mA/MHz (Max)
- Fast Access Time 150ns (Typ)
- 16,384 x 1-Bit
- Single +5V Power Supply
- Asynchronous Operation
- CMOS or TTL Compatible Inputs
- Completely Static Operation
- Three-State Output
- Military Temperature Range -55°C to +125°C

Description

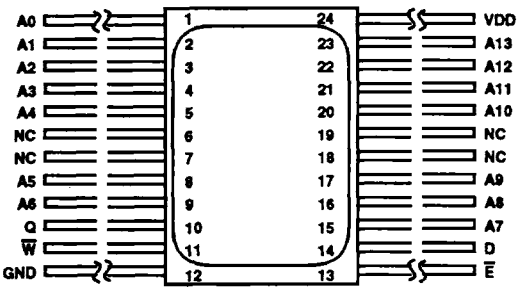
The HS-65C262RH and HS-65T262RRH are both designed to be functionally compatible with the Harris HM-65262. Two versions of the radiation hardened CMOS RAM are offered to provide both CMOS input levels (HS-65C262RH) and TTL compatible input levels (HS-65T262RRH). Both RAMs are asynchronous 16,384 x 1 bit static CMOS RAMs fabricated using the Harris radiation hardened, self-aligned junction isolated silicon gate technology. The devices are designed to have a maximum access time of 150ns for CMOS input levels and 175ns for TTL input levels after exposure to 2 x 10^5 Rads(Si) over the full military temperature range. Latch-up free operation is achieved by the use of epitaxial starting material. In addition, the devices have the option to be single event upset resistant. Operation is designed for +5V. Contact your nearest Harris represent- ative for sample availability.

Pinouts

20 PIN CERAMIC DIP
CASE OUTLINE D8, CONFIGURATION 3
TOP VIEW



24 PIN FLATPACK
CASE OUTLINE F-6A, CONFIGURATION 2
TOP VIEW

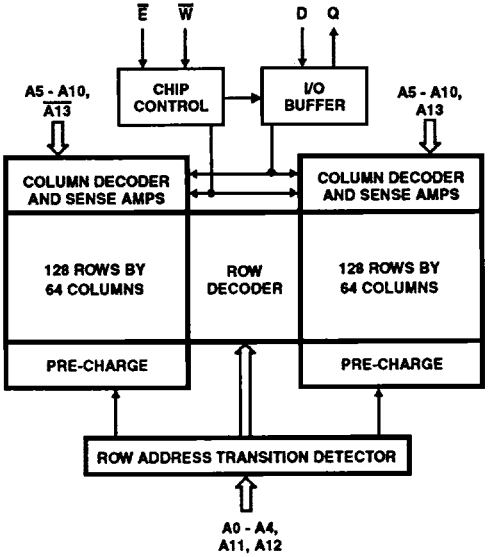


PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
NC	No Connect

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3031

Functional Diagram



TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE
1	X	X	Disabled
0	1	1	Enabled
0	0	1	Read
0	X	0	Write

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, E = 5.5V, VO = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, E = VDD-0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 2), f = 1MHz, E = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, E = VDD-0.3V, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5, IO = 0mA, E = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Functional Test	FT	VDD = 4.5V (Note 3)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. Typical derating = 6mA/MHz increase in IDDOP.
3. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH ≤ 1.5V, and VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1, 2, 3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	145	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	95	-	ns
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	150	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1,2,3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	95	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	95	-	ns
Write Enable Pulse Width	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	85	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	85	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	150	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	85	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	85	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns

NOTES:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	8	pF
			1, 3, 4	$T_A = +25°C$	-	10	pF
Output Capacitance	CO	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	10	pF
			1, 3, 4	$T_A = +25°C$	-	12	pF
Read/Write	(1) TAVAX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	150	-	ns
Write Enable to Output In High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Output Enable High to Output High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	25	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Invalid Output Hold Time	(23) TAXQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	ns
Cycle Time	TAVAX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	150	-	ns
High Level Output Voltage	VOH2	VDD = 4.5V, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VDD - 0.4V	-	V

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All measurements referenced to device grounds.

TABLE 4. POST 200K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
	IIH	±100nA
Low Impedance Output Leakage Current	IOZL	±1µA
High Impedance Output Leakage Current	IOZH	±1µA
Standby Supply Current	IDDSB1	±30µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... VDD -1.5V to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max.
SEU Immunity Operating Temperature Range ..... -20°C to +80°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 5.0mA	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD-0.3V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 2), f = 1MHz, $\overline{E}$ = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, E = VDD-0.3V, VI = VDD or GND	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5, IO = 0mA, E = 0.8V, VI = GND or VDD	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	200	µA
Functional Test	FT	VDD = 4.5V (Note 3)	7, 8A, 8B	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTE:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. Typical derating = 6mA/MHz increase in IDDOP.
3. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH ≤ 1.5V, and VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1, 2, 3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	145	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	150	-	ns
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	-55°C ≤ T_A ≤ +125°C	-	150	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1, 2, 3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	150	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	150	-	ns
Write Enable Pulse Width	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	150	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	140	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	150	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	140	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	140	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns

NOTES:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	8	pF
			1, 3, 4	$T_A = +25°C$	-	TBD	pF
Output Capacitance	CO	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	10	pF
			1, 3, 4	$T_A = +25°C$	-	TBD	pF
Read/Write	(1) TAVAX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	150	-	ns
Write Enable to Output in High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Output Enable High to Output High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	25	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	(23) TAXQX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	5	-	ns
High Level Output Voltage	VOH2	VDD = 4.5, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VDD-0.4V	-	V
Cycle Time	TAVAX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	150	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All Measurements Referenced To Device Grounds

TABLE 4. POST 200K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
	IIH	±100nA
Low Impedance Output Leakage Current	IOZL	±1µA
High Impedance Output Leakage Current	IOZH	±1µA
Standby Supply Current	IDDSB1	±30µA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage ..... GND-0.3V to VDD+0.3V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 6mA/MHz Increase in IDDOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Braze Seal DIP Package	78°C/W	13°C/W
Braze Seal FP Package	91°C/W	11°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package 0.64W
Braze Seal FP Package 0.55W
Gate Count ..... 26256 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0V to +0.8V
Input High Voltage ..... +2.3V to VDD
Data Retention Supply Voltage ..... 3.0V to 4.5V
Input Rise and Fall Time ..... 40ns Max.
SEU Immunity Operating Temperature Range ..... -20°C to +80°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -5.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VDD = 5.5V, $\overline{E}$ = 5.5V, VO = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-10.0	10.0	µA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	µA
Standby Supply Current	IDDSB1	VDD = 5.5V, IO = 0mA, $\overline{E}$ = VDD-0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	200	µA
Standby Supply Current	IDDSB2	VDD = 5.5V, IO = 0mA, $\overline{E}$ = 2.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	500	µA
Operating Supply Current	IDDOP	VDD = 5.5V, (Note 2), f = 1MHz, $\overline{E}$ = 0.8V, VI = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-	6	mA
Data Retention Supply Current	IDDDR	VDD = 3.0V, IO = 0mA, $\overline{E}$ = VDD-0.3V, VI = VDD or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	100	µA
Enable Supply Current	IDDEN	VDD = 5.5, IO = 0mA, E = 0.8V, VI = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-	200	µA
Functional Test	FT	VDD = 4.5V (Note 3)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

NOTE:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. Typical derating = 6mA/MHz increase in IDDOP.
3. Tested as follows: f = 3MHz, VIH = 4.5V, VIL = 0V, IOH = -4.0mA, IOL = 4.0mA, VOH ≤ 1.5V, and VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1, 2, 3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address Access Time	(2) TAVQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	165	ns
Chip Enable to End of Write	(3) TELWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETERS	SYMBOL	CONDITIONS	(NOTES 1,2,3) GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Access Time	(4) TELQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	175	ns
Address Hold Time	(5) TWHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Setup Time	(6) TAVWL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Address Valid to End of Write	(7) TAVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Address Setup Time	(8) TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Hold Time	(9) TEHAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	0	-	ns
Address Valid to End of Write	(10) TAVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Write Enable Pulse Width	(11) TWLWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Data Setup Time	(12) TDVWH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	165	-	ns
Data Hold Time	(13) TWHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	15	-	ns
Enable Pulse Width	(14) TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	175	-	ns
Write to End of Write	(15) TWLEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	165	-	ns
Data Setup Time	(16) TDVEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	165	-	ns
Data Hold Time	(17) TEHDX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	15	-	ns

NOTES:

1. All voltages referenced to device GND. Negative undershoots to a minimum of -0.3V are allowed with a maximum of 50ns pulse width.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD-1.5; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF; for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	8	pF
			1, 3, 4	$T_A = +25°C$	-	TBD	pF
Output Capacitance	CO	VDD = Open, f = 1MHz	1, 2, 4	$T_A = +25°C$	-	10	pF
			1, 3, 4	$T_A = +25°C$	-	TBD	pF
Read/Write	(1) TAVAX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	175	-	ns
Write Enable to Output in High Z	(18) TWLQZ	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	30	ns
Write Enable High to Output ON	(19) TWHQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Chip Enable to Output ON	(20) TELQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	5	-	ns
Output Enable High to Output High Z	(21) TEHQZ	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	-	30	ns
Chip Disable to Output Hold Time	(22) TEHQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	15	-	ns
Address Invalid Output Hold Time	(23) TAXQX	VDD = 4.5V and 5.5V	1	$-55°C \le T_A \le +125°C$	10	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC (Continued)

PARAMETERS	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH2	VDD = 4.5, IO = -100µA	1	-55°C ≤ T_A ≤ +125°C	VDD-0.4V	-	V
Cycle Time	TAVAX	VDD = 4.5V and 5.5V	1	-55°C ≤ T_A ≤ +125°C	175	-	ns

NOTES:

1. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All Measurements Referenced To Device Grounds

TABLE 4. POST 200K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The post irradiation test conditions and limits are the same as those listed in Tables 1 and 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Output Low Voltage	VOL	± 60mV
Output High Voltage	VOH	± 400mV
Input Leakage Current	IIL	± 100nA
	IIH	±100nA
Low Impedance Output Leakage Current	IOZL	±1µA
High Impedance Output Leakage Current	IOZH	±1µA
Standby Supply Current	IDDSB1	±30µA

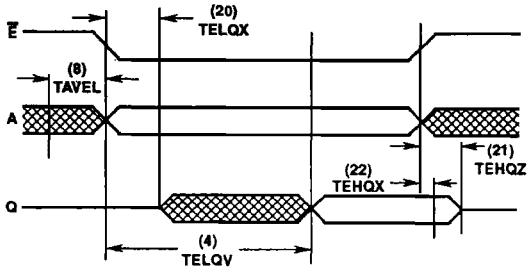
TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	-	-
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA		100%/5004	1, 7, Δ	1
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7	N/A
Group C (Optional)		Samples/5005	N/A	1, 7
Group D (Optional)		Samples/5005	1, 7	1, 7
Group E, Subgroup 2		Samples/5005	1, 7	1, 7

Timing Waveforms

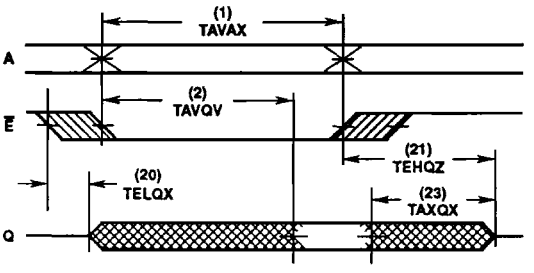
READ CYCLES

READ CYCLE 1: CONTROLLED BY E



NOTE: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until E goes high.

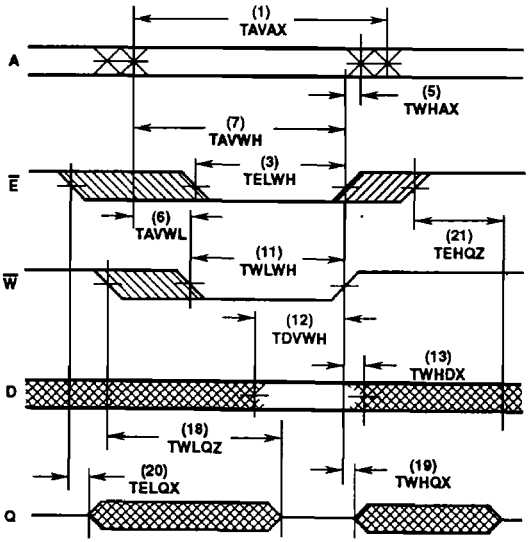
READ CYCLE 2: CONTROLLED BY ADDRESS



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ stable prior to A becoming valid and after A becomes invalid.

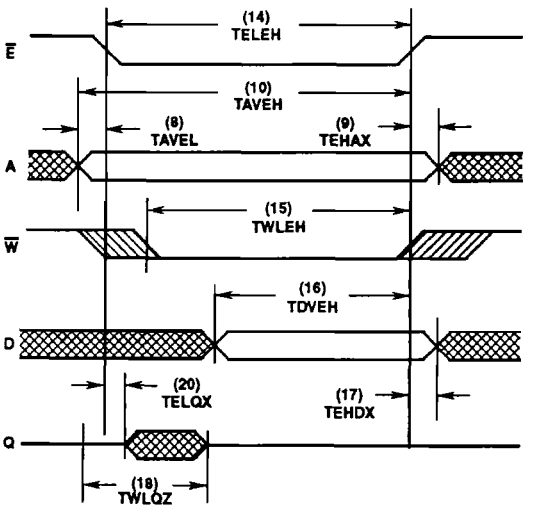
WRITE CYCLES

WRITE CYCLE 1: CONTROLLED BY $\overline{W}$ (LATE WRITE



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

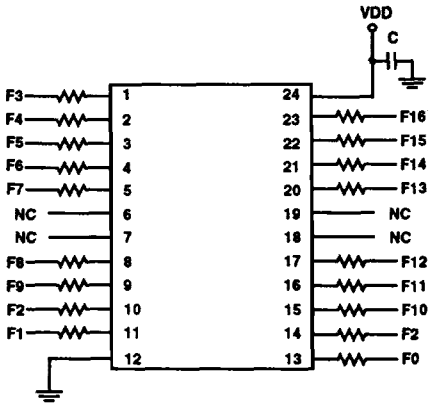
WRITE CYCLE 2: CONTROLLED BY $\overline{E}$ (EARLY WRITE)



NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding TWLQZ (Max) TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) - TWHQZ (Min), then Q will remain in the high impedance state throughtout the cycle.

Burn-In Circuits

HS-65C262RH 24 PIN FLATPACK

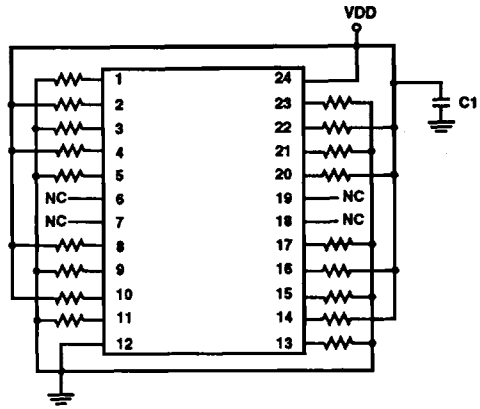


DYNAMIC CONFIGURATION

NOTES:

All Resistors = 47kΩ ± 10%
F0 = 100kHz ± 10%
F1 = F0/2 = F1/2; F3 = F2/2; F4 = F3/2 . . . F16 = F15/2
VDD = 6.0V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.8V
C = 0.01µf (min)

HS-65C262RH 24 PIN FLATPACK

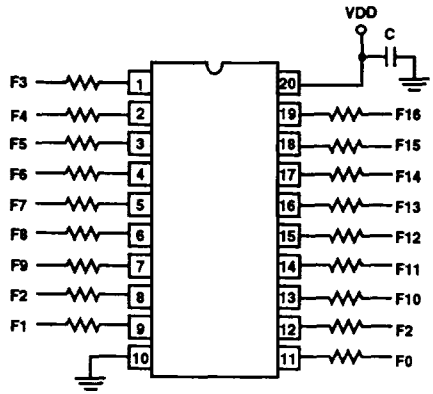


STATIC CONFIGURATION

NOTES:

All Resistors = 47kΩ ± 10%
VDD = 6.0V ± 0.5V
C1 = 0.01µf (min)

HS-65C262 20 PIN DIP

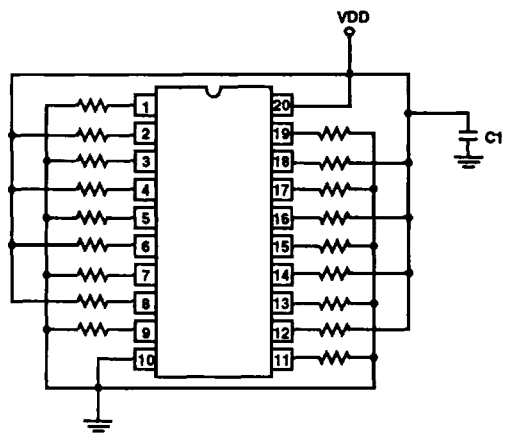


DYNAMIC CONFIGURATION

NOTES:

All Resistors = 47kΩ ± 10%
F0 = 100kHz ± 10%
F1 = F0/2 = F1/2; F3 = F2/2; F4 = F3/2 . . . F16 = F15/2
VDD = 6.0V ± 0.5V
VIH = 4.5V ± 10%
VIL = -0.2V to +0.8V
C = 0.01µf (min)

HS-65C262RH 20 PIN DIP



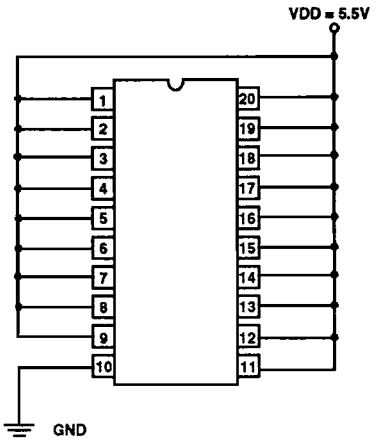
STATIC CONFIGURATION

NOTES:

All Resistors = 47kΩ ± 10%
VDD = 6.0V ± 0.5V
C1 = 0.01µf (min)

Irradiation Circuits

HS-65C262RH AND HS-65T262RH 20 PIN DIP



NOTES:

Pin 10 is tied to GND
Output (Pin 8) floats
All other pins tied to VDD
VDD = 5.5V

Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018
Wafer Lot Acceptance Method 5007
Internal Visual Inspection Method 2010, Condition A
Gamma Radiation Assurance Tests Method 1019
Nondestructive Bond Pull Method 2023
Customer Pre-Cap Visual Inspection (Note 2)
Temperature Cycling Method 1010, Condition C
Constant Acceleration Method 2001, Condition E Min, Y1
Particle Impact Noise Detection Method 2020, Condition A
Electrical Tests (Harris' Option)
Serialization
X-Ray Inspection Method 2012
Electrical Tests - Subgroup 1; Read and Record (T0)
Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.
Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)
Burn-In Delta Calculation (T0 -T1)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)
Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)
Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1
Burn-In Delta Calculation (T0 - T2)
PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ
Electrical Tests - Subgroup 3; Read and Record
Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1
Marking
Electrical Tests - Subgroup 2; Read and Record
Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1
Gross Leak Tests Method 1014, 100%
Fine Leak Tests Method 1014, 100%
Customer Source Inspection (Note 2)
Group B Inspection Method 5005 (Note 2)
End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9
Group D Inspection Method 5005 (Notes 2, 4)
End-Point Electrical Parameters: Subgroups 1, 7, 9
External Visual Inspection Method 2009
Data Package Generation (Note 5)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. For Group D, Subgroup 3 inspection of package configurations which utilizes a gold plated lid in its construction; the inspection criteria for illegible markings criteria of Method 1010, paragraph 3.3 and of Method 1004, paragraph 3.8.a shall not apply.
5. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (Including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection
Gamma Radiation Assurance Tests Method 1019
Customer Pre-Cap Visual Inspection (Note 1)
Temperature Cycling Method 1010, Condition C
Fine and Gross Leak Tests Method 1014
Constant Acceleration Method 2001 Y1 30KG
Initial Electrical Tests
Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C
+25°C Electrical Tests - Subgroups 1, 7, 9
PDA Calculation 5% Subgroups 1, 7
Electrical Tests +125°C, -55°C
Group A Inspection Method 5005. 5% PDA (Note 3)
Brand
Customer Source Inspection (Note 1)
Group C Inspection Method 5005 (Notes 1, 2)
Group D Inspection Method 5005 (Notes 1, 2)
External Visual Inspection Method 2009
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B and D data package contains Attributes Data plus Variables Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Metallization Topology

DIE DIMENSIONS:
258 x 177 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 13kÅ ± 1.5kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Braze Seal DIP - 460°C (Max)
Braze Seal Flatpack - 460°C (Max)

WORST CASE CURRENT DENSITY:
1.6×10^5 A/cm^2

SUBSTRATE POTENTIAL: VDD

Metallization Mask Layout

HS-65C262 AND HS-65T262RH