TSI-16 Time-Slot Interchanger Hardware Design Guide

Introduction

This document describes the hardware interfaces to Agere Systems Inc. TSI-16 device. Information relevant to the use of the device in a board design is covered. Ball descriptions, dc electrical characteristics, timing diagrams, ac timing parameters, packaging, and operating conditions are included.

Related Documents

More information on the TSI-16 is contained in the following documents:

- TSI-16 Product Description
- TSI-16 Register Description
- TSI-16 Systems Design Guide

Description

Block Diagram and High-Level Interface Definition

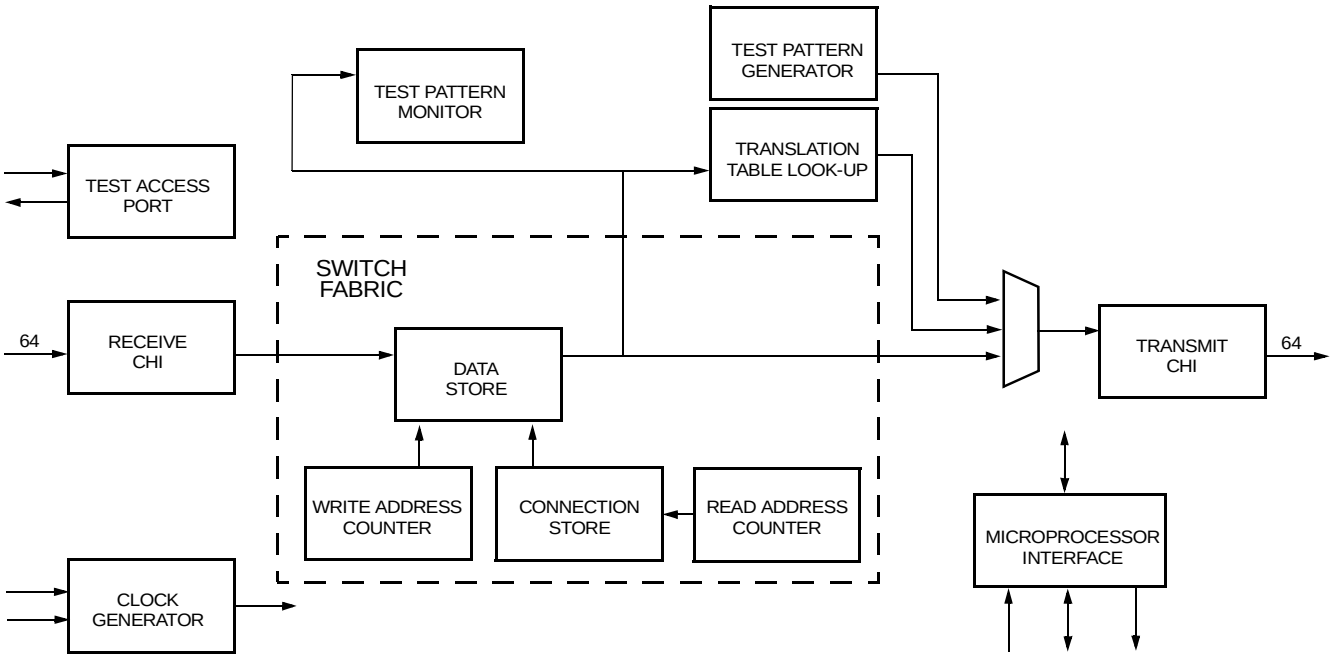

Figure 1. Block Diagram and High-Level Interface Definition

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Ball Information

Ball Diagram

The TSI-16 is housed in a 324-ball plastic ball grid array. Figure 2 shows the ball arrangement viewed from the top of the package. The balls are spaced on a 1.0 mm pitch.

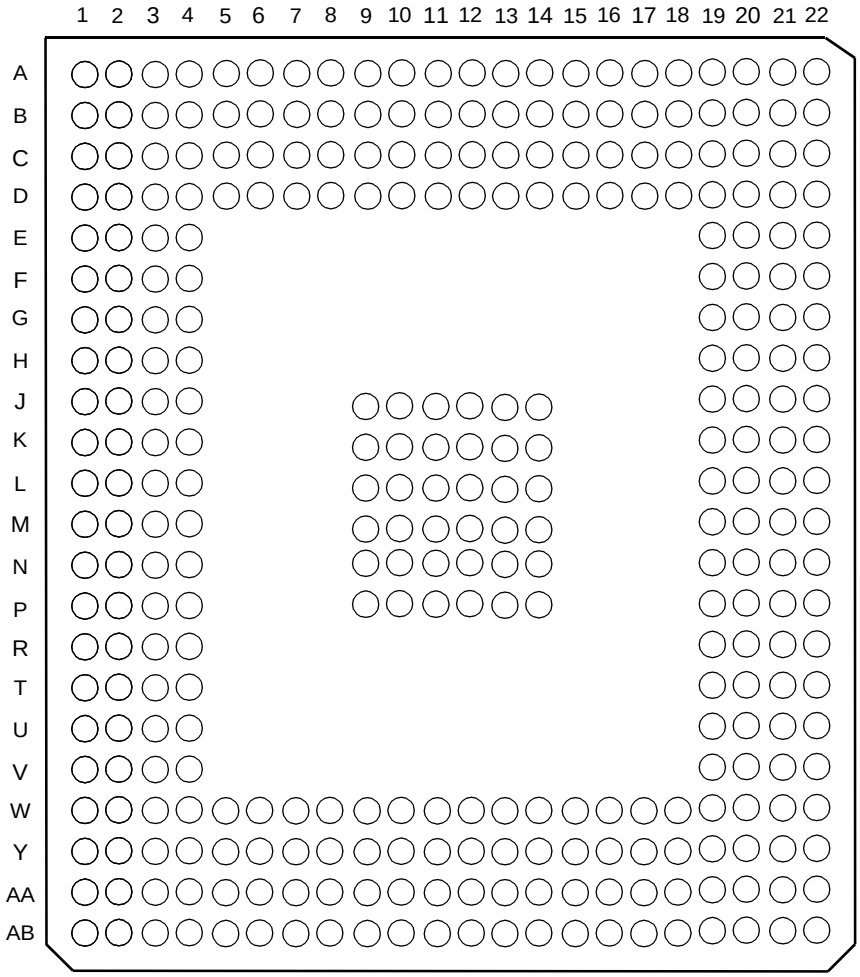


Figure 2. Package Diagram (Top View)

Ball Information (continued)

Package Ball Assignments

Table 1. Package Ball Assignments in Signal Name Order

Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball
ADDR00	A19	DATA13	U22	RXD11	W9	RXD45	W10	TXD10	H1
ADDR01	A18	DATA14	U21	RXD12	Y9	RXD46	AA11	TXD11	J2
ADDR02	A17	DATA15	V22	RXD13	AB10	RXD47	AB12	TXD12	J1
ADDR03	A16	$\overline{DT}$	J21	RXD14	Y10	RXD48	Y11	TXD13	K2
ADDR04	A15	FSYNC	AA16	RXD15	AB11	RXD49	AB13	TXD14	K1
ADDR05	A14	$\overline{HIZ}$	Y22	RXD16	W11	RXD50	W12	TXD15	L1
ADDR06	A13	$\overline{INT}$	K22	RXD17	AA12	RXD51	AB14	TXD16	M1
ADDR07	A12	MPUCLK	M19	RXD18	Y12	RXD52	AA14	TXD17	N1
ADDR08	A11	PAR0	W22	RXD19	AA13	RXD53	AB15	TXD18	N2
ADDR09	A10	PAR1	V21	RXD20	Y13	RXD54	Y14	TXD19	P1
ADDR10	A9	R/$\overline{W}$	L21	RXD21	W13	RXD55	W14	TXD20	P2
ADDR11	A8	$\overline{RESET}$	K21	RXD22	AA15	RXD56	Y15	TXD21	R1
ADDR12	A7	RSV1	F22	RXD23	AB16	RXD57	AB18	TXD22	T1
ADDR13	A6	RSV2	G20	RXD24	AB17	RXD58	AA18	TXD23	T2
ADDR14	A5	RSV3	F21	RXD25	AA17	RXD59	Y17	TXD24	U1
ADDR15	A4	RSV4	E22	RXD26	Y16	RXD60	AB20	TXD25	V1
$\overline{AS}$	L20	RSV5	F20	RXD27	AB19	RXD61	W17	TXD26	V2
CHICLK	V19	RSV6	D21	RXD28	AA19	RXD62	AB21	TXD27	W1
CKSPD0	E21	RSV7	D20	RXD29	AA20	RXD63	W18	TXD28	W2
CKSPD1	D22	RSV8	C21	RXD30	Y18	TCK	H22	TXD29	Y1
$\overline{CS}$	K20	RSV9	E20	RXD31	Y19	TDI	H21	TXD30	Y2
DATA00	L22	RSV10	W21	RXD32	AB3	TDO	G22	TXD31	AA1
DATA01	M21	RSV11	AA22	RXD33	Y4	TMS	J22	TXD32	D3
DATA02	M22	RXD00	AA3	RXD34	AB4	TRSTN	J20	TXD33	E3
DATA03	N21	RXD01	W5	RXD35	W6	TXD00	B1	TXD34	E4
DATA04	N22	RXD02	AA4	RXD36	AB5	TXD01	C2	TXD35	F3
DATA05	P21	RXD03	Y5	RXD37	Y6	TXD02	C1	TXD36	F4
DATA06	P20	RXD04	AA5	RXD38	AB6	TXD03	D2	TXD37	F2
DATA07	P22	RXD05	AA6	RXD39	Y7	TXD04	D1	TXD38	G4
DATA08	R21	RXD06	W7	RXD40	W8	TXD05	E2	TXD39	G3
DATA09	R22	RXD07	AA7	RXD41	Y8	TXD06	E1	TXD40	H3
DATA10	T22	RXD08	AB7	RXD42	AA9	TXD07	F1	TXD41	H2
DATA11	T21	RXD09	AA8	RXD43	AB9	TXD08	G2	TXD42	J3
DATA12	T20	RXD10	AB8	RXD44	AA10	TXD09	G1	TXD43	J4

Ball Information (continued)

Package Ball Assignments (continued)

Table 1. Package Ball Assignments in Signal Name Order (continued)

Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball
TXD44	K3	VDD15	M9	VIO	M2	VSS	C9	VSS	N13
TXD45	K4	VDD15	M10	VPRE	AB2	VSS	C10	VSS	N14
TXD46	L2	VDD15	M13	VSS	A1	VSS	C13	VSS	N20
TXD47	L3	VDD15	M14	VSS	A21	VSS	C14	VSS	P9
TXD48	M3	VDD15	N11	VSS	A22	VSS	C15	VSS	P10
TXD49	M4	VDD15	N12	VSS	AA2	VSS	C16	VSS	P13
TXD50	N4	VDD15	P11	VSS	AA21	VSS	C17	VSS	P14
TXD51	N3	VDD15	P12	VSS	AB1	VSS	C20	VSS	R4
TXD52	P3	VDD33	A2	VSS	AB22	VSS	D6	VSS	R19
TXD53	P4	VDD33	A3	VSS	B2	VSS	D10	VSS	R20
TXD54	R2	VDD33	A20	VSS	B3	VSS	D13	VSS	U19
TXD55	R3	VDD33	C4	VSS	B4	VSS	D17	VSS	U20
TXD56	T3	VDD33	C5	VSS	B5	VSS	E19	VSS	V20
TXD57	U2	VDD33	C11	VSS	B6	VSS	F19	VSS	W20
TXD58	T4	VDD33	C12	VSS	B7	VSS	G21	VSS	Y3
TXD59	U4	VDD33	C18	VSS	B8	VSS	H4	VSS	Y20
TXD60	U3	VDD33	C19	VSS	B9	VSS	H19	VSS	Y21
TXD61	V3	VDD33	C22	VSS	B10	VSS	J9	VSSPLL	W15
TXD62	W3	VDD33	D4	VSS	B11	VSS	J10		
TXD63	V4	VDD33	D5	VSS	B12	VSS	J13		
VDD15	D7	VDD33	D11	VSS	B13	VSS	J14		
VDD15	D8	VDD33	D12	VSS	B14	VSS	J19		
VDD15	D9	VDD33	D18	VSS	B15	VSS	K9		
VDD15	D14	VDD33	D19	VSS	B16	VSS	K10		
VDD15	D15	VDD33	G19	VSS	B17	VSS	K13		
VDD15	D16	VDD33	H20	VSS	B18	VSS	K14		
VDD15	J11	VDD33	K19	VSS	B19	VSS	L11		
VDD15	J12	VDD33	L4	VSS	B20	VSS	L12		
VDD15	K11	VDD33	N19	VSS	B21	VSS	L19		
VDD15	K12	VDD33	P19	VSS	B22	VSS	M11		
VDD15	L9	VDD33	T19	VSS	C3	VSS	M12		
VDD15	L10	VDD33	W4	VSS	C6	VSS	M20		
VDD15	L13	VDD33	W19	VSS	C7	VSS	N9		
VDD15	L14	VDDPLL	W16	VSS	C8	VSS	N10		

Ball Information (continued)

Package Ball Assignments (continued)

Table 2. Package Ball Assignments in Ball Number Order (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	VSS	VDD33	VDD33	ADDR15	ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR09	ADDR08	ADDR07	ADDR06	ADDR05	ADDR04	ADDR03	ADDR02	ADDR01	ADDR00	VDD33	VSS	VSS
B	TXD00	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
C	TXD02	TXD01	VSS	VDD33	VDD33	VSS	VSS	VSS	VSS	VSS	VDD33	VDD33	VSS	VSS	VSS	VSS	VSS	VDD33	VDD33	VSS	RSV8	VDD33
D	TXD04	TXD03	TXD32	VDD33	VDD33	VSS	VDD15	VDD15	VDD15	VSS	VDD33	VDD33	VSS	VDD15	VDD15	VDD15	VSS	VDD33	VDD33	RSV7	RSV6	CKSPD1
E	TXD06	TXD05	TXD33	TXD34	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	RSV9	CKSPD0	RSV4
F	TXD07	TXD37	TXD35	TXD36	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	RSV5	RSV3	RSV1
G	TXD09	TXD08	TXD39	TXD38	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	RSV2	VSS	TDO
H	TXD10	TXD41	TXD40	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	VDD33	TDI	TCK
J	TXD12	TXD11	TXD42	TXD43	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	VSS	TRSTN	$\overline{DT}$	TMS
K	TXD14	TXD13	TXD44	TXD45	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	VDD33	$\overline{CS}$	$\overline{RESET}$	$\overline{INT}$
L	TXD15	TXD46	TXD47	VDD33	—	—	—	—	VDD15	VDD15	VSS	VSS	VDD15	VDD15	—	—	—	—	VSS	$\overline{AS}$	R/$\overline{W}$	DATA00
M	TXD16	VIO	TXD48	TXD49	—	—	—	—	VDD15	VDD15	VSS	VSS	VDD15	VDD15	—	—	—	—	MPU-CLK	VSS	DATA01	DATA02
N	TXD17	TXD18	TXD51	TXD50	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	VDD33	VSS	DATA03	DATA04
P	TXD19	TXD20	TXD52	TXD53	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	VDD33	DATA06	DATA05	DATA07
R	TXD21	TXD54	TXD55	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	VSS	DATA08	DATA09
T	TXD22	TXD23	TXD56	TXD58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	DATA12	DATA11	DATA10
U	TXD24	TXD57	TXD60	TXD59	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	VSS	DATA14	DATA13
V	TXD25	TXD26	TXD61	TXD63	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHICLK	VSS	PAR1	DATA15
W	TXD27	TXD28	TXD62	VDD33	RXD01	RXD35	RXD06	RXD40	RXD11	RXD45	RXD16	RXD50	RXD21	RXD55	VSSPLL	VDDPLL	RXD61	RXD63	VDD33	VSS	RSV10	PAR0
Y	TXD29	TXD30	VSS	RXD33	RXD03	RXD37	RXD39	RXD41	RXD12	RXD14	RXD48	RXD18	RXD20	RXD54	RXD56	RXD26	RXD59	RXD30	RXD31	VSS	VSS	$\overline{HIZ}$
AA	TXD31	VSS	RXD00	RXD02	RXD04	RXD05	RXD07	RXD09	RXD42	RXD44	RXD46	RXD17	RXD19	RXD52	RXD22	FSYNC	RXD25	RXD58	RXD28	RXD29	VSS	RSV11
AB	VSS	VPRE	RXD32	RXD34	RXD36	RXD38	RXD08	RXD10	RXD43	RXD13	RXD15	RXD47	RXD49	RXD51	RXD53	RXD23	RXD24	RXD57	RXD27	RXD60	RXD62	VSS

Ball Information (continued)

Package Ball Assignments (continued)

Table 3. Package Ball Assignments in Ball Number Order (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
AB	VSS	VPRE	RXD32	RXD34	RXD36	RXD38	RXD08	RXD10	RXD43	RXD13	RXD15	RXD47	RXD49	RXD51	RXD53	RXD23	RXD24	RXD57	RXD27	RXD60	RXD62	VSS
AA	TXD31	VSS	RXD00	RXD02	RXD04	RXD05	RXD07	RXD09	RXD42	RXD44	RXD46	RXD17	RXD19	RXD52	RXD22	FSYNC	RXD25	RXD58	RXD28	RXD29	VSS	RSV11
Y	TXD29	TXD30	VSS	RXD33	RXD03	RXD37	RXD39	RXD41	RXD12	RXD14	RXD48	RXD18	RXD20	RXD54	RXD56	RXD26	RXD59	RXD30	RXD31	VSS	VSS	$\overline{\text{HIZ}}$
W	TXD27	TXD28	TXD62	VDD33	RXD01	RXD35	RXD06	RXD40	RXD11	RXD45	RXD16	RXD50	RXD21	RXD55	VSSPLL	VDDPLL	RXD61	RXD63	VDD33	VSS	RSV10	PAR0
V	TXD25	TXD26	TXD61	TXD63	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHICLK	VSS	PAR1	DATA15
U	TXD24	TXD57	TXD60	TXD59	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	VSS	DATA14	DATA13
T	TXD22	TXD23	TXD56	TXD58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	DATA12	DATA11	DATA10
R	TXD21	TXD54	TXD55	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	VSS	DATA08	DATA09
P	TXD19	TXD20	TXD52	TXD53	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	VDD33	DATA06	DATA05	DATA07
N	TXD17	TXD18	TXD51	TXD50	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	VDD33	VSS	DATA03	DATA04
M	TXD16	VIO	TXD48	TXD49	—	—	—	—	VDD15	VDD15	VSS	VSS	VDD15	VDD15	—	—	—	—	MPU-CLK	VSS	DATA01	DATA02
L	TXD15	TXD46	TXD47	VDD33	—	—	—	—	VDD15	VDD15	VSS	VSS	VDD15	VDD15	—	—	—	—	VSS	$\overline{\text{AS}}$	R/$\overline{\text{W}}$	DATA00
K	TXD14	TXD13	TXD44	TXD45	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	VDD33	$\overline{\text{CS}}$	$\overline{\text{RESET}}$	$\overline{\text{INT}}$
J	TXD12	TXD11	TXD42	TXD43	—	—	—	—	VSS	VSS	VDD15	VDD15	VSS	VSS	—	—	—	—	VSS	TRSTN	$\overline{\text{DT}}$	TMS
H	TXD10	TXD41	TXD40	VSS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	VDD33	TDI	TCK
G	TXD09	TXD08	TXD39	TXD38	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD33	RSV2	VSS	TDO
F	TXD07	TXD37	TXD35	TXD36	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	RSV5	RSV3	RSV1
E	TXD06	TXD05	TXD33	TXD34	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS	RSV9	CKSPD0	RSV4
D	TXD04	TXD03	TXD32	VDD33	VDD33	VSS	VDD15	VDD15	VDD15	VSS	VDD33	VDD33	VSS	VDD15	VDD15	VDD15	VSS	VDD33	VDD33	RSV7	RSV6	CKSPD1
C	TXD02	TXD01	VSS	VDD33	VDD33	VSS	VSS	VSS	VSS	VSS	VDD33	VDD33	VSS	VSS	VSS	VSS	VSS	VDD33	VDD33	VSS	RSV8	VDD33
B	TXD00	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
A	VSS	VDD33	VDD33	ADDR15	ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR09	ADDR08	ADDR07	ADDR06	ADDR05	ADDR04	ADDR03	ADDR02	ADDR01	ADDR00	VDD33	VSS	VSS

Ball Information (continued)

Ball Types

This table describes each type of input, output, and I/O ball used on the TSI-16.

Table 4. Ball Types

Type Label	Description
I	CMOS input, TTL switching thresholds.
I pd	CMOS input, TTL switching thresholds with internal pull-down resistor.
I pu	CMOS input, TTL switching thresholds with internal pull-up resistor.
O	CMOS output.
O od	Open drain output.
I/O	Bidirectional ball; CMOS input with TTL switching thresholds and CMOS output.
None	Analog inputs for external resistors, capacitors, voltage references, etc.
P	Power and ground.

The dc switching and other electrical characteristics are specified later in this document.

Ball Definitions

This section describes the function of each of the device balls. The balls are listed by ball name. Package ball numbers are listed in Table 1 of this document. The static parameters (drive currents, switching thresholds, etc.) for each ball type (input, output, etc.) are described in Table 14 through Table 17.

Table 5. Timing Port

Ball Name	Type	Name/Description
FSYNC	I	**Frame Synchronization.** This signal indicates the beginning of a 125 µs frame event (8 kHz). The FSYNC ball can be programmed as active-low or active-high, but its polarity is the same for all concentration highway interfaces (CHI). FSYNC can be sampled on either the positive or negative edge of CHICLK. Time-slot numbers and bit offsets for each CHI are assigned relative to the detection of FSYNC.
CHICLK	I	**Clock.** This is the master synchronous clock for the transmit and receive concentration highways. The frequency can be 8.192 MHz or 16.384 MHz. It **must** be at least as fast as the highest CHI data rate.
CKSPD0	I	**Clock Speed.** Static control input that should be tied according to the frequency of CHICLK. If CHICLK is connected to an 8.192 MHz source, CKSPD0 should be tied to V_{SS}. If CHICLK is connected to a 16.384 MHz source, CKSPD0 should be tied to V_{DD33}.
CKSPD1	I pd	**Clock Speed.** Reserved, leave disconnected. 20 kΩ pull-down resistor.

Ball Information (continued)

Ball Definitions (continued)

Table 6. Transmit and Receive Concentration Highways

Ball Name	Type	Name/Description
RXD[63:00]	I pd	**Receive Data [63:0].** Receive concentration highways. These are serial, synchronous data streams which may be individually programmed to operate at 2.048 Mbits/s, 4.096 Mbits/s, 8.192 Mbits/s, or 16.384 Mbits/s. They carry 32, 64, 128, or 256 time slots (respectively) each occupying eight contiguous bits. 20 kΩ pull-down resistor.
TXD[63:32]	I/O	**Transmit Data [63:32].** Normally these are output concentration highway data streams with data rate options identical to the RXD inputs. These balls can be configured to operate as bidirectional multiplex ports. Further information can be found in the system design guide. 20 kΩ pull-down resistor.
TXD[31:00]	I/O	**Transmit Data [31:00].** Normally these are output concentration highway data streams with data rate options identical to the RXD inputs. These balls can be configured to operate as bidirectional multiplex ports such as H.110. Further information can be found in the system design guide. 20 kΩ resistor connected to VPRE.

Table 7. Control Port

Ball Name	Type	Name/Description
MPUCLK	I	**Processor Clock.** This clock is used to sample address, data, and control signals from the microprocessor. This clock must be within the range of 0 MHz—66 MHz. Required for operation.
$\overline{CS}$	I	**Chip Select.** Active-low chip select. This input is held low for the duration of any read or write access to the TSI-16. Required for operation.
$\overline{AS}$	I	**Address Strobe.** Active-low address strobe that is one MPUCLK cycle wide at the start of a microprocessor access cycle to the TSI-16. This is used to initiate a microprocessor access. Required for operation.
R/$\overline{W}$	I	**Read/Write.** Cycle selection. R/$\overline{W}$ is set high during a read cycle, or set low for a write cycle. Required for operation.
ADDR [15:00]	I pu	**Address [15:00].** ADDR[15] is the most significant bit and ADDR[00] is the least significant bit for addressing all the internal registers during microprocessor access cycles. All addresses are 16-bit word addresses; hence, in a typical application ADDR[00] of the TSI-16 device would be connected to address bit 1 of a byte addressable system address bus. Required for operation. 200 kΩ pull-up resistor. **Note:** The TSI-16 is little-endian; the least significant byte is stored in the lowest address and the most significant byte is stored in the highest address. Care must be exercised in connection to microprocessors that use big-endian byte ordering.
DATA [15:00]	I/O	**Data [15:00].** Data bus for all transfers between the microprocessor and the internal registers. The balls are inputs during write cycles and outputs during read cycles. DATA[15] is the most significant bit, and DATA[00] is the least significant bit. Required for operation.
PAR[1:0]	I/O	**Control Port Parity [1:0].** Byte-wide parity bits for data. PAR[1] is the parity for DATA[15:8], and PAR[0] is the parity for DATA[7:0]. The parity sense (even or odd) is application programmable via a register bit in the TSI-16. **Not** required for operation.
$\overline{DT}$	O	**Data Transfer Acknowledge.** Active-low for one MPUCLK cycle. Indicates that data has been written during write cycles or that data is valid during read cycles. High impedance when $\overline{CS}$ is a 1 and driven when $\overline{CS}$ is 0. Required for operation.
$\overline{INT}$	O od	**Interrupt.** This output is asserted low to indicate that an interrupt condition has occurred. This signal remains active-low until the interrupt status register has been cleared or masked.

Ball Information (continued)

Ball Definitions (continued)

Table 8. Initialization and Test Access

Ball Name	Type	Name/Description
$\overline{\text{RESET}}$	I pu	**Reset.** Global reset, active-low. Initializes all internal registers to their default state. The reset occurs asynchronously, but $\overline{\text{RESET}}$ should be held low for at least two CHICLK periods. 20 kΩ pull-up resistor.
TCK	I pu	**Test Clock.** This signal provides timing for the boundary scan and test access port (TAP) controller. Should be static except during boundary-scan testing. 20 kΩ pull-up resistor.
TDI	I pu	**Test Data In.** Data input for the boundary scan. Sampled on the rising edge of TCK. 20 kΩ pull-up resistor.
TMS	I pu	**Test Mode Select (Active-Low).** Controls boundary-scan test operations. TMS is sampled on the rising edge of TCK. 20 kΩ pull-up resistor.
TRSTN	I pd	**Test Reset (Active-Low).** This signal is an asynchronous reset for the TAP controller. 20 kΩ pull-down resistor.
TDO	O	**Test Data Out.** Updated on the falling edge of TCK. The TDO output is high impedance except when scanning out test data.
$\overline{\text{HIZ}}$	I pu	**Output Enable.** All output and bidirectional buffers will be high impedance when this input is low unless boundary scan is enabled (TRSTN = 1). 20 kΩ pull-up resistor.
RSV[11:1]	—	**Reserved [11:1].** These balls are used by Agere Systems during the manufacturing process. They must be left unconnected.

Table 9. Power Balls

Symbol	Type	Name/Description
V_{DD33}	P	**I/O Power.** Power supply balls for the I/O pads (3.3 V ± 5%).
V_{DD15}	P	**Core Power.** Power supply balls for the core (1.5 V ± 5%).
VSS	P	**Ground.** Common ground balls for 3.3 V and 1.5 V supplies.
V_{PRE}	P	**Precharge.** Precharge voltage to support H.110 hot insertion on TXD[31:00]. If the device is used in an H.110 hot insertion applications, the signal should be connected to backplane early voltage; otherwise connect this signal to ground.
V_{IO}	P	**PCI Buffer Voltage Select.** For an H.110 application using TXD[31:00] in a 5 V signaling environment, connect this signal to 5 V. For an H.110 application using TXD[31:00] in a 3 V signaling environment, connect this signal to V_{DD33}. For all other applications, connect this signal to V_{DD33}.
V_{DDPLL}	P	**PLL Power.** 1.5 V power supply for the internal phase-locked loop. Must include local 0.01 µF capacitor to V_{SSPLL}.
V_{SSPLL}	P	**PLL Ground.** Isolated ground for the internal phase-locked loop.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 10. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage (V_{DD33})	–0.5	4.2	V
Supply Voltage (V_{DD15})	–0.5	1.8	V
Input Voltage: TXD[63:00] All Other Inputs	 –0.5 –0.3	 5.5 V_{DD33} + 0.3	V
Storage Temperature	–40	125	°C
Junction Temperature	—	125	°C

Handling Precautions

Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs both a human-body model (HBM) and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114 (HBM) and JESD22-C101 (CDM) standards.

ESD Tolerance

Table 11. ESD Tolerance

Device	Voltage	Type
TSI-16	2,000 V	HBM (human-body model)
	500 V	CDM (charged-device model)

Package Thermal Characteristics

- Θ_{JA} = 20 °C/W.

Table 12. Power Consumption

Supply Voltage	Typ*	Max
V_{DD33}	200 mW at 3.3 V	250 mW at 3.47 V
V_{DD15}	300 mW at 1.5 V	350 mW at 1.6 V

* MPUCLK = 66 MHz, CHICLK = 16.384 MHz, TA = 25 °C, all CHIs active, all outputs loaded with 50 pF.

Recommended Operating Conditions

Recommended conditions apply unless otherwise specified.

Table 13. Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage (V_{DD33})	3.14	3.3	3.47	V
Supply Voltage (V_{DD15})	1.4	1.5	1.6	V
Ambient Temperature	–40	—	85	°C

dc Electrical Characteristics

This section describes all the static parameters associated with all the ball types used in the TSI-16 device.

Table 14. CMOS Inputs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{IL}	$V_{SS} < V_{IN} < V_{DD33}$	—	—	1*	µA
High-input Voltage	V_{IH}	—	2.0	—	V_{DD33} + 0.3	V
Low-input Voltage	V_{IL}	—	–0.3	—	0.8	V
Input Capacitance	C_I	—	—	2.5	—	pF

* Excludes current due to pull-up or pull-down resistors.

Table 15. CMOS Outputs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage Low	V_{OL}	I_{OL} = –10 mA	—	—	0.4	V
Output Voltage High	V_{OH}	I_{OL} = 10 mA	2.4	—	—	V
Output Current Low	I_{OL}	—	—	—	10	mA
Output Current High	I_{OH}	—	—	—	10	mA
Output Capacitance	C_O	—	—	3	—	pF
HIZ Output Leakage Current	I_{OZ}	—	—	—	10	µA

dc Electrical Characteristics (continued)

Table 16. CMOS Bidirectionals (Excluding TXD[63:00])

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Leakage Current	I_L	$V_{SS} < V_{IN} < V_{DD33}$	—	—	11	µA
High-input Voltage	V_{IH}	—	2.0	—	V_{DD33} + 0.3	V
Low-input Voltage	V_{IL}	—	–0.3	—	0.8	V
Biput Capacitance	C_{IB}	—	—	5.0	—	pF
Output Voltage Low	V_{OL}	I_{OL} = –10 mA	—	—	0.4	V
Output Voltage High	V_{OH}	I_{OL} = 10 mA	2.4	—	—	V

Table 17. CMOS Bidirectionals (TXD[63:00])

Parameter	Symbol	Conditions	Min	Max	Unit
Leakage Current	I_L	$V_{SS} < V_{IN} < V_{DD33}$	—	10	µA
High-input Voltage	V_{IH}	VIO = 5.0 V VIO = 3.3V	2.0 0.5 V_{DD33}	5.5 V_{DD33} + 0.5	V
Low-input Voltage	V_{IL}	VIO = 5.0 V VIO = 3.3V	–0.5 –0.5	0.8 0.3 V_{DD33}	V
Biput Capacitance	C_{IB}	—	—	10	pF
Output Voltage Low	V_{OL}	I_{OL} = 1.5 mA, VIO = 3.3 V I_{OL} = 6.0 mA, VIO = 5.0 V	— —	0.1 V_{DD33} 0.55	V
Output Voltage High	V_{OH}	I_{OL} = –0.5 mA, VIO = 3.3 V I_{OL} = –2.0 mA, VIO = 5.0 V	0.9 V_{DD33} 2.4	— —	V
Positive-going Threshold	V_{t+}	—	1.2	2.0	V
Negative-going Threshold	V_{t-}	—	0.6	1.6	V
Hysteresis ($V_{t+} – V_{t-}$)	V_{HYS}	—	0.4	—	V

Timing Diagrams and ac Characteristics

Figure 3 and Figure 4 describe the timing specifications for the input clocks on the TSI-16.

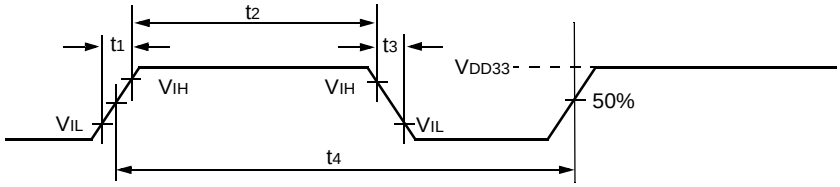


Figure 3. CHICLK Timing Specifications

Table 18. CHICLK Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t1	CHICLK Rise Time	—	2	7	ns
t2	CHICLK Width (8.192 MHz)*	48.84	—	73.24	ns
t2	CHICLK Width (16.384 MHz)*	24.42	—	36.62	ns
t3	CHICLK Fall Time	—	2	7	ns
t4	CHICLK Period (8.192 MHz)	—	122.07	—	ns
t4	CHICLK Period (16.384 MHz)	—	61.03	—	ns

* VIH to VIH or VIL to VIL.

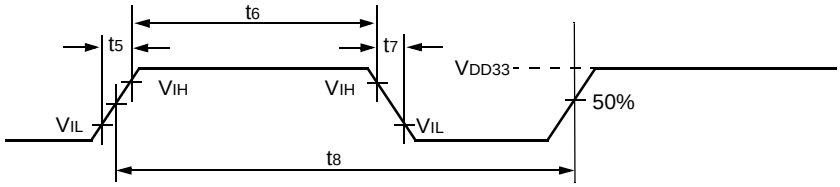


Figure 4. MPUCLK Timing Specifications

Table 19. MPUCLK Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t5	MPUCLK Rise Time	—	2	7	ns
t6	MPUCLK Width*	6.06	—	—	ns
t7	MPUCLK Fall Time	—	2	7	ns
t8	MPUCLK Period	15.2	—	—	ns

* VIH to VIH or VIL to VIL.

Timing Diagrams and ac Characteristics (continued)

Figure 5 shows the ac timing specifications for the TSI-16. All timing parameters are referenced to V_{IHmin} and V_{ILmax}. The reference signal polarity may be inverted for some timing parameters.

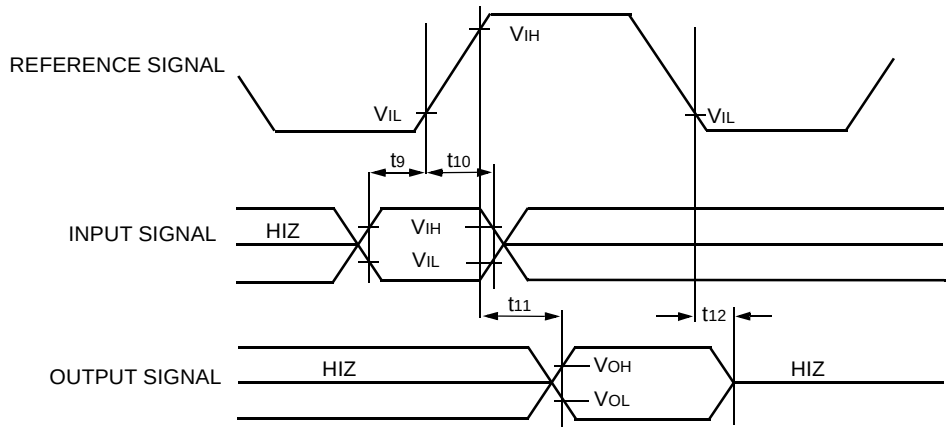
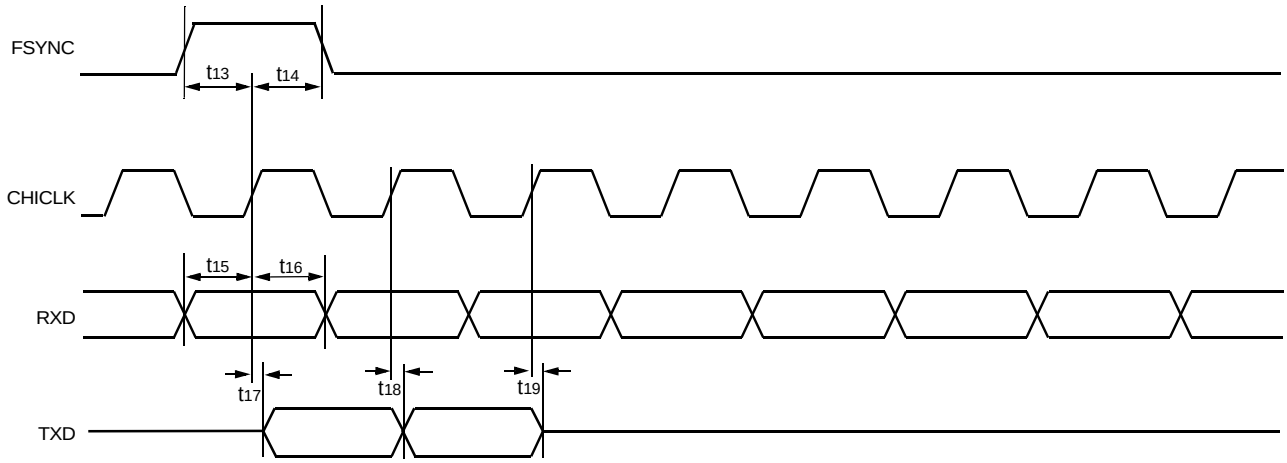


Figure 5. ac Timing Measurement Specification

Table 20. ac Timing Measurement Specification

Parameter	Description
t_9	Setup Time
t_{10}	Hold Time
t_{11}	Output Delay
t_{12}	Output 3-State Time

Timing Diagrams and ac Characteristics (continued)



Note: This figure assumes TSI-16 is programmed to sample FSYNC on rising edge of CHICLK.

Figure 6. CHI Interface Timing

Table 21. CHI Interface Timing

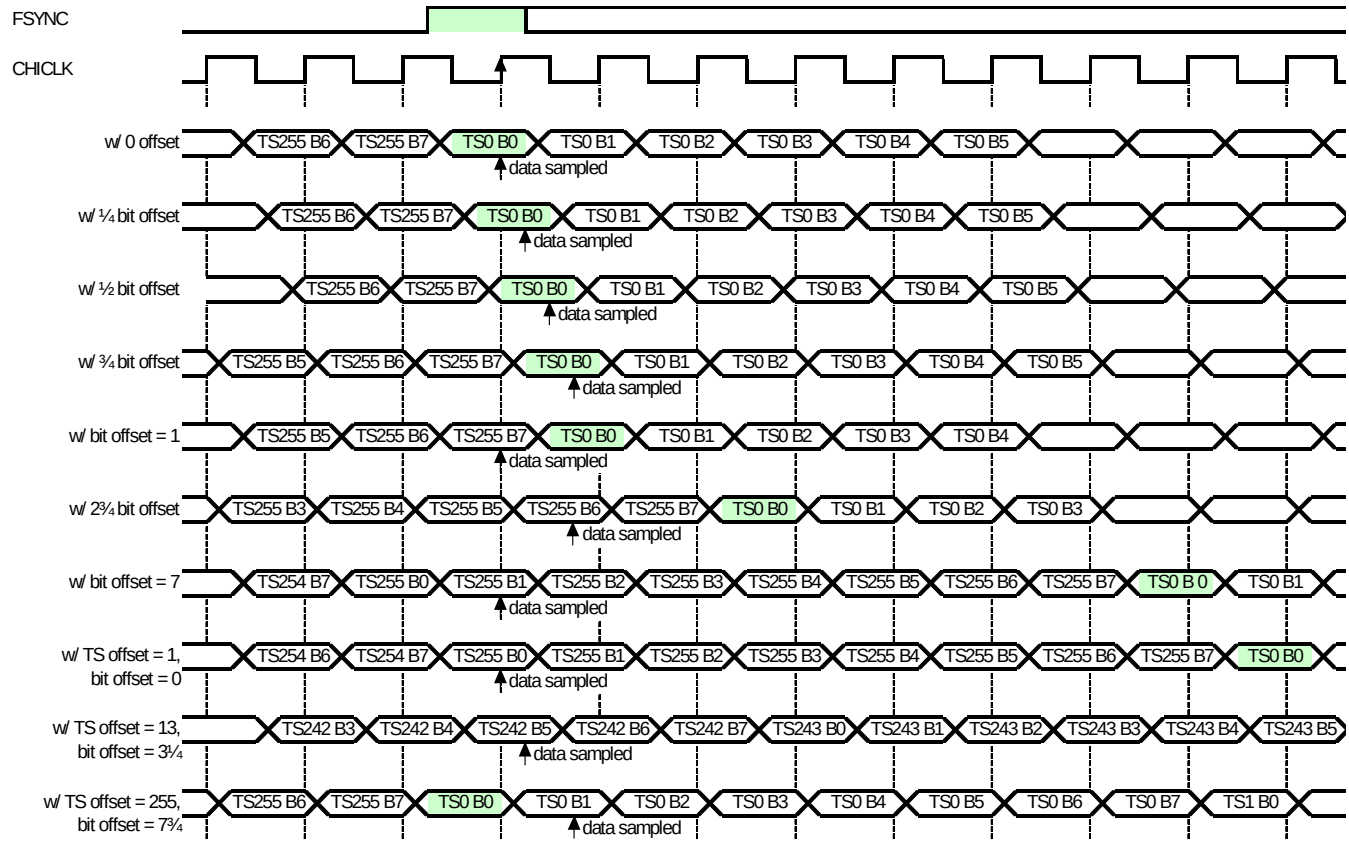
Parameter	Description	Min	Max	Unit
t_{13}	FSYNC Setup Time to Active CHICLK Edge	10	—	ns
t_{14}	FSYNC Hold Time from Active CHICLK Edge	5	—	ns
t_{15}	RXD Setup to Active CHICLK Edge	10	—	ns
t_{16}	RXD Hold Time from Active CHICLK Edge	5	—	ns
t_{17}	TXD High Z to Data Valid	—	15	ns
t_{18}	TXD Propagation Delay from Active CHICLK Edge	2	12	ns
t_{19}	Transmit Data High Impedance*	—	15	ns

* Applies if Driver_Enable_Control = 01; see Figure 17, CHI 3-state Output Control, if Driver_Enable_Control = 11.

All timing specifications are with respect to V_{IHmin} and V_{ILmax} as shown in Figure 5. All timing specifications also apply under the following conditions:

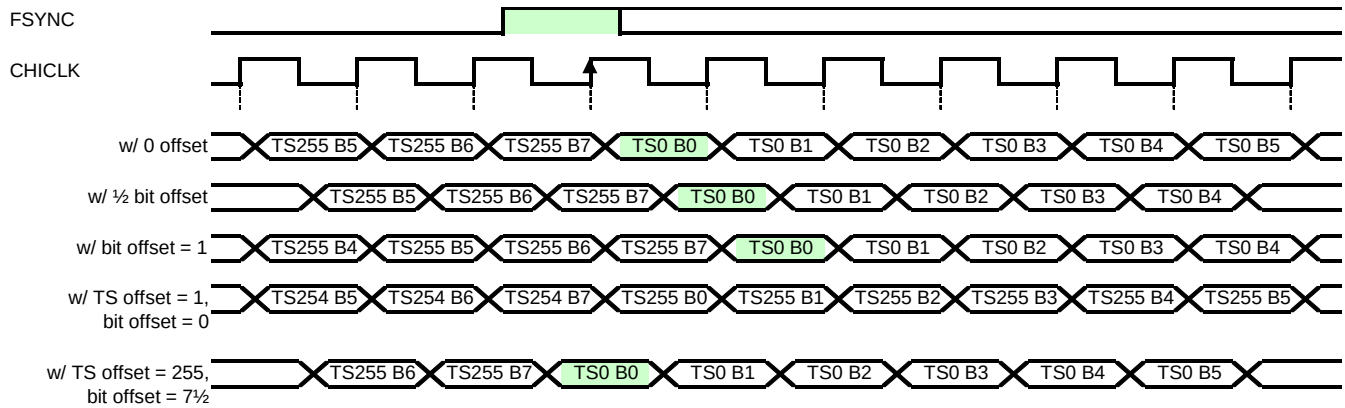
- If FS is active-low.
- If the falling edge of CHICLK is specified as the active edge.
- At all RXD and TXD rates (16.384 Mbits/s, 8.192 Mbits/s, 4.096 Mbits/s, or 2.048 Mbits/s) with a CHICLK frequency of 16.384 MHz or 8.192 MHz.

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

Figure 7. Typical Receive CHI Timing with 16.384 Mbits/s Data and 16.384 MHz CHICLK

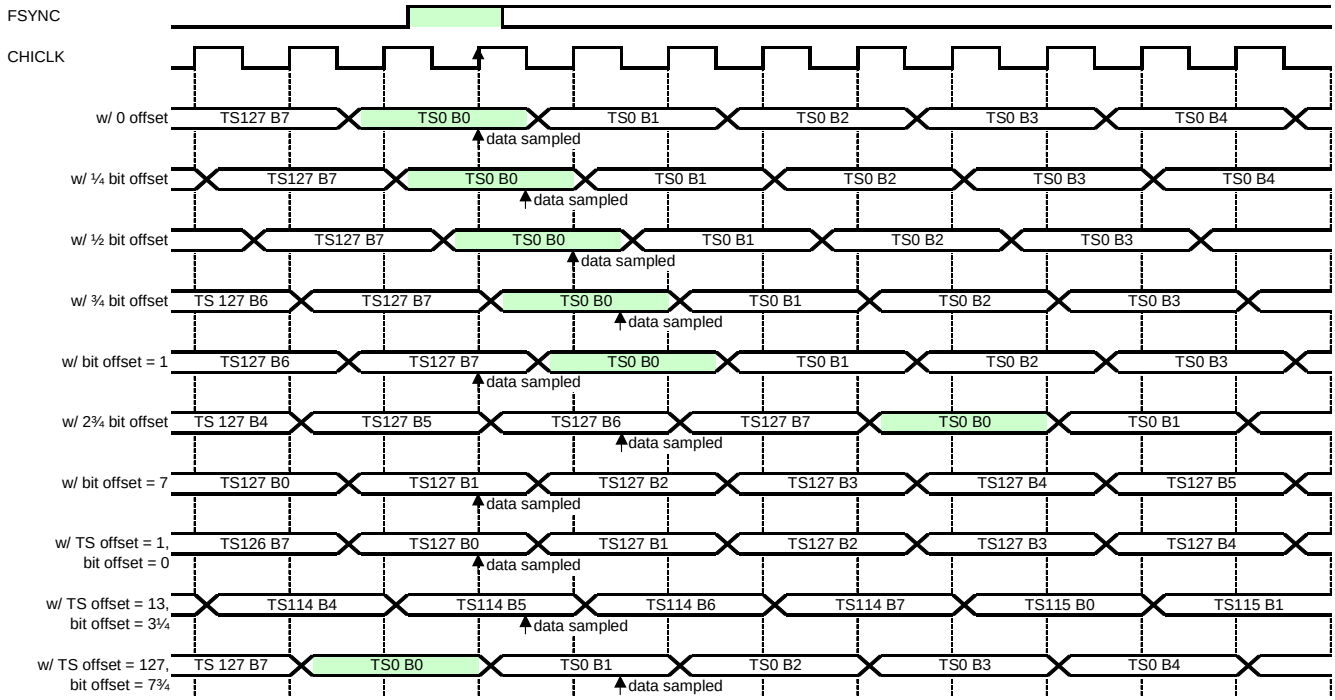


Notes:
1/4 bit offset not valid with 16 Mbits/s data.

For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

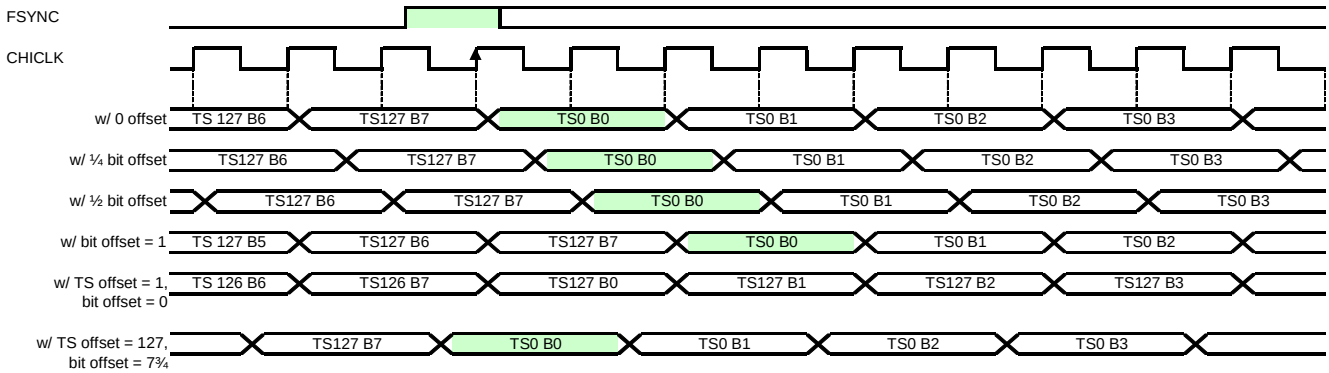
Figure 8. Transmit CHI Timing with 16.384 Mbits/s Data and 16.384 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

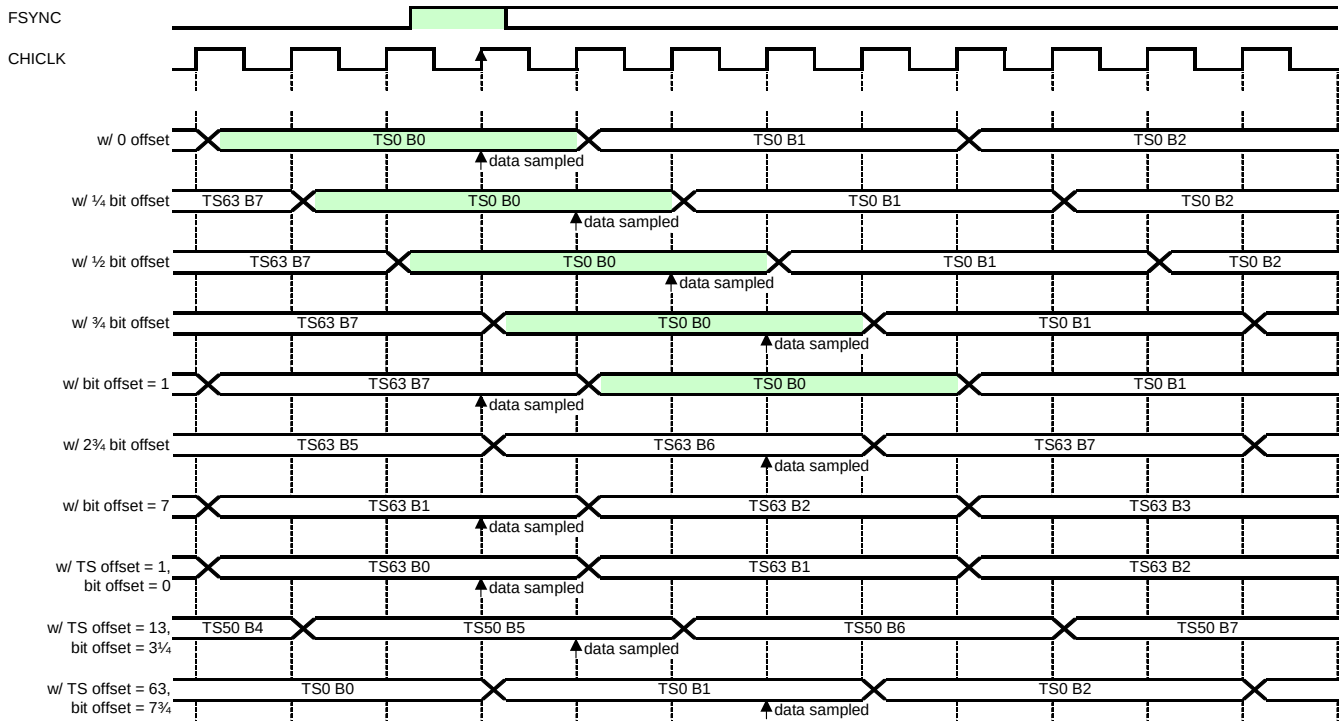
Figure 9. Typical Receive CHI Timing with 8.192 Mbits/s Data and 16.384 MHz CHICLK



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

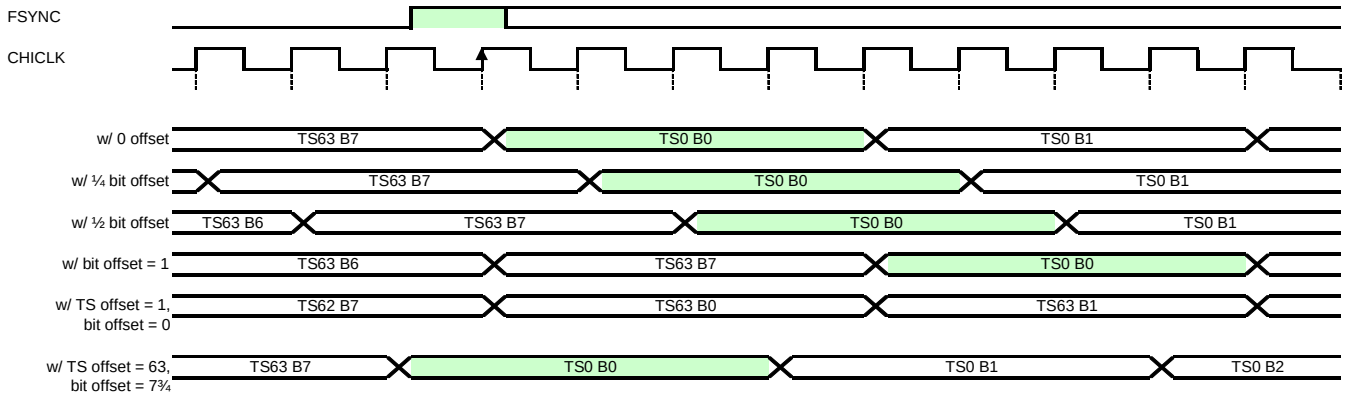
Figure 10. Transmit CHI Timing with 8.192 Mbits/s Data and 16.384 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

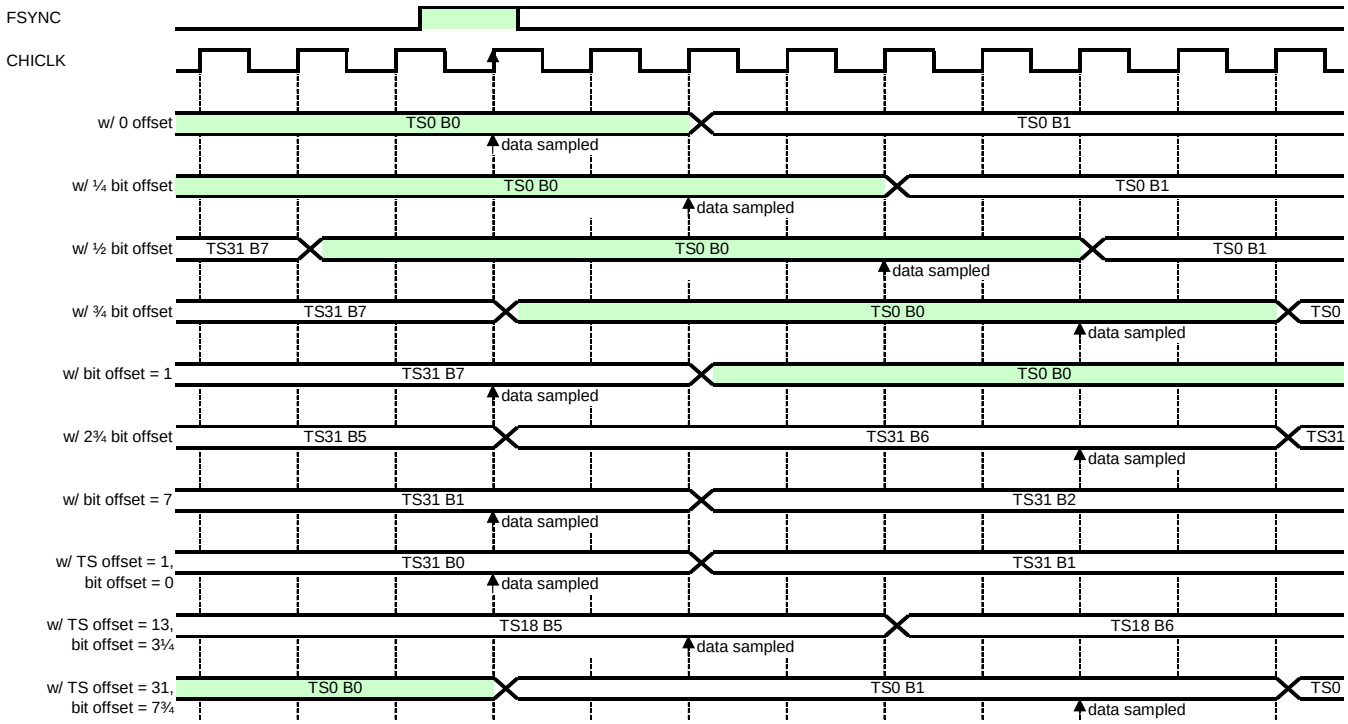
Figure 11. Typical Receive CHI Timing with 4.096 Mbits/s Data and 16.384 MHz CHICLK



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

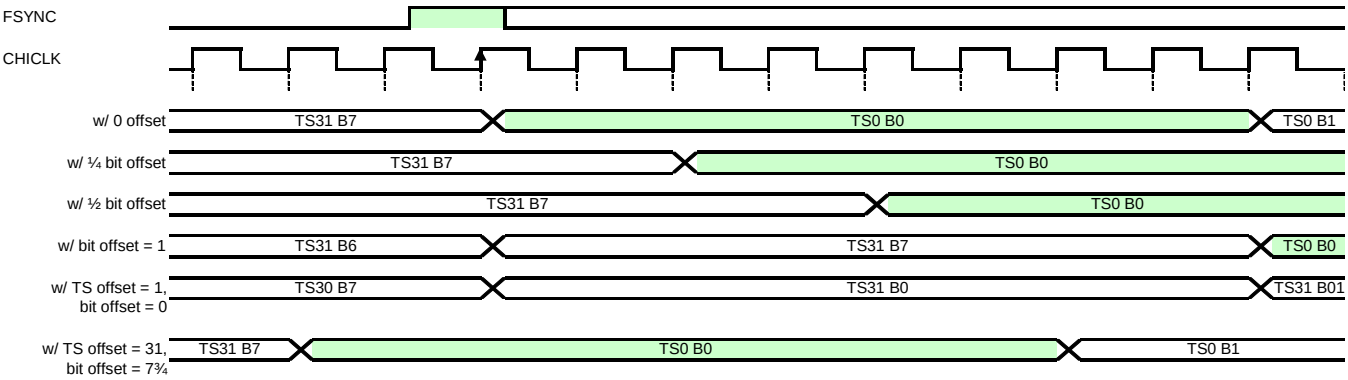
Figure 12. Transmit CHI Timing with 4.096 Mbits/s Data and 16.384 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

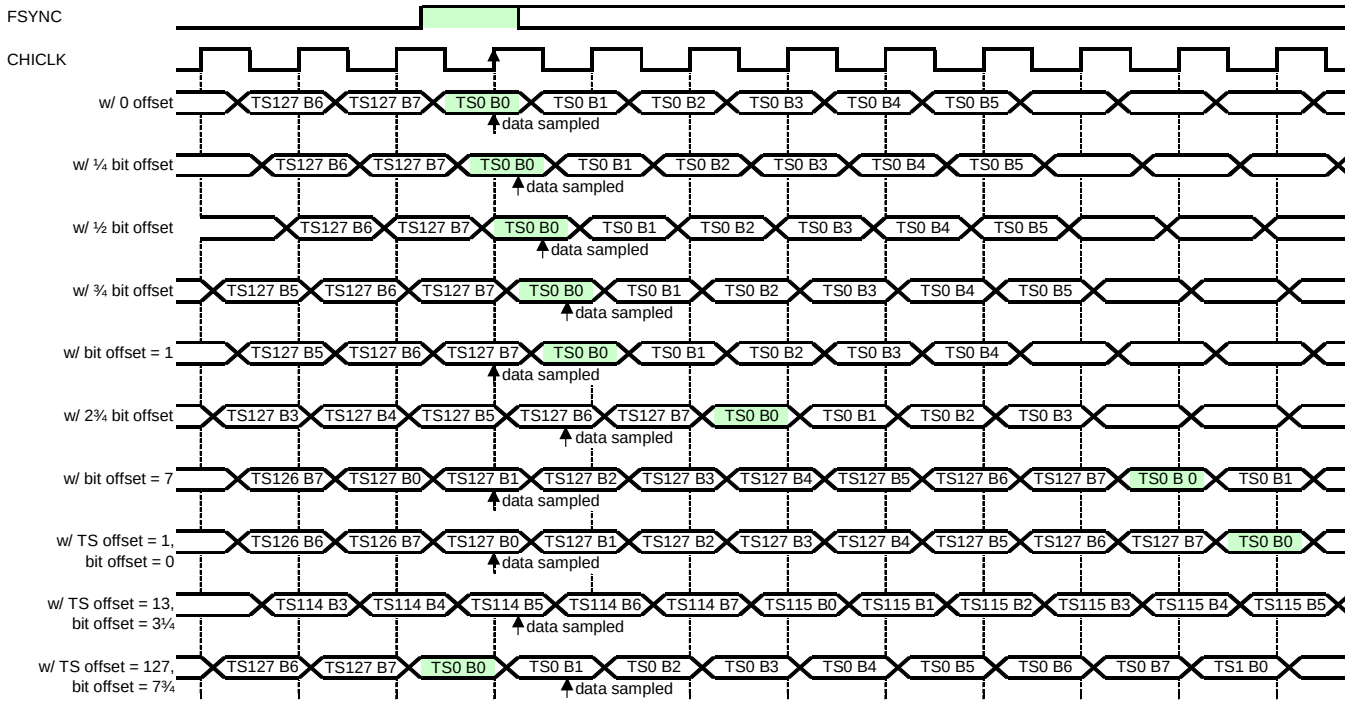
Figure 13. Typical Receive CHI Timing with 2.048 Mbits/s Data and 16.384 MHz CHICLK



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

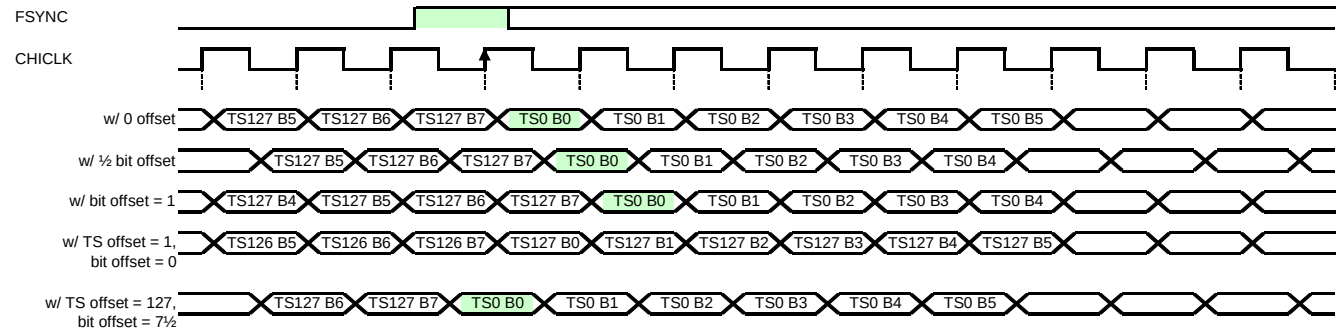
Figure 14. Transmit CHI Timing with 2.048 Mbits/s Data and 16.384 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)



Note: For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

Figure 15. Typical Receive CHI Timing with 8.192 Mbits/s Data and 8.192 MHz CHICLK



Notes:
1/4 bit offset not valid with 8 MHz data and 8 MHz clock.

For this timing diagram, it is assumed that FSYNC has been programmed to be active-high, and to be sampled by the rising edge of the CHICLK.

Figure 16. Transmit CHI Timing with 8.192 Mbits/s Data and 8.192 MHz CHICLK

Timing Diagrams and ac Characteristics (continued)

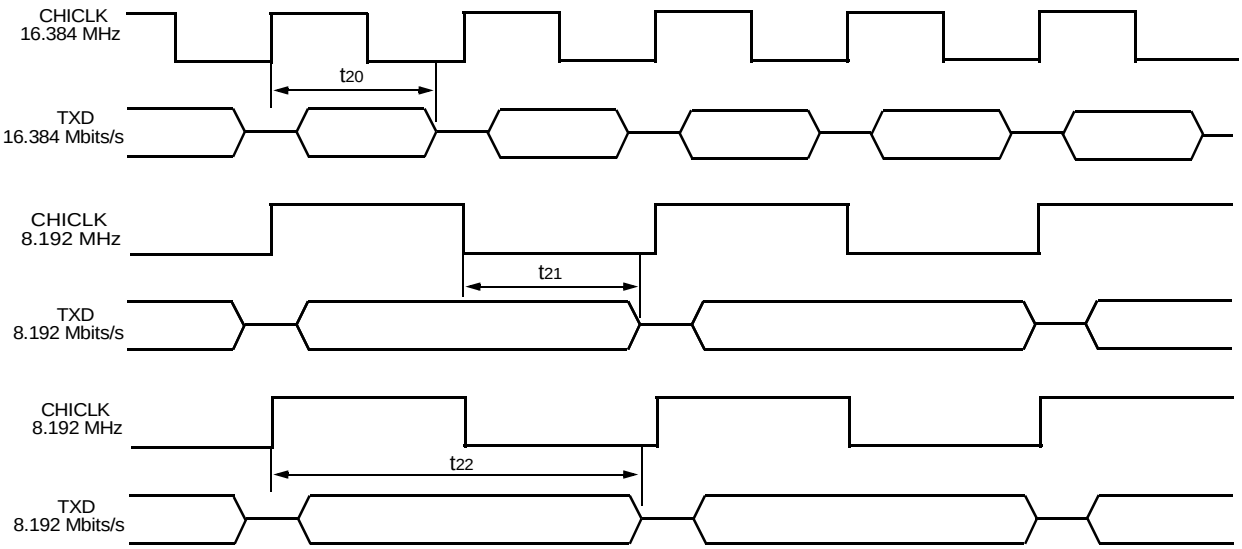


Figure 17. CHI 3-state Output Control

Table 22. CHI 3-state Output Control

Control in the table below refers to bits [6:4] in Transmit_CHI_Global_Configuration register (0x0C84). This only applies if bits 13 and 12 of the corresponding Transmit_CHI_Control register (0x0C00—0x0C7E) are set to 11. See TSI-16 Register Description.

Parameter	Control	Reference Point*	Min†	Max*	Unit
t20	000	After Previous Like Edge in 16 MHz	50	59	ns
	001	After Previous Like Edge in 16 MHz	44	53	ns
	010	After Previous Like Edge in 16 MHz	38	47	ns
	011	After Previous Like Edge in 16 MHz	32	41	ns
t21	000	After Previous Opposite Edge in 8 MHz	50	59	ns
	001	After Previous Opposite Edge in 8 MHz	44	53	ns
	010	After Previous Opposite Edge in 8 MHz	38	47	ns
	011	After Previous Opposite Edge in 8 MHz	32	41	ns
t22	100	After Previous Like Edge (8 MHz mode only)	111	120	ns
	101	After Previous Like Edge (8 MHz mode only)	105	114	ns
	110	After Previous Like Edge (8 MHz mode only)	99	108	ns
	111	After Previous Like Edge (8 MHz mode only)	93	102	ns

* Like edge is the reference edge (rising or falling) as defined by the Transmit_Clock_Edge bit in the Transmit_CHI_Global_Configuration (0x0C84) register. See TSI-16 Register Description document for further details.
† All timing specifications are with respect to the parameters shown in Figure 5.

Timing Diagrams and ac Characteristics (continued)

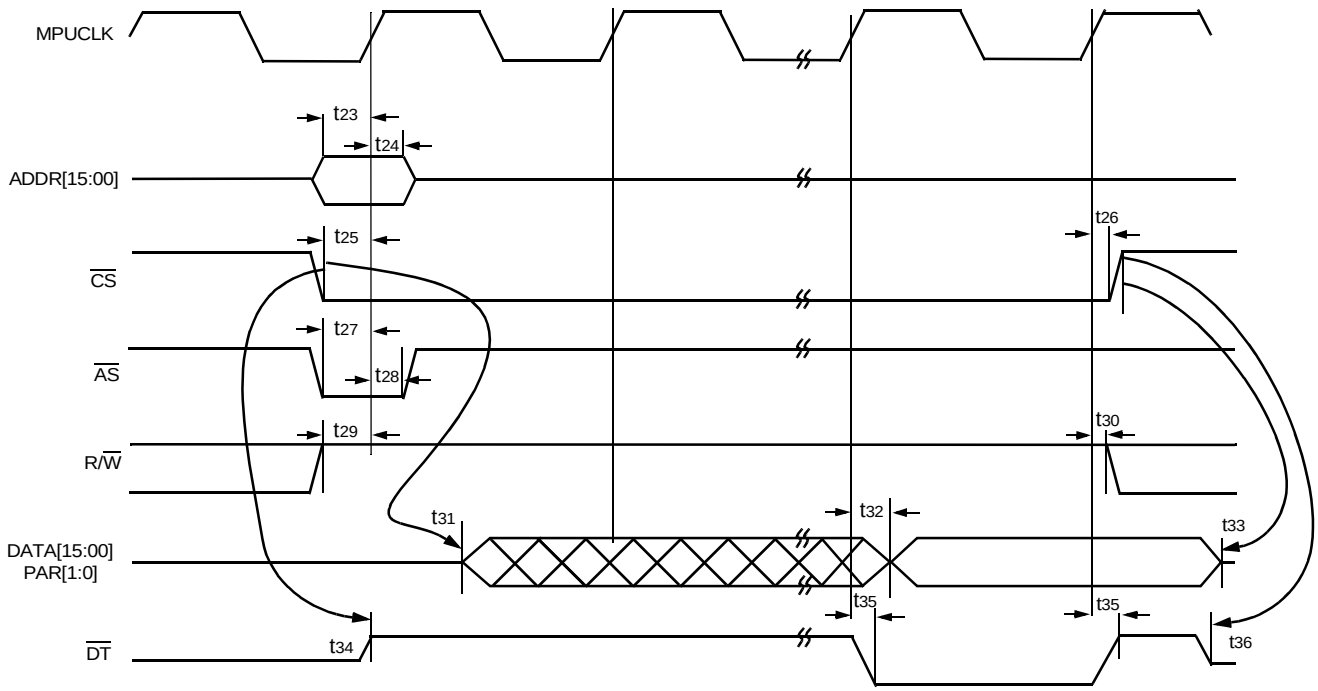


Figure 18. Microprocessor Port Timing—Read Cycle

Table 23. Microprocessor Port Timing—Read Cycle

Parameter	Description	Min*	Max*	Unit
t23	Address Setup	5	—	ns
t24	Address Hold	1	—	ns
t25	Chip Select Setup	5	—	ns
t26	Chip Select Hold	1	—	ns
t27	Address Strobe Setup	5	—	ns
t28	Address Strobe Hold	1	—	ns
t29	R/$\overline{W}$ Setup	5	—	ns
t30	R/$\overline{W}$ Hold	1	—	ns
t31	Data Output Enable	—	15	ns
t32	Data Clock to Valid	1	7	ns
t33	Data High Impedance	—	8	ns
t34	$\overline{DT}$ High Impedance to Valid	1	15	ns
t35	$\overline{DT}$ Clock to Out	1	7	ns
t36	$\overline{DT}$ Valid to High Impedance	1	8	ns

* All timing specifications are with respect to the parameters shown in Figure 5.

Timing Diagrams and ac Characteristics (continued)

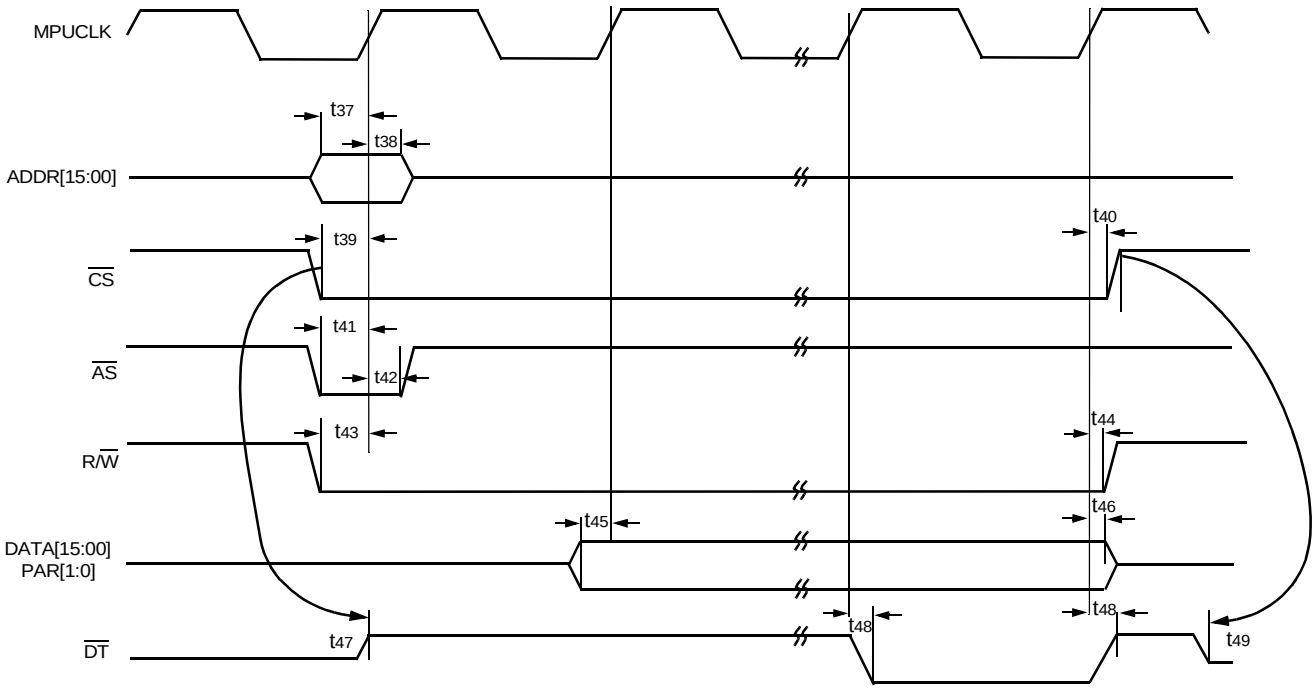


Figure 19. Microprocessor Port Timing—Write Cycle

Table 24. Microprocessor Port Timing—Write Cycle

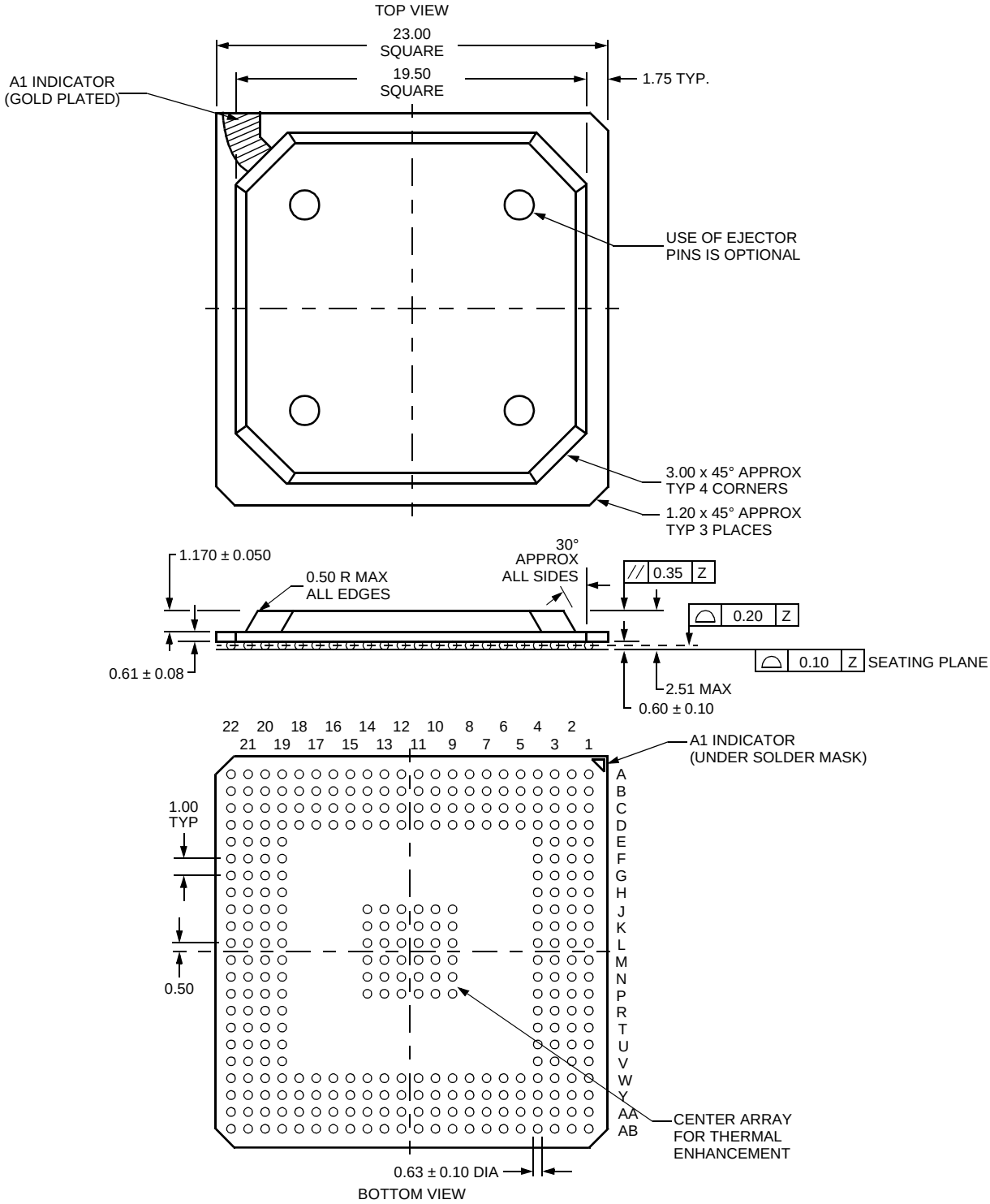
Parameter	Description	Min*	Max*	Unit
t37	Address setup	5	—	ns
t38	Address Hold	1	—	ns
t39	Chip Select Setup	5	—	ns
t40	Chip Select Hold	1	—	ns
t41	Address Strobe Setup	5	—	ns
t42	Address Strobe Hold	1	—	ns
t43	R/$\overline{W}$ Setup	5	—	ns
t44	R/$\overline{W}$ Hold	1	—	ns
t45	Data Setup	5	—	ns
t46	Data Hold	1	—	ns
t47	$\overline{DT}$ High Impedance to Valid	1	15	ns
t48	$\overline{DT}$ Clock to Out	1	7	ns
t49	$\overline{DT}$ Valid to High Impedance	1	8	ns

* All timing specifications are with respect to the parameters shown in Figure 5.

Note: Posted writes follow the same timing shown in Figure 19 and Table 24. A posted write may return a $\overline{DT}$ prior to the device completing the write cycle. This allows the microprocessor to continue operation while the TSI-16 completes the write.

Outline Diagrams

Dimensions are in millimeters.



2649(F)

Ordering Information

Device	Part Number	Ball Count	Package	Comcode
TSI-16	TTSI016641BL-1	324	PBGAM1	700007322

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