Not Recommended For New Design

LX1686

Digital Dimming CCFL Controller IC

PRODUCTION DATA SHEET

DESCRIPTION

The LX1686 Backlight Controller IC provides all the control functions needed to implement Microsemi's direct drive inverters used to operate cold cathode fluorescent lamps (CCFL's). This IC can be used to control single or multiple-lamp configurations. CCFL's are used for back or edge lighting of liquid crystal flat panel displays (LCD's) and typically find application in notebook computers, web browsers, automotive and industrial instrumentation, and entertainment systems.

The LX1686 includes a PWM controlled lamp current burst circuit that can provide a > 100:1 dimming range from a simple zero to 2.5V potentiometer input. The PWM dimming burst rate is easily synchronized to the LCD panel's frame rate to prevent interference from optical beat frequencies.

Safety and reliability features include a new dual feedback control loop that permits regulation of maximum lamp strike voltage as well as lamp current. Regulating maximum lamp voltage permits the designer to provide for ample worst case lamp strike voltage while at the same time conservatively limit maximum open circuit voltage.

An innovative new strike voltage generation technique enables the nodule designer to optimize high voltage transformer design for maximum operating efficiency with no power dissipating overhead to guarantee strike capability

Direct drive topology is a non-resonant, oscillator-controlled PWM regulation method. The LX1686 allows a wide choice of fixed operating frequencies to match lamp current frequency to the lamp's most efficient operating point, and to minimize high frequency interference.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website:
Protected by U.S. Patents 5,615,093; 5,923,129; 5,930,121; 6,198,234; Patents Pending

KEY FEATURES

- RangeMAX™ Wide Range Dimming (>100:1)
- Synchronizable to Display Video Frequency
- High Voltage Feedback Loop Directly Controls Maximum Open Lamp
- Micro-Amp Sleep Mode
- User Programmable Fixed Frequency Operation
- Under-Voltage Lockout Feature With Power-Up Reset
- Built-In Soft-Start Feature
- Operates With 3.3V or 5V power Supplies
- 100mA Output Drive Capability

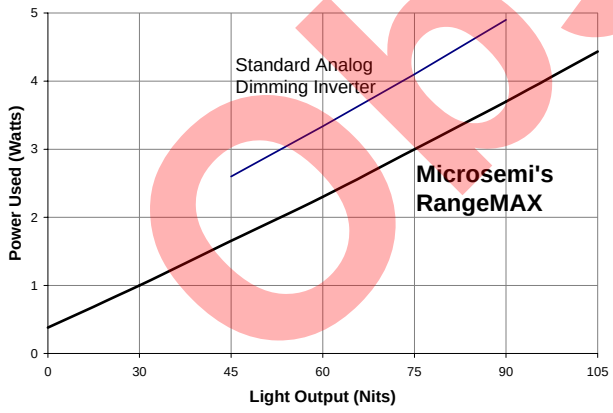
APPLICATIONS

- Notebooks
- Instrumentation Display
- Desktop Computer Monitors
- Low Ambient Light Displays (used in Aircraft, Automobiles, and Hand-Held Equipment)

BENEFITS

- Extremely High Efficiency From 3.3V to 5V Power Supplies
- Lower Cost Than Conventional Buck / Royer Inverter Topologies
- Improved Lamp Strike Capability
- Improved Over-Voltage Control

PRODUCT HIGHLIGHT



Light emitted by a CCFL is proportional to the current flowing through it. There are two ways to control the current: by adjusting the amplitude of a continuous AC current; or, as with RangeMAX technology, by varying the amount of time a burst of full current is present. RangeMAX technology frees the backlight inverter module designer to operate in a lower brightness and lower power consumption mode than is possible with conventional amplitude control methods.

PACKAGE ORDER INFO

T_A (°C)	PW Plastic TSSOP 24-PIN RoHS Complaint / Pb-free Transition D/C: 0442
0 to 85	**LX1686CPW**
-40 to 85	**LX1686IPW**

Note: Available in Tape & Reel.
Append the letters "TR" to the part number. (i.e. LX1686CPW-TR)

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INTEGRATED PRODUCTS

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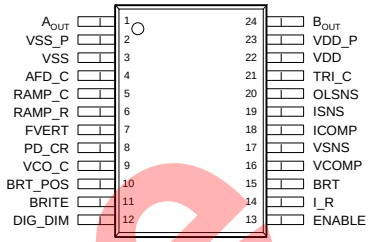
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD, VDD_P) 6.5V
Digital Inputs ..... -0.3 to VDD +0.5V
Analog Inputs ..... -0.3 to VDD +0.5V
Digital Outputs ..... -0.3 to VDD +0.5V
Analog Outputs ..... -0.3 to VDD +0.5V
Operating Junction Temperature ..... 150°C
Storage Temperature ..... -65°C to 150°C
RoHS / Pb-free Peak Package Solder Reflow Temperature
(40 second maximum exposure) ..... 260°C (+0,-5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal

PACKAGE PIN OUT



PW PACKAGE
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

THERMAL DATA

PW PACKAGE

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	100°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

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FUNCTIONAL PIN DESCRIPTION

PIN NAME	DESCRIPTION
AOUT	Output driver A.
VSS_P	Power ground for output drivers only.
VSS	Signal ground.
AFD_C	Connects to an external capacitor, C_{AFD}. Forcing to ground or VDD will make the VCO oscillate at approximately 50% of the maximum VCO frequency. Forcing to VDD/2 will make the VCO oscillate at 2x the FVERT frequency.
RAMP_C	Connects to external capacitor C_{RAMP} for setting Direct Drive PWM operating frequency.
RAMP_R	Connects to external resistor R_{RAMP} for setting Direct Drive PWM operating frequency.
FVERT	Vertical frequency reference digital input. Has internal pull down.
PD_CR	Phase Detector Filter. Part of phase lock loop. Connects to external capacitor and resistor network.
VCO_C	Connects to external capacitor C_{VCO}
BRT_POS	Brightness control polarity. Has internal pull up. Leave open or pull up to VDD for dimming brightness proportional to BRITE voltage, connect to ground for brightness inversely proportional to BRITE voltage.
BRITE	Analog voltage input for brightness control.
DIG_DIM	Digital Dimming Enable internal pull up. Leave open or pull up to VDD for operating in digital dimming mode. Connect to ground for analog dimming mode.
ENABLE	Chip Enable internal pull up. High enables the chip. Low disables.
I_R	Current Reference Resistor. External resistor to ground (Ri) determines internal capacitor C_{ICOMP}.
BRT	Current Error Amplifier non-inverting input
VCOMP	Voltage Error Amplifier output. Connects to external frequency compensation capacitor C_{VCOMP}. Controls soft-start timing.
VSNS	Voltage Error Amplifier inverting input.
ICOMP	Current Error Amplifier output. Connects to external frequency compensation capacitor C_{ICOMP}.
ISNS	Current Error Amplifier inverting Input.
OLSNS	Open Lamp Sense Input.
TRI_C	Connects to external capacitor C_{TRI} for setting strike Frequency ramp slope.
VDD	VDD
VDD_P	Dedicated VDD for output buffers only.
BOUT	Output Driver B.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature -0°C ≤ T_A ≤ 85°C for the LX1686*C*PW and -40°C ≤ T_A ≤ 85°C for the LX1686IPW except where otherwise noted. Test conditions: VDD = VDD_P = 3.0 to 5.5V, Ri = 40kΩ, C_{VCO} = 0.01µF, C_{AFD} = 0.22µF, C_{TRI} = 0.83µF, C_{RAMP} = 208pF, R_{RAMP} = 15kΩ, C_{PD} = 0.22µF, C_{PDB} = 0.047µF, R_{PD} = 110kΩ

Parameter	Symbol	Test Conditions	LX1686			Units
			Min	Typ	Max	
Power Supply Voltage	VDD	VDD = VDD_P	3		5.5	V
Operating Current	I_{DD}	VDD = VDD_P = 5V		5	7	mA
Power Supply Voltage	VDD_P	VDD = VDD_P	3		5.5	V
Output Buffer Operating Current	I_{DD_P}	Volsns = VDD = VDD_P = 5V, CA = CB = 1000pF		2	10	mA
UVLO Threshold	V_{TH_UVLO}		2.7		2.9	V
UVLO Hysteresis	V_{H_UVLO}			160		mV
DIRECT DRIVE RAMP BLOCK						
Triangular Wave Generator Analog Output Peak Voltage	V_{P_TRI}			2.25		V
Triangular Wave Generator Analog Output Valley Voltage	V_{V_TRI}			0.75		V
Triangular Wave Generator Oscillation Frequency	$F_{\_TRI}$			10		Hz
Triangular Wave Generator Oscillation Charge Current	I_{CHG_TRI}	Tri_c = 0V	-2.3	-2.55	-2.9	µA
Triangular Wave Generator Oscillation Discharge Current	I_{DISCHG_TRI}	Tri_c = 3V	2.3	2.65	2.9	µA
Ramp Generator Analog Output Peak Voltage	V_{P_RAMP}			2.25		V
Ramp Generator Analog Output Valley Voltage	V_{V_RAMP}			0.75		V
Ramp Frequency Change Threshold	$V_{TH\_RAMP\_R}$	VDD = 3V	1.35	1.5	1.65	V
		VDD = 5.5V	1.55	1.65	1.85	V
Ramp Generator Oscillation Frequency – Nominal	F_{RAMP}	V_{TRI_C} = 1.4V	84	100	116	KHz
Ramp Generator Oscillation Frequency – Maximum	F_{RAMP_HI}	V_{TRI_C} = 2.25V	170	200	256	KHz
OLSNS Threshold Voltage	V_{TH_OLSNS}	VDD = 3V	200	300	400	mV
OLSNS Hysteresis	V_{H_OLSNS}	VDD = 3V		45		mV
OLSNS-to-ICOMP Propagation Delay	T_{D_OLSNS}	GBD		1		µS
DIGITAL DIMMER BLOCK						
FVERT Input Frequency Capture Range	F_{R_FVERT}		45		200	Hz
FVERT Logic Threshold	V_{TH_FVERT}	Design Reference Only		VDD/2		V
FVERT Input Resistance	R_{FVERT}	Design Reference Only		50		kΩ
VCO Analog Output Peak Voltage	V_{P_VCO}			2.5		V
VCO Analog Output Valley Voltage	V_{V_VCO}			0.65		V
VCO Forced Source Current	$F_{R\_VCO\_I\_SRC}$	VPD_CR = 3V, VDD = 3V	-6.4	-5.8	-5.2	µA
Forced VCO Oscillation Frequency	F_{X_VCO}	AFC_C = 0V, CVCO = 0.01µF		250		Hz
Auto-Frequency Detection Response	T_{D_AFD}	FVERT Frequency is 200Hz, VDD = 3V		1000		ms
BRITE Voltage Range	V_{R_BRITE}		0		VDD	V
Full-Brightness Brite Input Voltage	V_{BRITE_FULL}	V_{BRT_POS} = VDD or float; BRITE = 2.5V	2.35	2.5	2.65	V
		VBRT_POS = 0V, BRITE = 0.5V	2.35	2.5	2.65	V
Full-Darkness Brite Input Voltage	V_{BRITE_DARK}	VBRT_POS = VDD or float, BRITE = 0.5V	0.35	0.5	0.65	V
		VBRT_POS = 0V, BRITE = 2.5V	0.35	0.5	0.65	V

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Parameter	Symbol	Test Conditions	LX1686 Min	LX1686 Typ	LX1686 Max	Units
DIGITAL DIMMING BLOCK (CONTINUED)						
BRITE-to-ICOMP Propagation Delay	T_{D_BRITE}			300		ns
BRITE_POS Logic Threshold				VDD/2		V
DIG-DIM Logic Threshold				VDD/2		V
DIRECT DRIVE PWM BLOCK						
ISNS Threshold Voltage Range	V_{R_ISNS}	DIG_DIM = VDD	0		2.5	V
VAMP Transconductance	G_{M_VAMP}	VCOMP = 1.25V		400		µmho
VAMP Output Source Current	I_{S_VAMP}	VCOMP = 1.5V	10	50	110	µA
VAMP Output Sink Current	I_{SK_VAMP}	VCOMP = 1.5V	15	70	120	µA
VAMP Output Voltage Range	V_{R_VAMP}		0		VDD	V
VSNS Threshold Voltage	V_{TH_VSNS}	VCOMP = VSNS	1.12	1.25	1.38	V
VCOMP Discharge Current	I_{D_VCOMP}	VCOMP = 0.5V, VDD = 3V	0.8	1.5	10	mA
IAMP Transconductance	G_{M_IAMP}	BRITE = 0.5 – 2.6V	70	200	700	µmho
IAMP Output Source Current	I_{S_IAMP}	ICOMP = 1.5V, VDD = 3V	-15	-40	-80	µA
IAMP Output Sink Current	I_{SK_IAMP}	ICOMP = 1.5V, VDD = 3V	20	60	100	µA
IAMP Output Voltage Range	V_{R_IAMP}		0		VDD	V
VCMP Input Offset Voltage	V_{OS_VCMP}	VCOMP = 1.25V, VDD = 3V	-10	3	10	mV
VCOMP-to-Output Propagation Delay	T_{D_VCOMP}	VDD = 3V		250	500	ns
ICMP Input Offset Voltage	V_{OS_ICMP}	ICOMP = 0.5 to 2.25V, VDD = 3V	-10	3	10	mV
ICOMP-to-Output Propagation Delay	T_{D_ICOMP}	BRITE = 1.25V, RAMP_C = 2V, VDD = 3V		1100		ns
OUTPUT BUFFER BLOCK						
Output Sink Current	I_{SK_OUTBUF}	AOUT, BOUT = VDD = 3V	25	45	85	mA
		AOUT, BOUT = 1V, VDD = 3V	20	35	85	mA
Output Source Current	I_{SOUT_BUF}	AOUT, BOUT = 0V, VDD = 3V	-35	-50	85	mA
		AOUT, BOUT = 2V, VDD = 3V	-20	-40	85	mA
BIAS CONTROL BLOCK						
Voltage at Pin I_R	V_{IR}		.975		1.02	V
Pin I_R Maximum Source Current	I_{MAX_IR}	Design Reference Only		50		µA
VBG Output Resistance	R_{O_VBG}	Design Reference Only		10		kΩ
ENABLE Logic Threshold – 3V	V_{EN3V}	VDD = 3V	1.5	1.9	2.4	V
ENABLE Logic Threshold – 5.5V	$V_{EN5.5}$	VDD = 5.5V	2.7	3.2	3.6	V
ENABLE Threshold Hysteresis – 3V	V_{H_EN3}			450		mV
ENABLE Threshold Hysteresis – 5.5V	$V_{H\_EN5.5}$			350		mV

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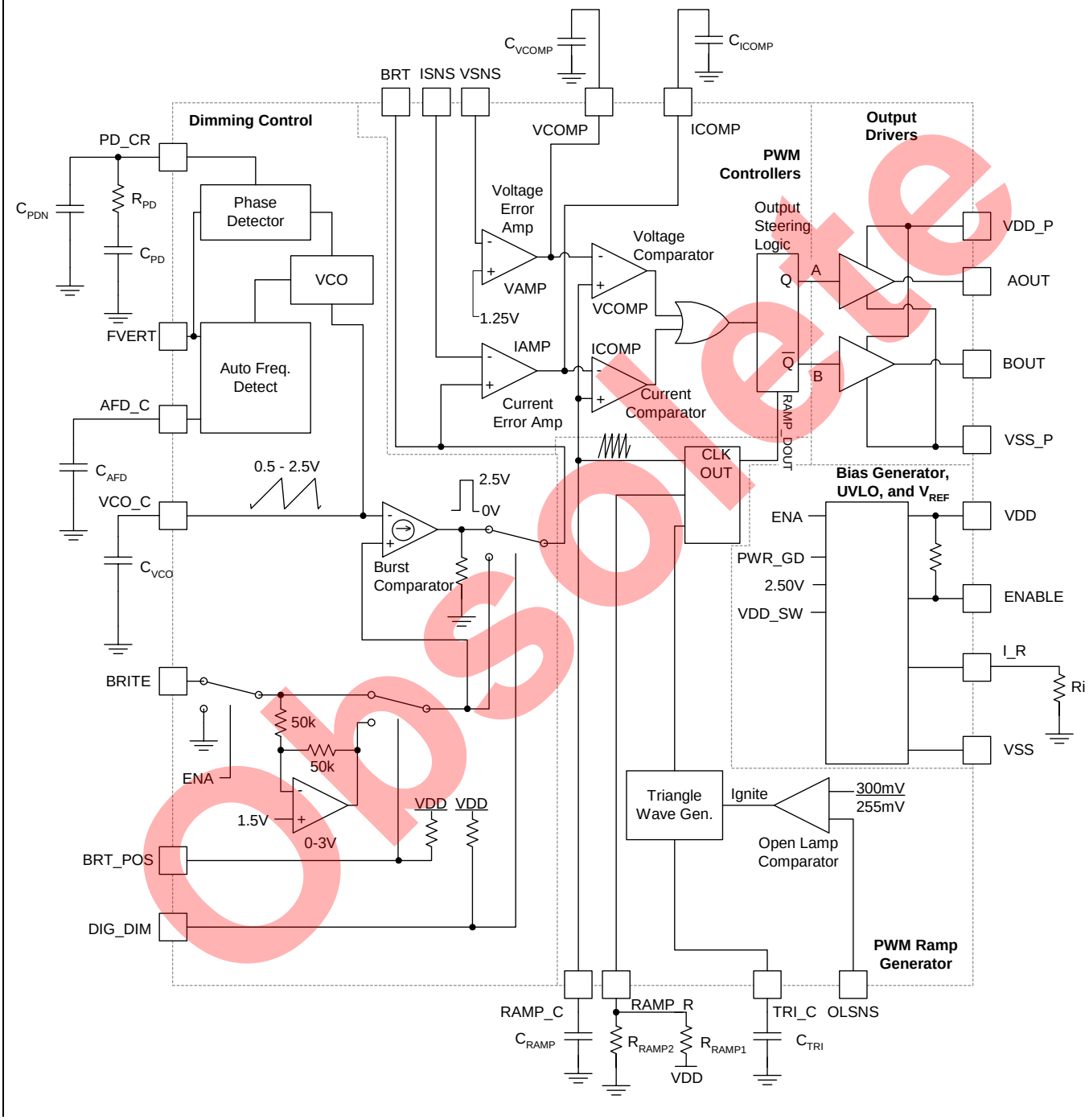
BLOCK DIAGRAM



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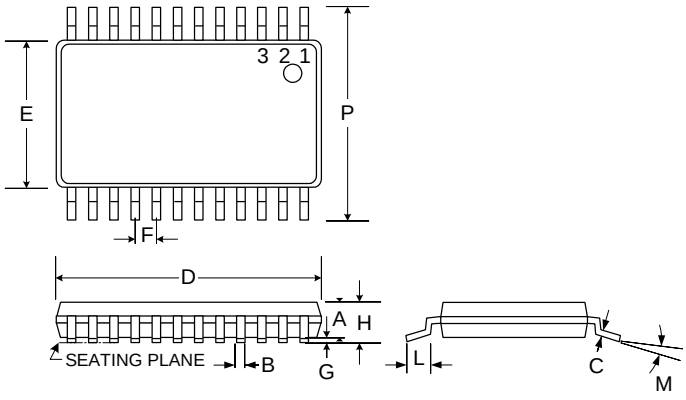
PACKAGE DIMENSIONS

PW 24-Pin Thin Small Shrink Outline (TSSOP)



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	0.95	0.033	0.037
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	7.70	7.90	0.303	0.311
E	4.30	4.50	0.169	0.177
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	–	1.10	–	.0433
L	0.50	0.75	0.020	0.030
M	0°	8°	0°	8°
P	6.25	6.50	0.246	0.256
*LC	–	0.10	–	0.004

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

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NOTES