

**16 M-BIT DYNAMIC RAM  
4 M-WORD BY 4-BIT, FAST PAGE MODE**

**Description**

The  $\mu$ PD42S16400, 4216400, 42S17400, 4217400 are 4,194,304 words by 4 bits CMOS dynamic RAMs. The fast page mode capability realize high speed access and low power consumption.

These differ in refresh cycle and the  $\mu$ PD42S16400, 42S17400 can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh.

These are packaged in 26-pin plastic TSOP(II) and 26-pin plastic SOJ.

**Features**

- 4,194,304 words by 4 bits organization
- Single +5.0 V  $\pm$  10 % power supply
- Fast page mode
- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
$\mu$ PD42S16400-50, 4216400-50	550 mW	50 ns	90 ns	35 ns
$\mu$ PD42S17400-50, 4217400-50	660 mW			
$\mu$ PD42S16400-60, 4216400-60	495 mW	60 ns	110 ns	40 ns
$\mu$ PD42S17400-60, 4217400-60	605 mW			
$\mu$ PD42S16400-70, 4216400-70	440 mW	70 ns	130 ns	45 ns
$\mu$ PD42S17400-70, 4217400-70	550 mW			
$\mu$ PD42S16400-80, 4216400-80	385 mW	80 ns	150 ns	50 ns
$\mu$ PD42S17400-80, 4217400-80	495 mW			

- The  $\mu$ PD42S16400, 42S17400 can execute  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh.

Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
$\mu$ PD42S16400	4,096 cycles/128 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	1.4 mW (CMOS level input)
$\mu$ PD42S17400	2,048 cycles/128 ms		
$\mu$ PD4216400	4,096 cycles/64 ms	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh	5.5 mW (CMOS level input)
$\mu$ PD4217400	2,048 cycles/32 ms		

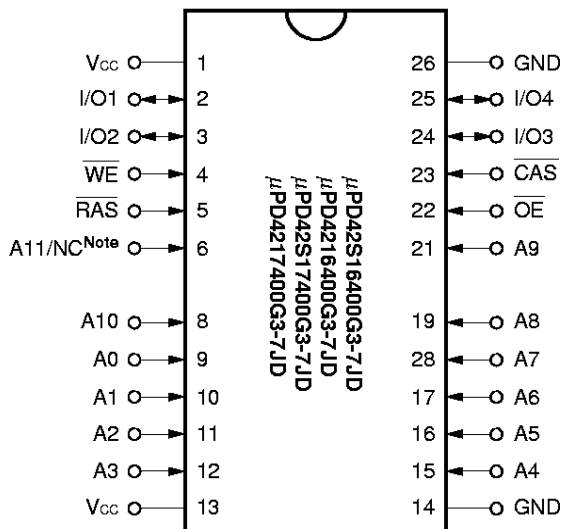
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Ordering Information

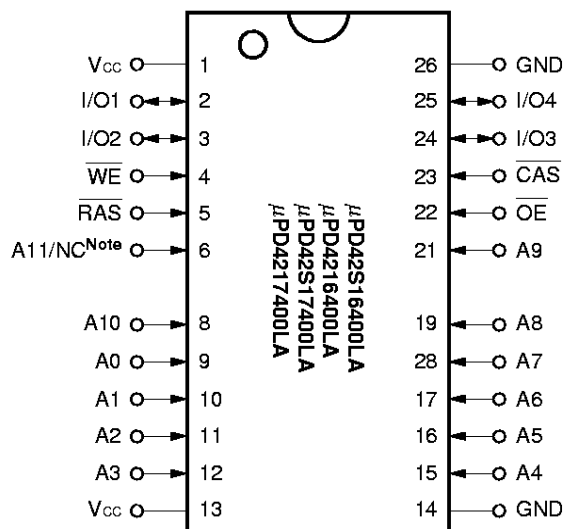
Part number	Access time (MAX.)	Package	Refresh
μPD42S16400G3-50-7JD	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD42S17400G3-50-7JD			
μPD42S16400G3-60-7JD	60 ns		
μPD42S17400G3-60-7JD			
μPD42S16400G3-70-7JD	70 ns		
μPD42S17400G3-70-7JD			
μPD42S16400G3-80-7JD	80 ns		
μPD42S17400G3-80-7JD			
μPD42S16400LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μPD42S17400LA-50			
μPD42S16400LA-60	60 ns		
μPD42S17400LA-60			
μPD42S16400LA-70	70 ns		
μPD42S17400LA-70			
μPD42S16400LA-80	80 ns		
μPD42S17400LA-80			
μPD4216400G3-50-7JD	50 ns	26-pin plastic TSOP (II) (300 mil)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh
μPD4217400G3-50-7JD			
μPD4216400G3-60-7JD	60 ns		
μPD4217400G3-60-7JD			
μPD4216400G3-70-7JD	70 ns		
μPD4217400G3-70-7JD			
μPD4216400G3-80-7JD	80 ns		
μPD4217400G3-80-7JD			
μPD4216400LA-50	50 ns	26-pin plastic SOJ (300 mil)	
μPD4217400LA-50			
μPD4216400LA-60	60 ns		
μPD4217400LA-60			
μPD4216400LA-70	70 ns		
μPD4217400LA-70			
μPD4216400LA-80	80 ns		
μPD4217400LA-80			

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)



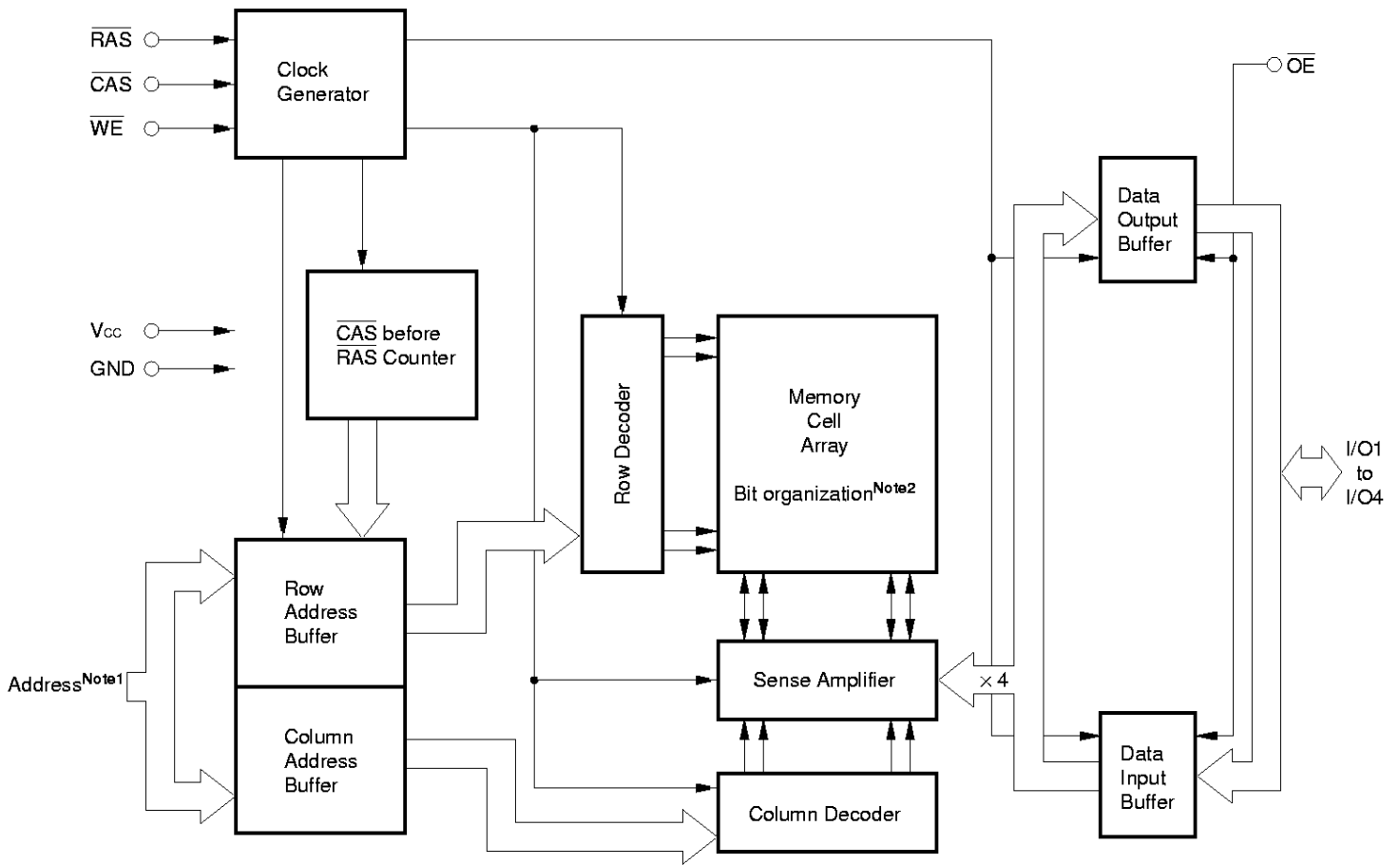
26-pin Plastic SOJ (300 mil)



**Note** A11 ... μPD42S16400, 4216400  
 NC .... μPD42S17400, 4217400

- A0 to A11 : Address Inputs
- I/O1 to I/O4: Data Inputs/Outputs
- $\overline{RAS}$  : Row Address Strobe
- $\overline{CAS}$  : Column Address Strobe
- $\overline{WE}$  : Write Enable
- $\overline{OE}$  : Output Enable
- V<sub>cc</sub> : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Notes 1.

Part number	Row address	Column address
μPD42S16400, 4216400	A0 – A11	A0 – A9
μPD42S17400, 4217400	A0 – A10	A0 – A10

2. μPD42S16400, 4216400 ... 4,096 × 1,024 × 4    μPD42S17400, 4217400 ... 2,048 × 2,048 × 4

**Input/Output Pin Functions**

The μPD42S16400, 4216400, 42S17400, 4217400 have input pins  $\overline{RAS}$ ,  $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{OE}$ , Address<sup>Note</sup> and input/output pins I/O1 to I/O4.

Pin name	Input/Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A <sub>x</sub> <sup>Note</sup> (Address inputs)	Input	Address bus. Input total 22-bit of address signal, upper bits and lower bits <sup>Note</sup> in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$ . Then, switch the address bus to column address and activate $\overline{CAS}$ . Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time ( $t_{ASR}$ , $t_{ASC}$ ) and hold time ( $t_{RAH}$ , $t_{CAH}$ ) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$ .
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ .
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$ , $\overline{CAS}$ and $\overline{OE}$ . If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O4 (Data inputs/outputs)	Input/Output	4-bit data bus. I/O1 to I/O4 are used to input/output data.

**Note**

Part number	Address inputs	Upper bits	Lower bits
μPD42S16400, 4216400	A0 – A11	12	10
μPD42S17400, 4217400	A0 – A10	11	11

**Electrical Specifications**

- All voltages are referenced to GND.
- After power up ( $V_{CC} \geq V_{CC(MIN.)}$ ), wait more than 100 μs ( $\overline{RAS}$ ,  $\overline{CAS}$  inactive) and then, execute eight  $\overline{CAS}$  before  $\overline{RAS}$  or  $\overline{RAS}$  only refresh cycles as dummy cycles to initialize internal circuit.

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	$V_T$		-1.0 to +7.0	V
Supply voltage	$V_{CC}$		-1.0 to +7.0	V
Output current	$I_O$		50	mA
Power dissipation	$P_D$		1	W
Operating ambient temperature	$T_A$		0 to +70	°C
Storage temperature	$T_{stg}$		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	$V_{CC}$		4.5	5.0	5.5	V
High level input voltage	$V_{IH}$		2.4		$V_{CC} + 1.0$	V
Low level input voltage	$V_{IL}$		-1.0		+0.8	V
Operating ambient temperature	$T_A$		0		70	°C

**Capacitance ( $T_A = 25\text{ °C}$ ,  $f = 1\text{ MHz}$ )**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_{I1}$	Address			5	pF
	$C_{I2}$	$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$			7	
Data input/output capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended operating conditions unless otherwise noted)

[ $\mu$ PD42S16400, 4216400]

Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		$I_{CC1}$	$\overline{RAS}, \overline{CAS}$ cycling $t_{RC} = t_{RC(MIN.)}$ $I_o = 0$ mA	$t_{RAC} = 50$ ns	100	mA	1, 2, 3
				$t_{RAC} = 60$ ns	90		
				$t_{RAC} = 70$ ns	80		
				$t_{RAC} = 80$ ns	70		
Standby current	$\mu$ PD42S16400	$I_{CC2}$	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN.)}, I_o = 0$ mA $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2$ V, $I_o = 0$ mA $\overline{RAS}, \overline{CAS} \geq V_{IH(MIN.)}, I_o = 0$ mA $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2$ V, $I_o = 0$ mA		2.0	mA	
	$\mu$ PD4216400				0.25		
					2.0		
					1.0		
$\overline{RAS}$ only refresh current		$I_{CC3}$	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}, I_o = 0$ mA	$t_{RAC} = 50$ ns	100	mA	1, 2, 3, 4
				$t_{RAC} = 60$ ns	90		
				$t_{RAC} = 70$ ns	80		
				$t_{RAC} = 80$ ns	70		
Operating current (Fast page mode)		$I_{CC4}$	$\overline{RAS} \leq V_{IL(MAX.)}, \overline{CAS}$ cycling $t_{PC} = t_{PC(MIN.)}, I_o = 0$ mA	$t_{RAC} = 50$ ns	80	mA	1, 2, 5
				$t_{RAC} = 60$ ns	70		
				$t_{RAC} = 70$ ns	60		
				$t_{RAC} = 80$ ns	50		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		$I_{CC5}$	$\overline{RAS}$ cycling $t_{RC} = t_{RC(MIN.)}$ $I_o = 0$ mA	$t_{RAC} = 50$ ns	100	mA	1, 2
				$t_{RAC} = 60$ ns	90		
				$t_{RAC} = 70$ ns	80		
				$t_{RAC} = 80$ ns	70		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (4,096 cycles / 128 ms, only for the $\mu$ PD42S16400)		$I_{CC6}$	$\overline{CAS}$ before $\overline{RAS}$ refresh : $t_{RC} = 31.3$ $\mu$ s $\overline{RAS}, \overline{CAS}$ : $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ $0$ V $\leq V_{IL} \leq 0.2$ V  Standby : $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2$ V Address : $V_{IH}$ or $V_{IL}$ $\overline{WE}, \overline{OE}$ : $V_{IH}$ $I_o = 0$ mA	$t_{RAS} \leq 300$ ns	450	$\mu$ A	1, 2
				$t_{RAS} \leq 1$ $\mu$ s	600	$\mu$ A	1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the $\mu$ PD42S16400)		$I_{CC7}$	$\overline{RAS}, \overline{CAS}$ : $t_{RASS} = 5$ ms $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH(MAX.)}$ $0$ V $\leq V_{IL} \leq 0.2$ V $I_o = 0$ mA		250	$\mu$ A	2
Input leakage current		$I_{I(L)}$	$V_I = 0$ to 5.5 V All other pins not under test = 0 V	-10	+10	$\mu$ A	
Output leakage current		$I_{O(L)}$	$V_O = 0$ to 5.5 V Output is disabled (Hi-Z)	-10	+10	$\mu$ A	
High level output voltage		$V_{OH}$	$I_o = -5.0$ mA	2.4		V	
Low level output voltage		$V_{OL}$	$I_o = +4.2$ mA		0.4	V	

[μPD42S17400, 4217400]

Parameter		Symbol	Test condition	MIN.	MAX.	Unit	Notes
Operating current		I <sub>CC1</sub>	$\overline{RAS}, \overline{CAS}$ cycling $t_{RC} = t_{RC(MIN)}$ $I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$		120	mA 1, 2, 3
				$t_{RAC} = 60 \text{ ns}$		110	
				$t_{RAC} = 70 \text{ ns}$		100	
				$t_{RAC} = 80 \text{ ns}$		90	
Standby current	μPD42S17400	I <sub>CC2</sub>	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN)}, I_o = 0 \text{ mA}$		2.0	mA	
			$\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}, I_o = 0 \text{ mA}$		0.25		
	μPD4217400	$\overline{RAS}, \overline{CAS} \geq V_{IH(MIN)}, I_o = 0 \text{ mA}$		2.0			
		$\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}, I_o = 0 \text{ mA}$		1.0			
$\overline{RAS}$ only refresh current		I <sub>CC3</sub>	$\overline{RAS}$ cycling, $\overline{CAS} \geq V_{IH(MIN)}$ $t_{RC} = t_{RC(MIN)}, I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$		120	mA 1, 2, 3, 4
				$t_{RAC} = 60 \text{ ns}$		110	
				$t_{RAC} = 70 \text{ ns}$		100	
				$t_{RAC} = 80 \text{ ns}$		90	
Operating current (Fast page mode)		I <sub>CC4</sub>	$\overline{RAS} \leq V_{IL(MAX)}, \overline{CAS}$ cycling $t_{PC} = t_{PC(MIN)}, I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$		80	mA 1, 2, 5
				$t_{RAC} = 60 \text{ ns}$		70	
				$t_{RAC} = 70 \text{ ns}$		60	
				$t_{RAC} = 80 \text{ ns}$		50	
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I <sub>CC5</sub>	$\overline{RAS}$ cycling $t_{RC} = t_{RC(MIN)}$ $I_o = 0 \text{ mA}$	$t_{RAC} = 50 \text{ ns}$		120	mA 1, 2
				$t_{RAC} = 60 \text{ ns}$		110	
				$t_{RAC} = 70 \text{ ns}$		100	
				$t_{RAC} = 80 \text{ ns}$		90	
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (2,048 cycles / 128 ms, only for the μPD42S17400)		I <sub>CC6</sub>	$\overline{CAS}$ before $\overline{RAS}$ refresh : $t_{RC} = 62.5 \mu\text{s}$ $\overline{RAS}, \overline{CAS}$ : $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$  Standby : $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Address : $V_{IH}$ or $V_{IL}$ $\overline{WE}, \overline{OE} : V_{IH}$ $I_o = 0 \text{ mA}$	$t_{RAS} \leq 300 \text{ ns}$		400	μA 1, 2
				$t_{RAS} \leq 1 \mu\text{s}$		500	μA 1, 2
$\overline{CAS}$ before $\overline{RAS}$ self refresh current (only for the μPD42S17400)		I <sub>CC7</sub>	$\overline{RAS}, \overline{CAS}$ : $t_{RASS} = 5 \text{ ms}$ $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq V_{IH(MAX)}$ $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$			250	μA 2
Input leakage current		I <sub>I(L)</sub>	$V_i = 0 \text{ to } 5.5 \text{ V}$ All other pins not under test = 0 V	-10	+10	μA	
Output leakage current		I <sub>O(L)</sub>	$V_o = 0 \text{ to } 5.5 \text{ V}$ Output is disabled (Hi-Z)	-10	+10	μA	
High level output voltage		V <sub>OH</sub>	$I_o = -5.0 \text{ mA}$	2.4		V	
Low level output voltage		V <sub>OL</sub>	$I_o = +4.2 \text{ mA}$		0.4	V	

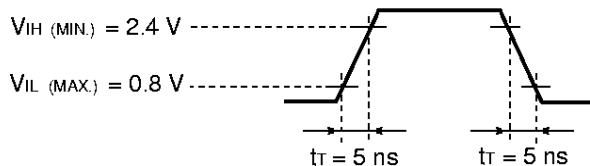
- Notes**
- I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub>, I<sub>CC5</sub> and I<sub>CC6</sub> depend on cycle rates (t<sub>RC</sub> and t<sub>PC</sub>).
  - Specified values are obtained with outputs unloaded.

3.  $I_{CC1}$  and  $I_{CC3}$  are measured assuming that address can be changed once or less during  $\overline{RAS} \leq V_{IL(MAX)}$  and  $\overline{CAS} \geq V_{IH(MIN)}$ .
4.  $I_{CC3}$  is measured assuming that all column address inputs are held at either high or low.
5.  $I_{CC4}$  is measured assuming that all column address inputs are switched only once during each fast page cycle.

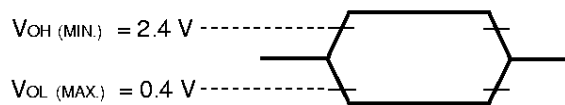
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

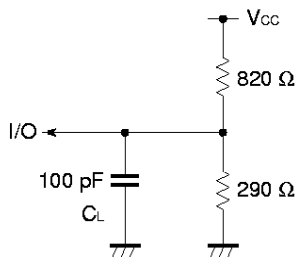
(1) Input timing specification



(2) Output timing specification



★ (3) Output load condition



Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	$t_{RAC} = 50\text{ ns}$		$t_{RAC} = 60\text{ ns}$		$t_{RAC} = 70\text{ ns}$		$t_{RAC} = 80\text{ ns}$		Unit	Notes	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Read / Write cycle time	$t_{RC}$	90	—	110	—	130	—	150	—	ns		
$\overline{RAS}$ precharge time	$t_{RP}$	30	—	40	—	50	—	60	—	ns		
$\overline{CAS}$ precharge time	$t_{CPN}$	8	—	10	—	10	—	10	—	ns		
$\overline{RAS}$ pulse width	$t_{RAS}$	50	10,000	60	10,000	70	10,000	80	10,000	ns	1	
$\overline{CAS}$ pulse width	$t_{CAS}$	13	10,000	15	10,000	18	10,000	20	10,000	ns		
$\overline{RAS}$ hold time	$t_{RSH}$	13	—	15	—	18	—	20	—	ns		
$\overline{CAS}$ hold time	$t_{CSH}$	50	—	60	—	70	—	80	—	ns		
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	18	37	20	45	20	52	25	60	ns	2	
$\overline{RAS}$ to column address delay time	$t_{RAD}$	13	25	15	30	15	35	17	40	ns	2	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	—	5	—	5	—	5	—	ns	3	
Row address setup time	$t_{ASR}$	0	—	0	—	0	—	0	—	ns		
Row address hold time	$t_{RAH}$	8	—	10	—	10	—	12	—	ns		
Column address setup time	$t_{ASC}$	0	—	0	—	0	—	0	—	ns		
Column address hold time	$t_{CAH}$	13	—	15	—	15	—	15	—	ns		
$\overline{OE}$ lead time referenced to $\overline{RAS}$	$t_{OES}$	0	—	0	—	0	—	0	—	ns		
$\overline{CAS}$ to data setup time	$t_{CLZ}$	0	—	0	—	0	—	0	—	ns		
$\overline{OE}$ to data setup time	$t_{OLZ}$	0	—	0	—	0	—	0	—	ns		
$\overline{OE}$ to data delay time	$t_{OED}$	10	—	15	—	15	—	20	—	ns		
Transition time (rise and fall)	$t_r$	3	50	3	50	3	50	3	50	ns		
Refresh time	μPD42S16400, 42S17400	$t_{REF}$	—	128	—	128	—	128	—	128	ms	4
	μPD4216400		—	64	—	64	—	64	—	64		
	μPD4217400		—	32	—	32	—	32	—	32		

- Notes** 1. In  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycles,  $t_{\text{RAS}}(\text{MAX.})$  is 100 μs. ★  
 If  $10 \mu\text{s} < t_{\text{RAS}} < 100 \mu\text{s}$ ,  $\overline{\text{RAS}}$  precharge time for  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  self refresh ( $t_{\text{RPS}}$ ) is applied.
2. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}}(\text{MAX.})$  are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time ( $t_{\text{RAC}}$ ,  $t_{\text{AA}}$  or  $t_{\text{CAC}}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$  will not cause any operation problems.

3.  $t_{\text{CRP}}(\text{MIN.})$  requirement is applied to  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  cycles.
4. This specification is applied only to the μPD42S16400, 42S17400.

**Read Cycle**

Parameter	Symbol	$t_{\text{RAC}} = 50 \text{ ns}$		$t_{\text{RAC}} = 60 \text{ ns}$		$t_{\text{RAC}} = 70 \text{ ns}$		$t_{\text{RAC}} = 80 \text{ ns}$		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	–	50	–	60	–	70	–	80	ns	1
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	–	13	–	15	–	18	–	20	ns	1
Access time from column address	$t_{\text{AA}}$	–	25	–	30	–	35	–	40	ns	1
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	–	13	–	15	–	18	–	20	ns	
Column address lead time referenced to $\overline{\text{RAS}}$	$t_{\text{RAL}}$	25	–	30	–	35	–	40	–	ns	
Read command setup time	$t_{\text{RCS}}$	0	–	0	–	0	–	0	–	ns	
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	0	–	0	–	0	–	0	–	ns	2
Read command hold time referenced to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	–	0	–	0	–	0	–	ns	2
Output buffer turn-off delay time from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	0	10	0	15	0	15	0	20	ns	3
Output buffer turn-off delay time from $\overline{\text{CAS}}$	$t_{\text{OFF}}$	0	10	0	15	0	15	0	20	ns	3

- Notes** 1. For read cycles, access time is defined as follows:

Input conditions	Access time	Access time from $\overline{\text{RAS}}$
$t_{\text{RAD}} \leq t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$	$t_{\text{RAC}}(\text{MAX.})$
$t_{\text{RAD}} > t_{\text{RAD}}(\text{MAX.})$ and $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{MAX.})$	$t_{\text{AA}}(\text{MAX.})$	$t_{\text{RAD}} + t_{\text{AA}}(\text{MAX.})$
$t_{\text{RCD}} > t_{\text{RCD}}(\text{MAX.})$	$t_{\text{CAC}}(\text{MAX.})$	$t_{\text{RCD}} + t_{\text{CAC}}(\text{MAX.})$

$t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}}(\text{MAX.})$  are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time ( $t_{\text{RAC}}$ ,  $t_{\text{AA}}$  or  $t_{\text{CAC}}$ ) is to be used for finding out when output data will be available. Therefore, the input conditions  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{MAX.})$  and  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{MAX.})$  will not cause any operation problems.

2. Either  $t_{\text{RCH}}(\text{MIN.})$  or  $t_{\text{RRH}}(\text{MIN.})$  should be met in read cycles.
3.  $t_{\text{OFF}}(\text{MAX.})$  and  $t_{\text{OEZ}}(\text{MAX.})$  define the time when the output achieves the condition of Hi-Z and is not referenced to  $V_{\text{OH}}$  or  $V_{\text{OL}}$ .

**Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		t <sub>RAC</sub> = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ hold time referenced to $\overline{CAS}$	t <sub>WCH</sub>	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ pulse width	t <sub>WP</sub>	8	–	10	–	10	–	15	–	ns	1
$\overline{WE}$ lead time referenced to $\overline{RAS}$	t <sub>RWL</sub>	18	–	20	–	20	–	20	–	ns	
$\overline{WE}$ lead time referenced to $\overline{CAS}$	t <sub>CWL</sub>	13	–	15	–	15	–	15	–	ns	
$\overline{WE}$ setup time	t <sub>WCS</sub>	0	–	0	–	0	–	0	–	ns	2
$\overline{OE}$ hold time	t <sub>OEH</sub>	0	–	0	–	0	–	0	–	ns	
Data-in setup time	t <sub>DS</sub>	0	–	0	–	0	–	0	–	ns	3
Data-in hold time	t <sub>DH</sub>	10	–	10	–	15	–	15	–	ns	3

- Notes**
1. t<sub>WP</sub>(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t<sub>WCH</sub>(MIN.) should be met.
  2. If t<sub>WCS</sub> ≥ t<sub>WCS</sub>(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
  3. t<sub>DS</sub>(MIN.) and t<sub>DH</sub>(MIN.) are referenced to the  $\overline{CAS}$  falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the  $\overline{WE}$  falling edge.

**Read Modify Write Cycle**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		t <sub>RAC</sub> = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read modify write cycle time	t <sub>RWC</sub>	133	–	160	–	180	–	205	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t <sub>RWD</sub>	70	–	85	–	95	–	110	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ delay time	t <sub>CWD</sub>	33	–	40	–	43	–	50	–	ns	1
Column address to $\overline{WE}$ delay time	t <sub>AWD</sub>	45	–	55	–	60	–	70	–	ns	1

- Note**
1. If t<sub>WCS</sub> ≥ t<sub>WCS</sub>(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t<sub>RWD</sub> ≥ t<sub>RWD</sub>(MIN.), t<sub>CWD</sub> ≥ t<sub>CWD</sub>(MIN.), t<sub>AWD</sub> ≥ t<sub>AWD</sub>(MIN.) and t<sub>CPWD</sub> ≥ t<sub>CPWD</sub>(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

**Fast Page Mode**

Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		t <sub>RAC</sub> = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Fast page mode cycle time	t <sub>PC</sub>	35	–	40	–	45	–	50	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	t <sub>ACP</sub>	–	30	–	35	–	40	–	45	ns	
$\overline{\text{RAS}}$ pulse width	t <sub>RASP</sub>	50	125,000	60	125,000	70	125,000	80	125,000	ns	
$\overline{\text{CAS}}$ precharge time	t <sub>CP</sub>	8	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t <sub>RHCP</sub>	30	–	35	–	40	–	45	–	ns	
Read modify write cycle time	t <sub>PRWC</sub>	73	–	83	–	90	–	95	–	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time	t <sub>CPWD</sub>	50	–	58	–	65	–	70	–	ns	1

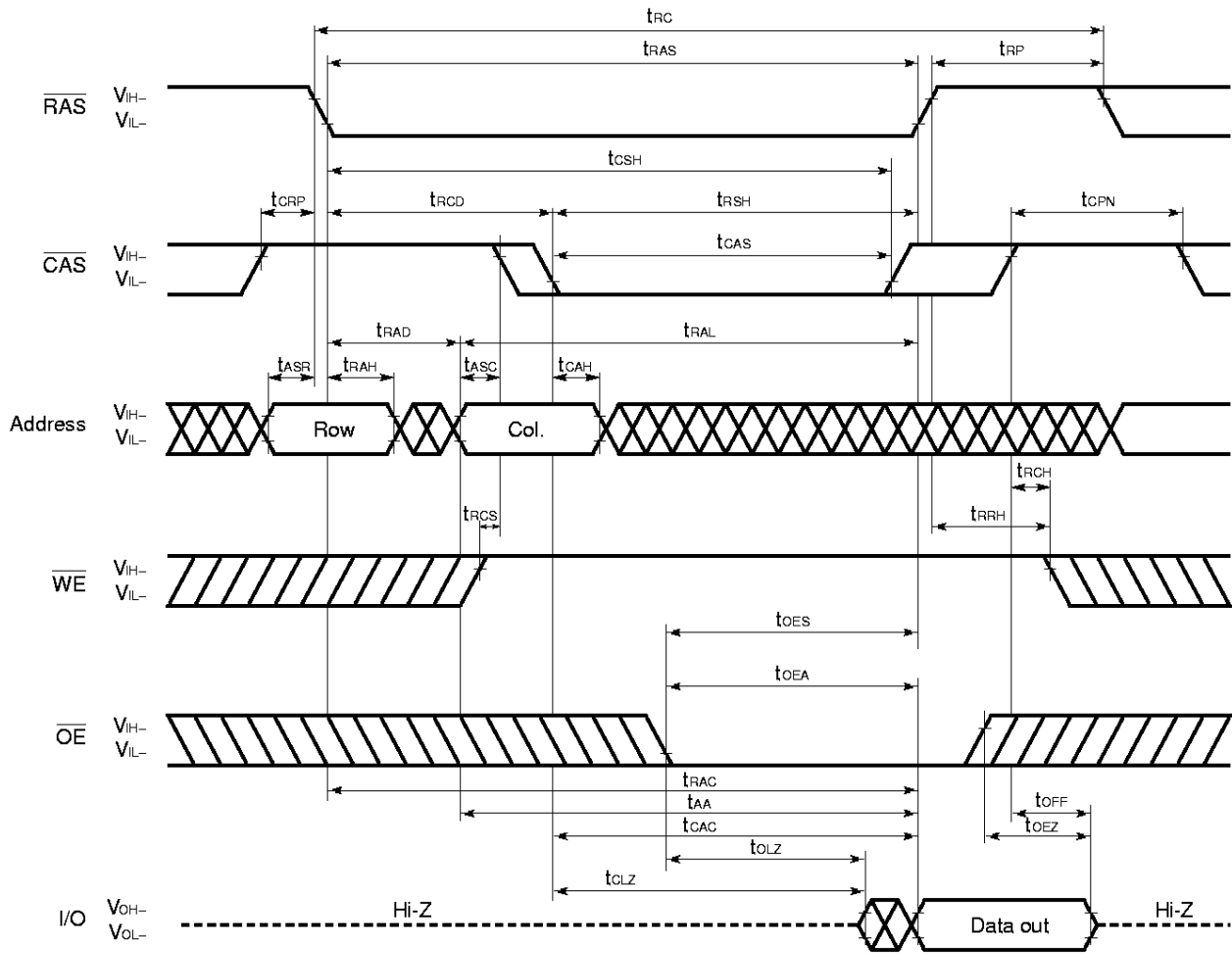
**Note 1.** If  $t_{wCS} \geq t_{wCS(MIN.)}$ , the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If  $t_{rWD} \geq t_{rWD(MIN.)}$ ,  $t_{cWD} \geq t_{cWD(MIN.)}$ ,  $t_{aWD} \geq t_{aWD(MIN.)}$  and  $t_{cPWD} \geq t_{cPWD(MIN.)}$ , the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

**Refresh Cycle**

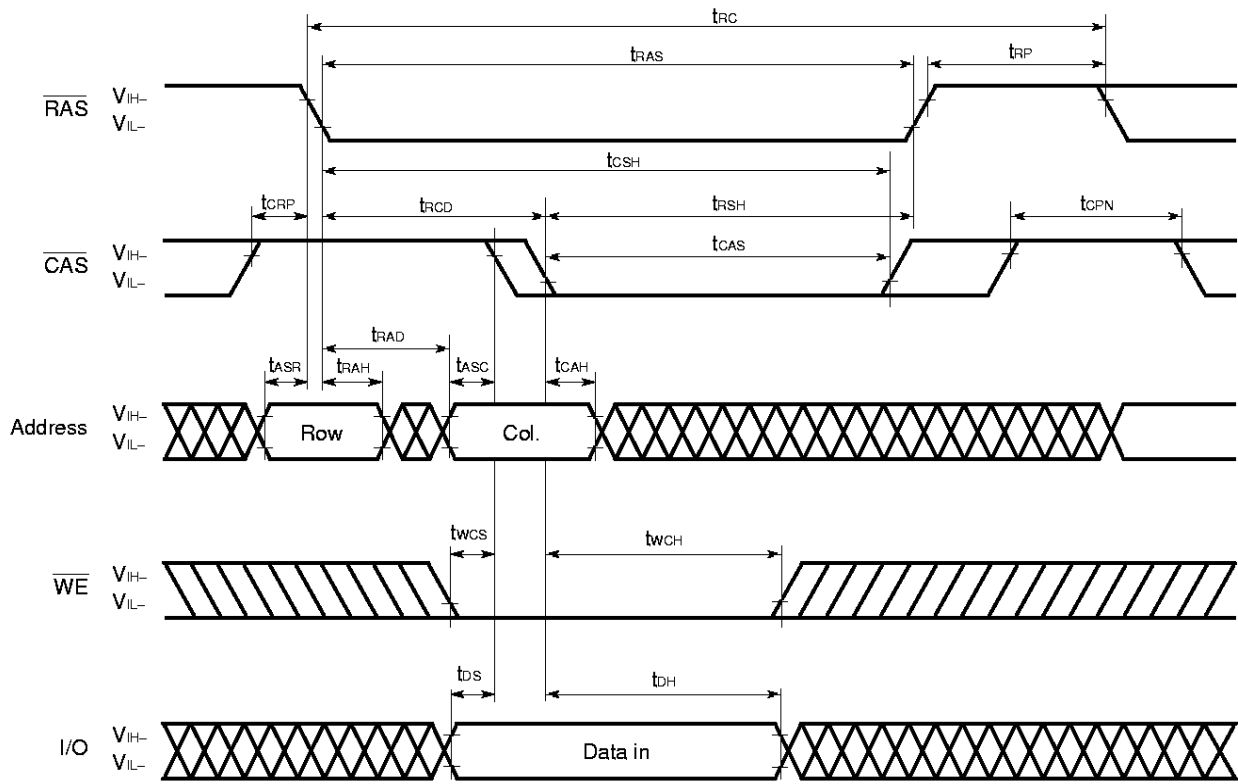
Parameter	Symbol	t <sub>RAC</sub> = 50 ns		t <sub>RAC</sub> = 60 ns		t <sub>RAC</sub> = 70 ns		t <sub>RAC</sub> = 80 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{\text{CAS}}$ setup time	t <sub>CSR</sub>	5	–	5	–	5	–	5	–	ns	
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t <sub>CHR</sub>	10	–	10	–	10	–	10	–	ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t <sub>RPC</sub>	5	–	5	–	5	–	5	–	ns	
$\overline{\text{RAS}}$ pulse width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t <sub>RASS</sub>	100	–	100	–	100	–	100	–	μs	1
$\overline{\text{RAS}}$ precharge time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t <sub>RPS</sub>	90	–	110	–	130	–	150	–	ns	1
$\overline{\text{CAS}}$ hold time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh)	t <sub>CHS</sub>	–50	–	–50	–	–50	–	–50	–	ns	1
$\overline{\text{WE}}$ setup time	t <sub>WSR</sub>	10	–	10	–	10	–	10	–	ns	
$\overline{\text{WE}}$ hold time	t <sub>WHR</sub>	15	–	15	–	15	–	15	–	ns	

**Note 1.** This specification is applied only to the μPD42S16400, 42S17400.

Read Cycle

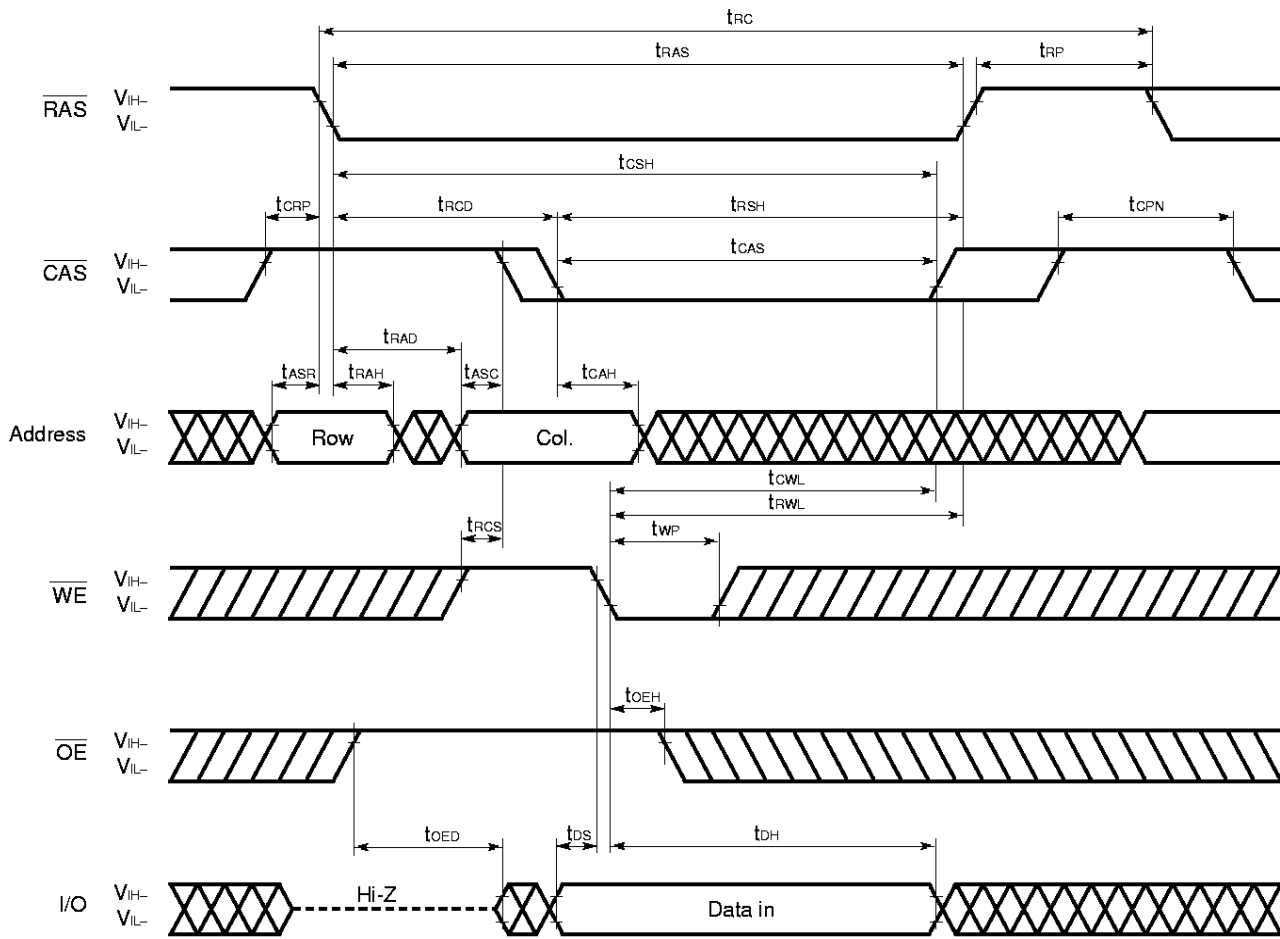


Early Write Cycle



Remark  $\overline{OE}$ : Don't care

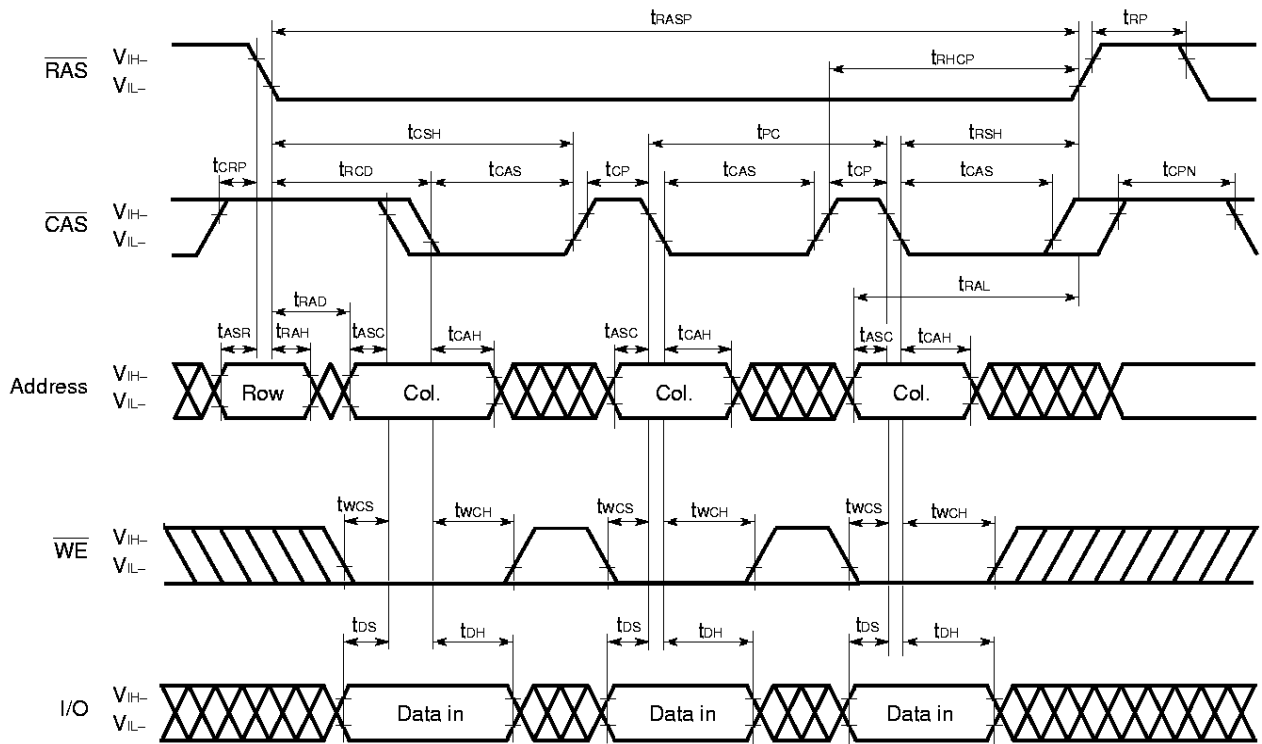
Late Write Cycle







Fast Page Mode Early Write Cycle

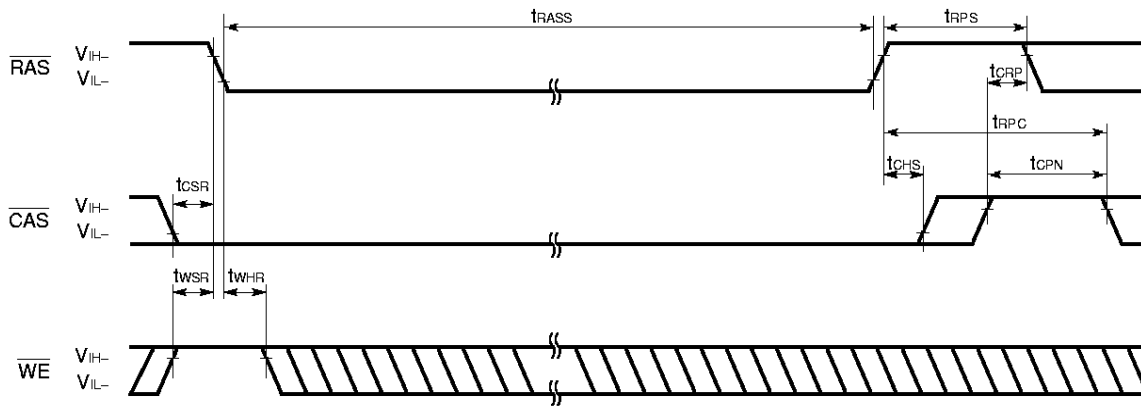


- Remarks**
1.  $\overline{\text{OE}}$  : Don't care
  2. In the fast page mode, read, write and read modify write cycles are available for each of the consecutive  $\overline{\text{CAS}}$  cycles within the same  $\overline{\text{RAS}}$  cycle.





**CAS Before RAS Self Refresh Cycle (Only for the  $\mu$ PD42S16400, 42S17400)**



**Remark** Address,  $\overline{OE}$  : Don't care I/O : Hi-Z

**Cautions on Use of  $\overline{CAS}$  Before  $\overline{RAS}$  Self Refresh**

$\overline{CAS}$  before  $\overline{RAS}$  self refresh can be used independently when used in combination with distributed  $\overline{CAS}$  before  $\overline{RAS}$  long refresh; However, when used in combination with burst  $\overline{CAS}$  before  $\overline{RAS}$  long refresh or with long  $\overline{RAS}$  only refresh (both distributed and burst), the following cautions must be observed.

**(1) Normal Combined Use of  $\overline{CAS}$  Before  $\overline{RAS}$  Self Refresh and Burst  $\overline{CAS}$  Before  $\overline{RAS}$  Long Refresh**

When  $\overline{CAS}$  before  $\overline{RAS}$  self refresh and burst  $\overline{CAS}$  before  $\overline{RAS}$  long refresh are used in combination, please perform  $\overline{CAS}$  before  $\overline{RAS}$  refresh as follows just before and after setting  $\overline{CAS}$  before  $\overline{RAS}$  self refresh.

$\mu$ PD42S16400: 4,096 times within a 64 ms interval

$\mu$ PD42S17400: 2,048 times within a 32 ms interval

**(2) Normal Combined Use of  $\overline{CAS}$  Before  $\overline{RAS}$  Self Refresh and Long  $\overline{RAS}$  Only Refresh**

When  $\overline{CAS}$  before  $\overline{RAS}$  self refresh and  $\overline{RAS}$  only refresh are used in combination, please perform  $\overline{RAS}$  only refresh as follows just before and after setting  $\overline{CAS}$  before  $\overline{RAS}$  self refresh.

$\mu$ PD42S16400: 4,096 times within a 64 ms interval

$\mu$ PD42S17400: 2,048 times within a 32 ms interval

**★ (3) If  $t_{RASS(MIN.)}$  is not satisfied at the beginning of  $\overline{CAS}$  before  $\overline{RAS}$  self refresh cycles ( $t_{RAS} < 100 \mu s$ ),  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycles will be executed one time.**

If  $10 \mu s < t_{RAS} < 100 \mu s$ ,  $\overline{RAS}$  precharge time for  $\overline{CAS}$  before  $\overline{RAS}$  self refresh ( $t_{RPS}$ ) is applied.

And refresh cycles as follows should be met.

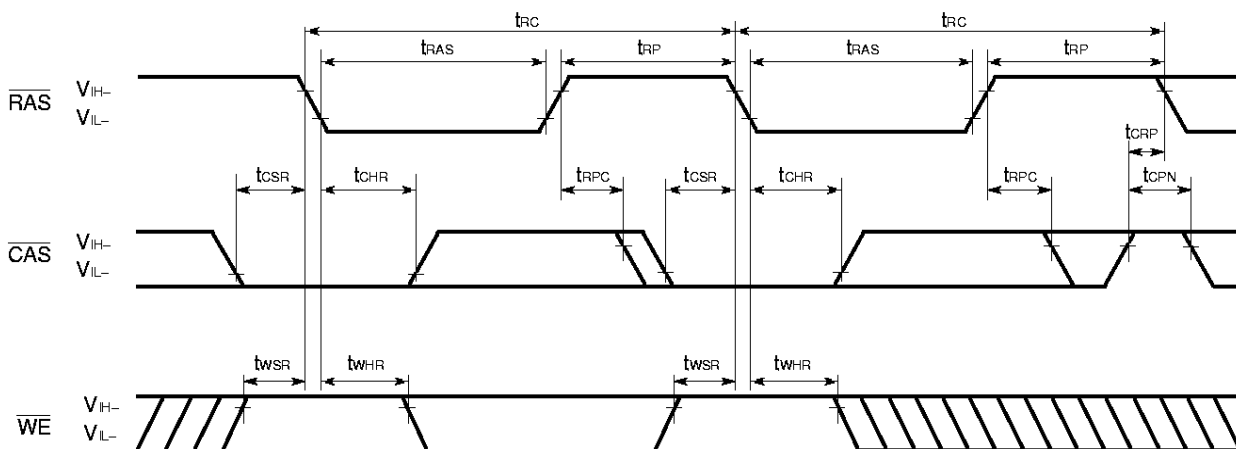
$\mu$ PD42S16400: 4,096 times within a 128 ms interval

$\mu$ PD42S17400: 2,048 times within a 128 ms interval

For details, please refer to **How to use DRAM** User's Manual.

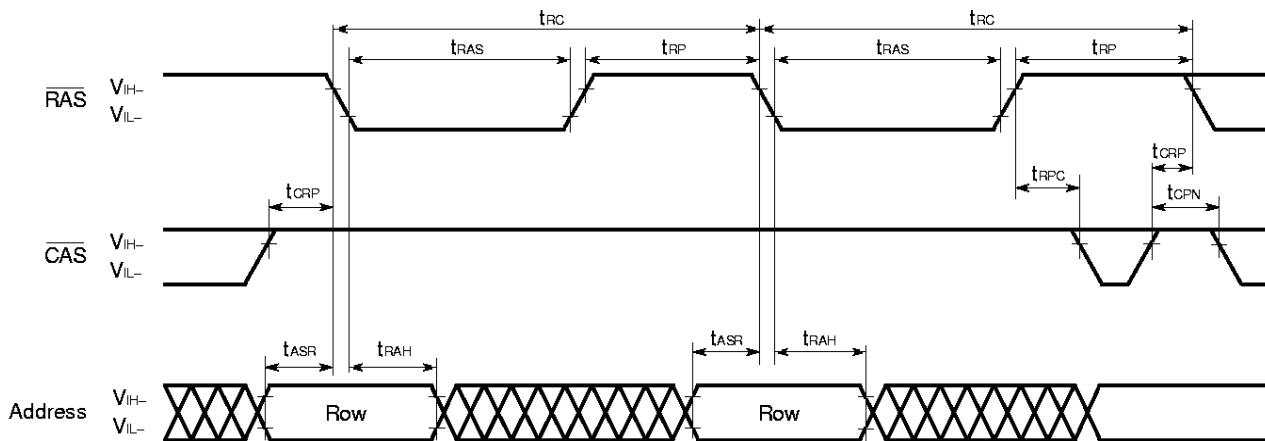
**CAS Before RAS Refresh Cycle**

★



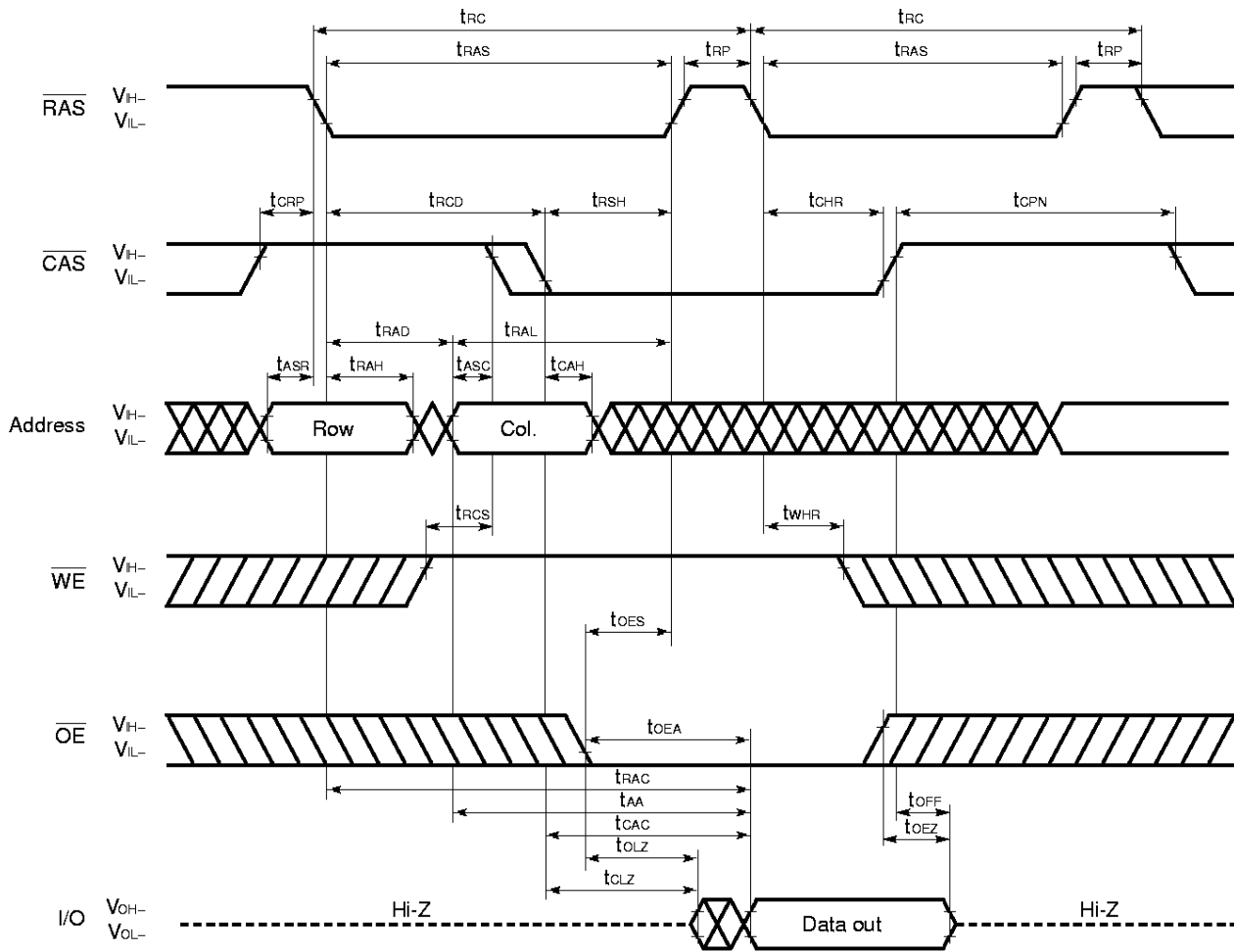
**Remark** Address,  $\overline{\text{OE}}$ : Don't care I/O: Hi-Z

**RAS Only Refresh Cycle**

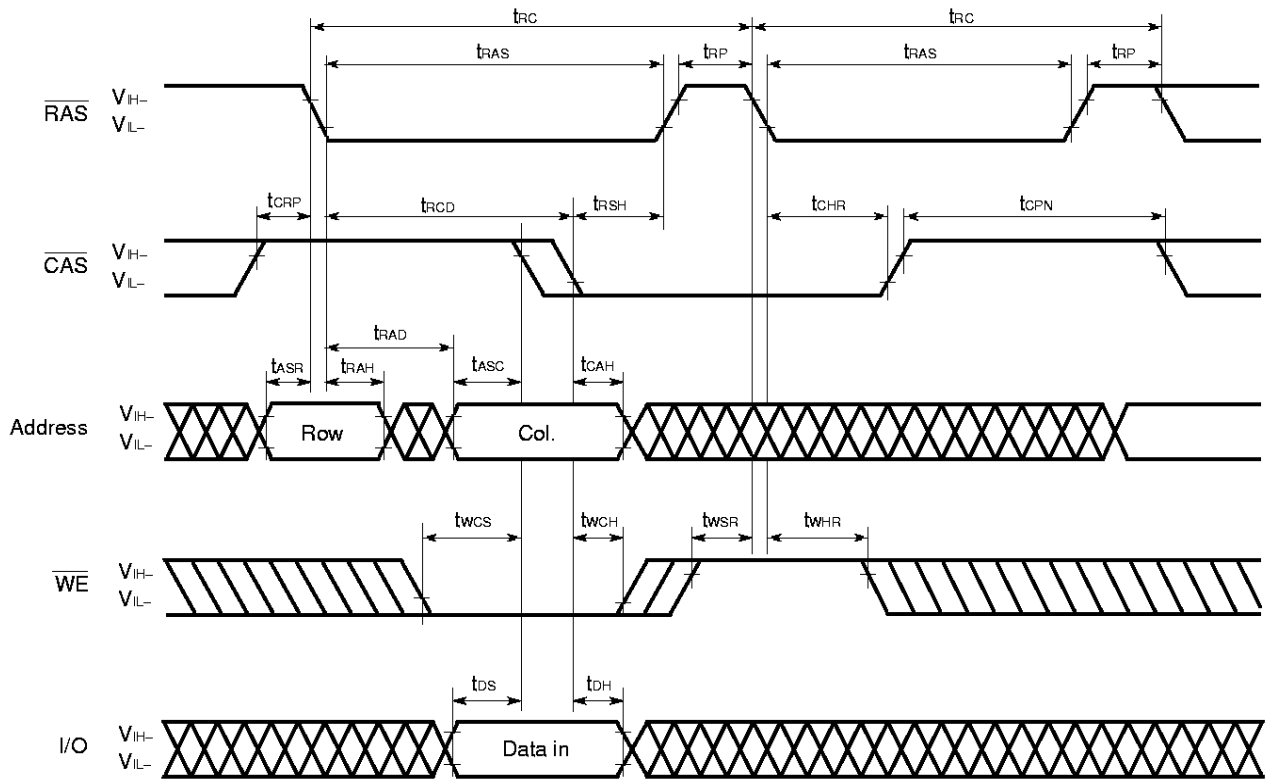


**Remark**  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ : Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

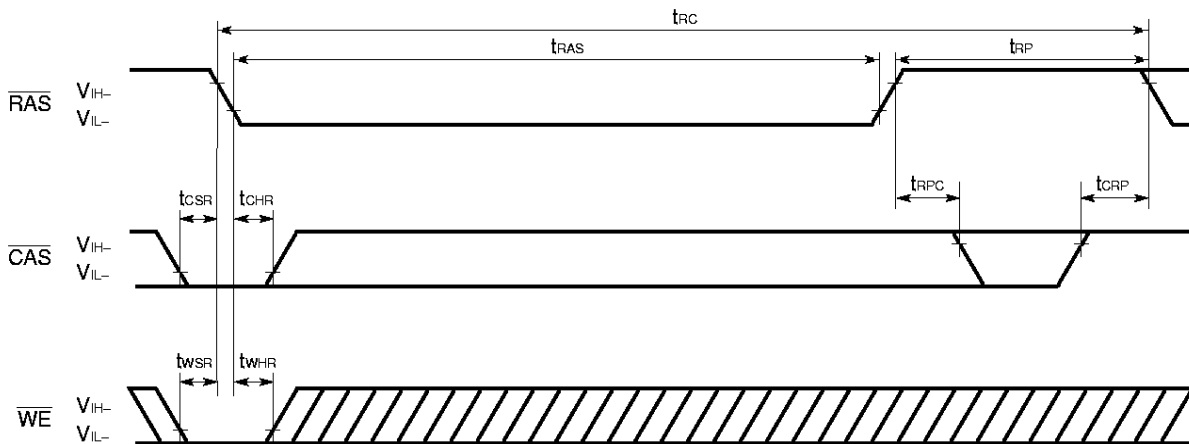


Hidden Refresh Cycle (Write)



Remark  $\overline{OE}$  : Don't care

**Test Mode Set Cycle ( $\overline{WE}$ ,  $\overline{CAS}$  Before  $\overline{RAS}$  Refresh Cycle)**



**Remark** Address,  $\overline{OE}$ : Don't care I/O: Hi-Z

**Test Mode**

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the  $\times 16$ -bit organization during test mode. Don't care about the input levels of the  $\overline{CAS}$  input A0, A1.

**(1) Setting the mode**

Executing the test mode cycle ( $\overline{WE}$ ,  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle) sets the test mode.

**(2) Write/read operation**

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

**(3) Refresh**

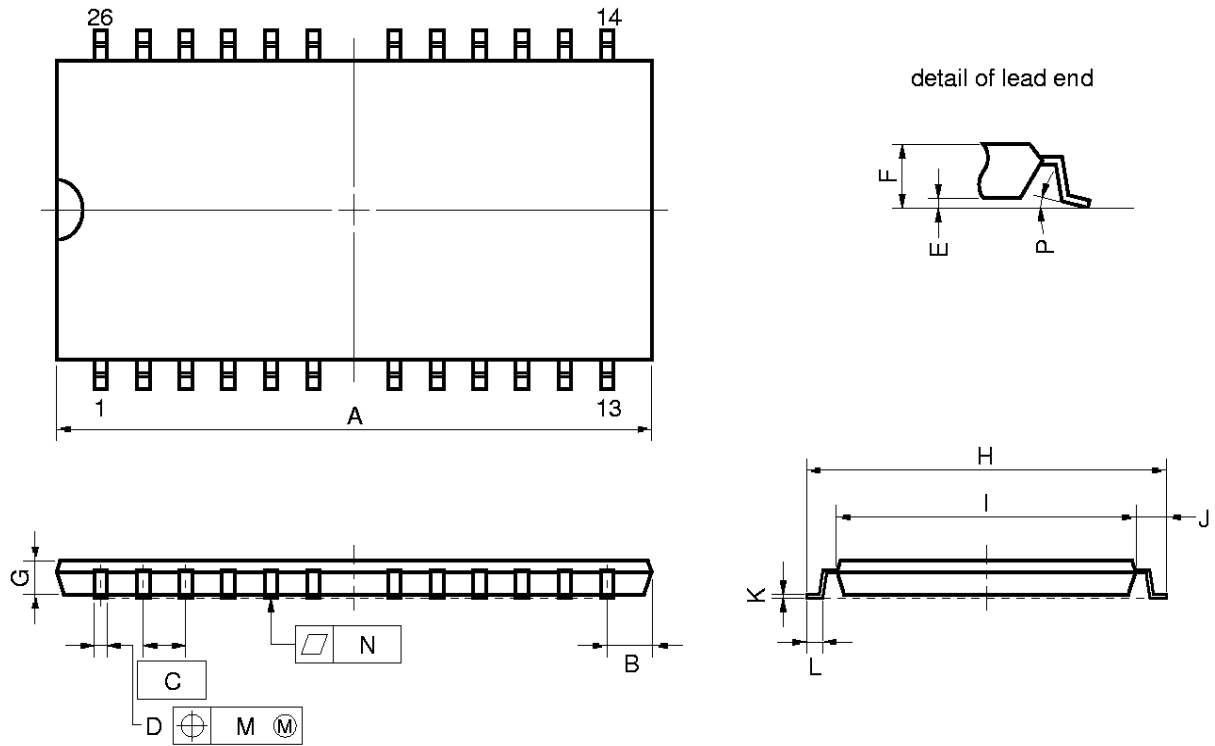
Refresh in the test mode must be performed with the  $\overline{RAS}$  /  $\overline{CAS}$  cycle or with the  $\overline{WE}$ ,  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle. The  $\overline{WE}$ ,  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle use the same counter as the  $\overline{CAS}$  before  $\overline{RAS}$  refresh's internal counter.

**(4) Mode Cancellation**

The test mode is cancelled by executing one cycle of  $\overline{RAS}$  only refresh cycle or  $\overline{CAS}$  before  $\overline{RAS}$  refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



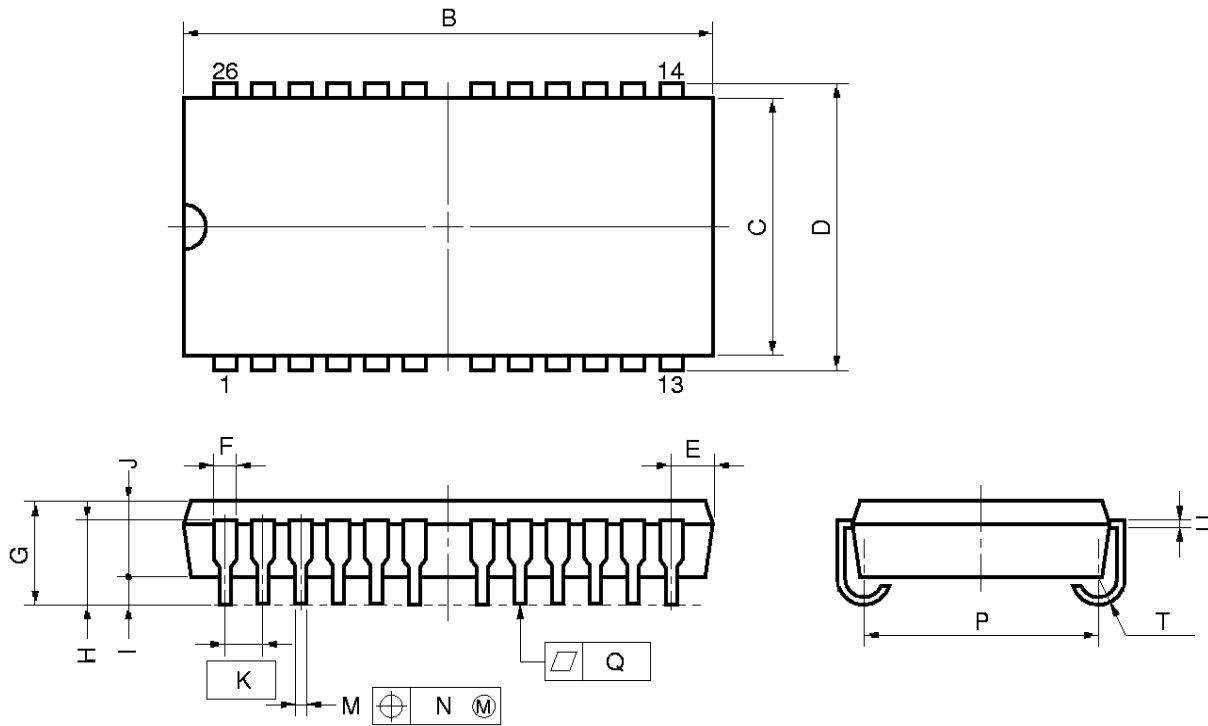
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.36 MAX.	0.684 MAX.
B	1.06 MAX.	0.042 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.42 <sup>+0.08</sup> <sub>-0.07</sub>	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	9.22±0.2	0.363±0.008
I	7.62±0.1	0.300±0.004
J	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>	0.006±0.001
L	0.5±0.1	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
M	0.21	0.009
N	0.10	0.004
P	3° <sup>+7°</sup> <sub>-3°</sub>	3° <sup>+7°</sup> <sub>-3°</sub>

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	17.3 <sup>+0.20</sup> <sub>-0.25</sub>	0.681 <sup>+0.008</sup> <sub>-0.010</sub>
C	7.62	0.300
D	8.47±0.2	0.333 <sup>+0.009</sup> <sub>-0.008</sub>
E	1.03±0.15	0.041 <sup>+0.006</sup> <sub>-0.007</sub>
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
N	0.12	0.005
P	6.73±0.2	0.265±0.008
Q	0.10	0.004
T	R0.85	R0.033
U	0.20 <sup>+0.10</sup> <sub>-0.05</sub>	0.008 <sup>+0.004</sup> <sub>-0.002</sub>

S26LA-300A-1

**Recommended Soldering Conditions**

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16400, 4216400, 42S17400, 4217400.

For more details, refer to our document “SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

**Types of Surface Mount Device**

**μPD42S16400G3-7JD, 4216400G3-7JD, 42S17400G3-7JD, 4217400G3-7JD: 26-pin plastic TSOP (II) (300 mil)**

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days <sup>Note</sup> (10 hours pre-baking is required at 125 °C afterwards)  <b>Cautions</b> 1. <b>After the first reflow process, cool the package down to room temperature, then start the second reflow process.</b> 2. <b>After the first reflow process, do not use water to remove residual flux (water can be used in the second process).</b>	IR35-107-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days <sup>Note</sup> (10 hours pre-baking is required at 125 °C afterwards)  <b>Cautions</b> 1. <b>After the first reflow process, cool the package down to room temperature, then start the second reflow process.</b> 2. <b>After the first reflow process, do not use water to remove residual flux (water can be used in the second process).</b>	VP15-107-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package).	_____

**Note** Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

**Caution** Do not apply more than one soldering method at any one time, except for “Partial heating method”.

μPD42S16400LA, 4216400LA, 42S17400LA, 4217400LA: 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days <sup>Note</sup> (20 hours pre-baking is required at 125 °C afterwards)  <b>Cautions</b> 1. <b>After the first reflow process, cool the package down to room temperature, then start the second reflow process.</b> 2. <b>After the first reflow process, do not use water to remove residual flux (water can be used in the second process).</b>	IR35-207-2
VPS	Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 2 Exposure limit: 7 days <sup>Note</sup> (20 hours pre-baking is required at 125 °C afterwards)  <b>Cautions</b> 1. <b>After the first reflow process, cool the package down to room temperature, then start the second reflow process.</b> 2. <b>After the first reflow process, do not use water to remove residual flux (water can be used in the second process).</b>	VP15-207-2
Partial heating method	Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package).	_____

**Note** Exposure limit before soldering after dry-pack package is opened.  
 Storage conditions: 25 °C and relative humidity at 65 % or less.

**Caution** Do not apply more than one soldering method at any one time, except for “Partial heating method”.

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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NEC devices are classified into the following three quality grades:

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices in "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.