NEC

Preliminary User's Manual

USB Host Controller

μPD9210FGC-7EA

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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PREFACE

This manual describes a USB host controller that complies with the **Open Host Controller Interface Specification Release 1.0** and **OpenHCI Legacy Support Interface Specification Release Version 1.01**.

Read this manual thoroughly to help ensure smooth system design. Also, be sure to observe the various notes in this manual (general notes, caution points, and restrictions). Operation faults and a reduction in the quality and performance levels of LSI products may occur if these notes are not observed.

Before starting a design, contact your local NEC sales representative or distributor to make sure you have the most recent documentation.

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CHAPTER 1 FEATURES

1.1 Features

(1) Functions

- Complies with **OpenHCI Specification Release 1.0** and **OpenHCI Legacy Support Interface Specification Release Version 1.01**.
- Supports asynchronous communication between host CPU and USB devices.
- Supports two types of USB devices: full speed (12 Mbps) devices and low speed (1.5 Mbps) devices.
- System clock: 48 MHz

(2) Interface

- USB interface transceiver
  Complies with **Universal Serial Bus Specification Revision 1.0**.
  Switchable between full speed (12 Mbps) and low speed (1.5 Mbps) modes.
- PCI interface buffer
  Complies with **PCI Local Bus Specification Revision 2.1** and **PCI Mobile Design Guide Revision 1.0**.
  Supports 32-bit, 33-MHz, 5-VPCI/3.3-VPCI operation.

(3) Communication with host CPU

- Communicates via Operational Registers built into USB host controller
- Communicates via the Host Controller Communication Area in the system memory space

(4) Memory and I/O space

- Maps to 4-Kbyte space within the 4-Gbyte system memory space.
- 256-byte Host Controller Communication Area is allocated in the system memory space.
- The legacy support register is allocated to 60h/64h in the I/O space.

(5) Legacy support

- USB keyboard + USB mouse, USB keyboard + legacy mouse
- Legacy keyboard + USB mouse, legacy keyboard + legacy mouse

(6) On-chip FIFO

- PCI side
  Read: 16 bytes (4 × 4 Dwords), Write: 16 bytes (4 × 4 Dwords)
- USB side
  64 bytes (64 × 1 byte)

(7) Root Hub

- Equipped with two downstream ports

(8) Low power consumption

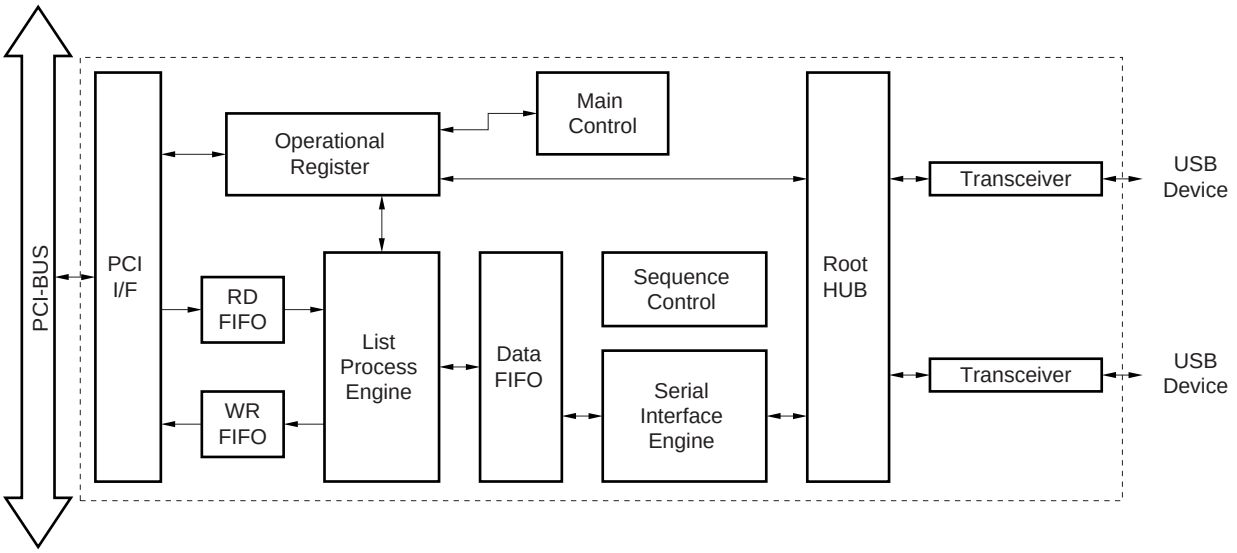
- On-chip clock run function
- On-chip PCI clock stop/USB clock stop functions

(9) Others

- CMOS process
- 3-V single power supply

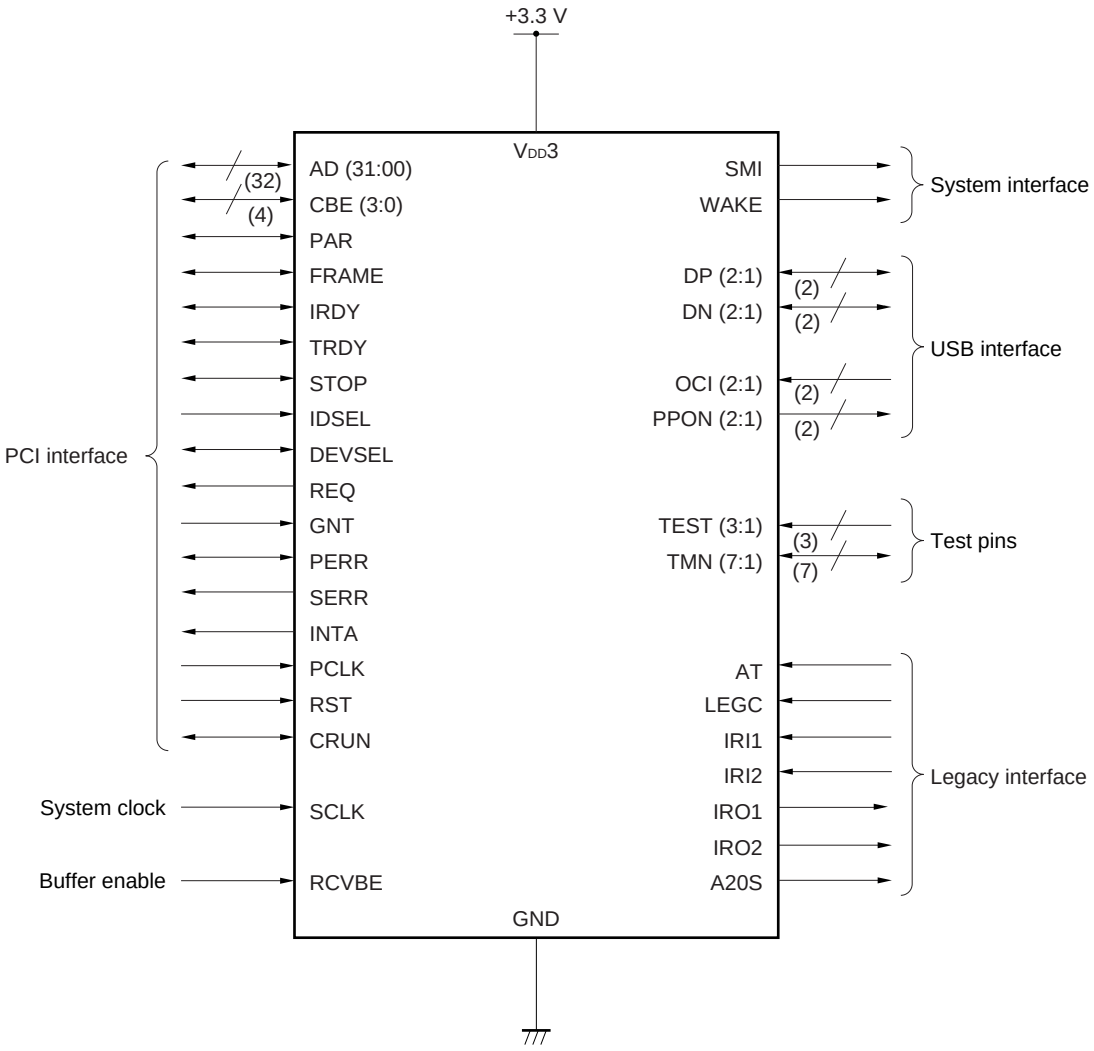
1.2 Block Diagram

Figure 1-1. Block Diagram



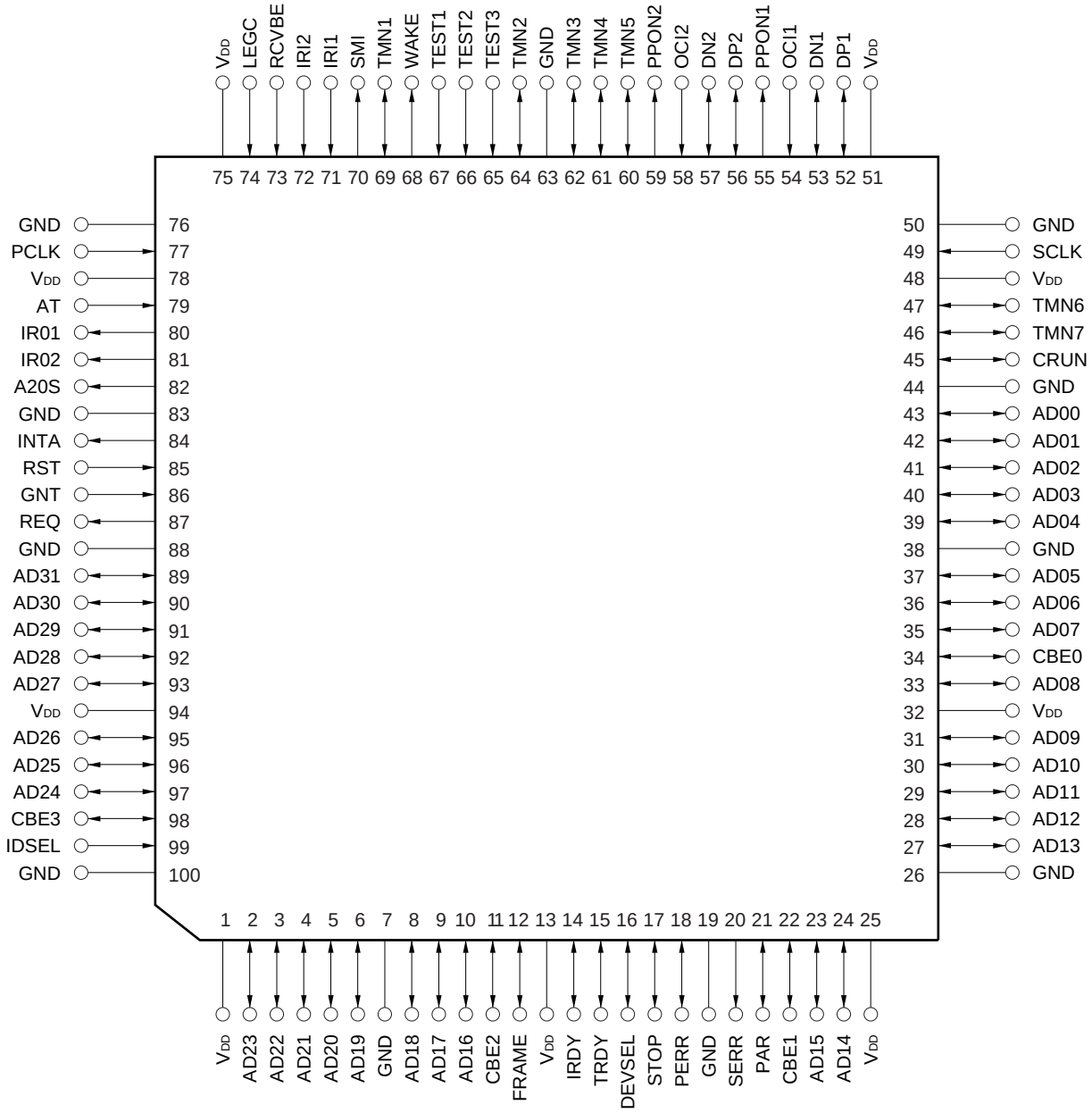
1.3 Pin Configuration

Figure 1-2. Pin Configuration



1.4 Pin Configuration Diagram

Figure 1-3. Pin Configuration Diagram



1.5 Pin Names and Pin Numbers

AD (31:00)	:	PCI Address and Data	SMI	:	System Management Interrupt
CBE (3:0)	:	PCI Bus Command and Byte Enable	DP (2:1)	:	USB D+
PAR	:	PCI Parity	DN (2:1)	:	USB D–
FRAME	:	PCI Cycle Frame	OCI (2:1)	:	Over Current Interrupt
IRDY	:	PCI Initiator Ready	PPON (2:1)	:	Port Power ON
TRDY	:	PCI Target Ready	SCLK	:	System Clock
STOP	:	PCI Stop	RCVBE	:	USB Receiver and Input Buffer Enable
IDSEL	:	PCI Initialization Device Select	AT	:	AT Mode Enable
DEVSEL	:	PCI Device Select	LEGC	:	Legacy Support Enable
REQ	:	PCI Request	IRI1	:	IRQ1 Input
GNT	:	PCI Grant	IRI2	:	IRQ12 Input
PERR	:	PCI Parity Error	IRO1	:	IRQ1 Output
SERR	:	PCI System Error	IRO2	:	IRQ12 Output
INTA	:	PCI Interrupt	A20S	:	GateA20 State
PCLK	:	PCI Clock	WAKE	:	Wakeup Interrupt
RST	:	PCI Reset	TEST (3:1)	:	TEST Control
CRUN	:	PCI Clock running	TMN (7:1)	:	TEST signal

Table 1-1. Pin Numbers

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	V_{DD}	26	GND	51	V_{DD}	76	GND
2	AD23	27	AD13	52	DP1	77	PCLK
3	AD22	28	AD12	53	DN1	78	V_{DD}
4	AD21	29	AD11	54	OCI1	79	AT
5	AD20	30	AD10	55	PPON1	80	IRO1
6	AD19	31	AD09	56	DP2	81	IRO2
7	GND	32	V_{DD}	57	DN2	82	A20S
8	AD18	33	AD08	58	OCI2	83	GND
9	AD17	34	CBE0	59	PPON2	84	INTA
10	AD16	35	AD07	60	TMN5	85	RST
11	CBE2	36	AD06	61	TMN4	86	GNT
12	FRAME	37	AD05	62	TMN3	87	REQ
13	V_{DD}	38	GND	63	GND	88	GND
14	IRDY	39	AD04	64	TMN2	89	AD31
15	TRDY	40	AD03	65	TEST3	90	AD30
16	DEVSEL	41	AD02	66	TEST2	91	AD29
17	STOP	42	AD01	67	TEST1	92	AD28
18	PERR	43	AD00	68	WAKE	93	AD27
19	GND	44	GND	69	TMN1	94	V_{DD}
20	SERR	45	CRUN	70	SMI	95	AD26
21	PAR	46	TMN7	71	IRI1	96	AD25
22	CBE1	47	TMN6	72	IRI2	97	AD24
23	AD15	48	V_{DD}	73	RCVBE	98	CBE3
24	AD14	49	SCLK	74	LEGC	99	IDSEL
25	V_{DD}	50	GND	75	V_{DD}	100	GND

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Table

Table 2-1. Pin Table

Pin Name	I/O	Buffer Type	Active Level	Function
AD (31 : 0)	I/O	5 V PCI I/O		PCI “AD [31 : 0]” signal
CBE (3 : 0)	I/O	5 V PCI I/O		PCI “C/BE [3 : 0]” signal
PAR	I/O	5 V PCI I/O		PCI “PAR” signal
FRAME	I/O	5 V PCI I/O		PCI “FRAME#” signal
IRDY	I/O	5 V PCI I/O		PCI “IRDY#” signal
TRDY	I/O	5 V PCI I/O		PCI “TRDY#” signal
STOP	I/O	5 V PCI I/O		PCI “STOP#” signal
IDSEL	I	5 V PCI Input		PCI “IDSEL” signal
DEVSEL	I/O	5 V PCI I/O		PCI “DEVSEL#” signal
REQ	O	5 V PCI Output		PCI “REQ#” signal
GNT	I	5 V PCI Input		PCI “GNT#” signal
PERR	I/O	5 V PCI I/O		PCI “PERR#” signal
SERR	O	5 V PCI N-ch Open Drain		PCI “SERR#” signal
INTA	O	5 V PCI N-ch Open Drain	Low	PCI “INTA#” signal
PCLK	I	5 V PCI Input		PCI “CLK” signal
RST	I	5 V Schmitt Input	Low	PCI “RST#” signal
CRUN	I/O	5 V PCI I/O (N-ch Open Drain)		PCI “CLKRUN#” signal
SCLK	I	5 V Schmitt Input		System clock input
SMI	O	5 V I_{OL} = 12 mA N-ch Open Drain	Low	System management interrupt output
DP (2 : 1)	I/O	USB D+I/O		USB’s D+ signal
DN (2 : 1)	I/O	USB D–I/O		USB’s D– signal
OCI (2 : 1)	I (I/O)	5 V Input with excessive through current prevention function	High	USB Root Hub Port’s overcurrent status input
PPON (2 : 1)	O	5 V I_{OL} = 6 mA Output	High	USB Root Hub Port’s power supply control output
RCVBE	I	5 V Input	High	USB Receiver and Input Buffer Enable signal
AT	I (I/O)	5 V Schmitt Input	High	Legacy support switch
LEGC	I (I/O)	5 V Schmitt Input	High	Legacy support switch
IRI1	I (I/O)	5 V Input with excessive through current prevention function	High	INT input from keyboard
IRI2	I (I/O)	5 V Input with excessive through current prevention function	High	INT input from mouse
IRO1	O	5 V I_{OL} = 6 mA N-ch Open Drain	High	INT output from keyboard
IRO2	O (I/O)	5 V I_{OL} = 6 mA N-ch Open Drain	High	INT output from mouse
A20S	O (I/O)	5 V I_{OL} = 6 mA N-ch Open Drain		GateA20 State output
WAKE	O	5 V I_{OL} = 6 mA Output	High	Wakeup interrupt output
TEST (3 : 1)	I	3 V Input with 50 kΩ Pull up R		Test pin
TMN (7 : 1)	I/O	3 V I/O with 50 kΩ Pull up R		Test pin

Remarks 1. The 5-V buffer in the table indicates a 5-V tolerant buffer. “5-V tolerant” means that the buffer is a 3-V buffer with 5-V maximum voltage.

2. “5 V PCI” indicates a PCI buffer that has a 5-V maximum voltage circuit which complies with the 3-V PCI standard. It does not indicate a buffer that fully complies with the 5-V PCI standard. However, this function can be used for evaluating the operation of a device by attaching a 5-V add-in card beforehand.

3. The signals marked as “(I/O)” in the above table operate as I/O signals during testing.
However, they do not need to be considered in normal use situations.

2.2 Description of Pin Functions

- **Power supply**

Pin	Pin No.	Direction	Function
V_{DD}	1, 13, 25, 32, 48, 51, 75, 78, 94	–	+3 V power supply
GND	7, 19, 26, 38, 44, 50, 63, 76, 83, 88, 100	–	Ground

- **PCI interface**

Pin	Pin No.	Direction	Function
AD (31 : 00)	2 to 6, 8 to 10, 23, 24, 27 to 31, 33, 35 to 37, 39 to 43, 89 to 93, 95 to 97	I/O	PCI “AD [31 : 00]” signal
CBE (3 : 0)	11, 22, 34, 98	I/O	PCI “C/BE [3 : 0]” signal
PAR	21	I/O	PCI “PAR” signal
FRAME	12	I/O	PCI “FRAME#” signal
IRDY	14	I/O	PCI “IRDY#” signal
TRDY	15	I/O	PCI “TRDY#” signal
STOP	17	I/O	PCI “STOP#” signal
IDSEL	99	I	PCI “IDSEL” signal
DEVSEL	16	I/O	PCI “DEVSEL#” signal
REQ	87	O	PCI “REQ#” signal
GNT	86	I	PCI “GNT#” signal
PERR	18	I/O	PCI “PERR#” signal
SERR	20	O	PCI “SERR#” signal
INTA	84	O	PCI “INTA#” signal
PCLK	77	I	PCI “CLK” signal
RST	85	I	PCI “RST#” signal
CRUN	45	I/O	PCI “CLKRUN#” signal

Remark For details of PCI operations, see the **PCI Local Bus Specification Revision 2.1**.

- **System clock**

Pin	Pin No.	Direction	Caution
SCLK	49	I	System clock input Apply 48-MHz clock input.

- **Test pins**

Pin	Pin No.	Direction	Caution
TEST (3 : 1)	65, 66, 67	I	Be sure to leave open on circuit board.
TMN (7 : 1)	46, 47, 60, 61, 62, 64, 69	I/O	Be sure to leave open on circuit board.

- **System interface**

Pin	Pin No.	Direction	Function
SMI	70	O	System management interrupt output Changed to INTA by ownership change before being output. 0: Interrupt occurs 1: Interrupt does not occur
RCVBE	73	I	USB Receiver/Input Buffer Enable signal 0: Excessive through current prevention/differential buffer operating current cut-off function ON 1: Excessive through current prevention/differential buffer operating current cut-off function OFF The pins being controlled are as follows. DP (2 : 1), DN (2 : 1), OCI (2 : 1), IRI1, IRI2
WAKE	68	O	Wakeup request signal is output from the USB. 0: No Wakeup request 1: Wakeup request exists

- **USB interface**

Pin	Pin No.	Direction	Function
DP (2 : 1)	52, 56	I/O	USB's D+ signal Shared with DNx pins having the same numbers.
DN (2 : 1)	53, 57	I/O	USB's D– signal Shared with DPx pins having the same numbers.
OCI (2 : 1)	54, 58	I	Pin for inputting the overcurrent status of the USB Root Hub Port 0: No power supply problem 1: Overcurrent has occurred
PPON (2 : 1)	55, 59	O	Power supply control output for USB Root Hub Port 0: Power supply OFF 1: Power supply ON

- **Legacy support interface**

Pin	Pin No.	Direction	Function
AT	79	I	Legacy support 0: Legacy OFF 1: Legacy ON
LEGC	74	I	Legacy support switch 0: Legacy OFF 1: Legacy ON When off, “L” clamp IRI1 and IRI2 and leave IRO1, IRO2, and A20S open.
IRI1[Note]	71	I	INT input from keyboard: active H
IRI2[Note]	72	I	INT input from mouse: active H
IRO1	80	O	INT output from keyboard: active H
IRO2	81	O	INT output from mouse: active H
A20S	82	O	GateA20 State output

Note IRQ is sampled using the 12-MHz clock signal generated by SCLK, and an interrupt is detected as a result. The next IRQ is not received during emulation. After emulation is completed, an interrupt can be received once the IRQ's H level has been sampled.

2.3 Handling Unused Pins

Handle unused pins as shown below.

Pin	Direction	Connection Method
DPx	I/O	Connect via 15 kΩ ±5% pull-down resistor.
DNx	I/O	Connect via 15 kΩ ±5% pull-down resistor.
OCIx	I	“L” clamp
PPONx	O	No Connection (Open)
TEST (3 : 1)	I	No Connection (Open)
TMN (1 : 7)	I/O	No Connection (Open)

When the legacy function is off (AT = L, LEGC = L), handle unused pins as shown below.

Pin	Direction	Connection Method
IRI1	I	“L” clamp
IRI2	I	“L” clamp
IRO1	O	No Connection (Open)
IRO2	O	No Connection (Open)
A20S	O	No Connection (Open)

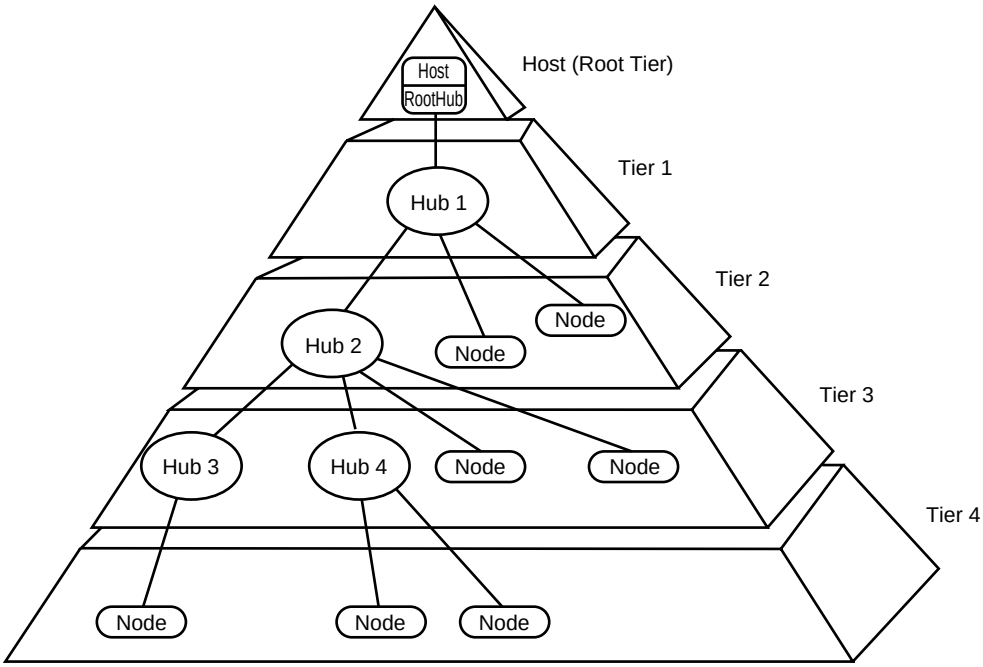
CHAPTER 3 DESCRIPTION OF USB HOST CONTROLLER FUNCTIONS

This chapter provides an overview of the USB, the operations of the host controller, and the structure of the interface data that is used. For details, see the **Open Host Controller Interface Specification Release 1.0** and **OpenHCI Legacy Support Interface Specification Release Version 1.01**.

3.1 Overview of USB

The USB (Universal Serial Bus) is a type of serial bus that enables transfer of data between a host computer and various types of peripheral devices. The USB host has point-to-point connections with USB devices via a tiered star topology, in which each star contains a device called a hub. Figure 3-1 shows a USB bus topology. The USB enables connection of up to 127 devices via this tiered star topology. In addition, devices can be connected or disconnected while the system is still operating.

Figure 3-1. Bus Topology



USB signals are transferred point-to-point as differential signals using two signal lines. There are two signal trace modes: full speed mode (12 Mbs) and low speed mode (1.5 Mbs). Low speed mode is used in low-cost devices such as mouse devices that do not require much EMI protection. As shown in Figures 3-2 and 3-3, the mode is set as full speed or low speed based on the position of the terminating resistors connected to both ends of the USB cable. Terminating resistors are also used at each port to detect when devices are being connected or disconnected.

Figure 3-2. Full Speed Device Cable and Resistor Connections

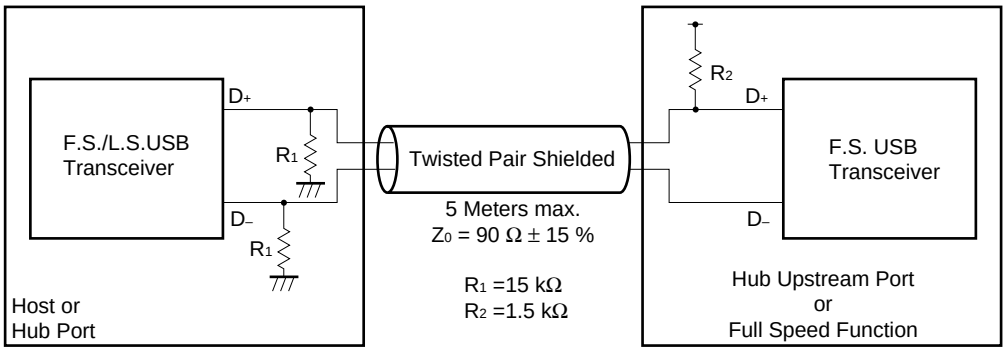
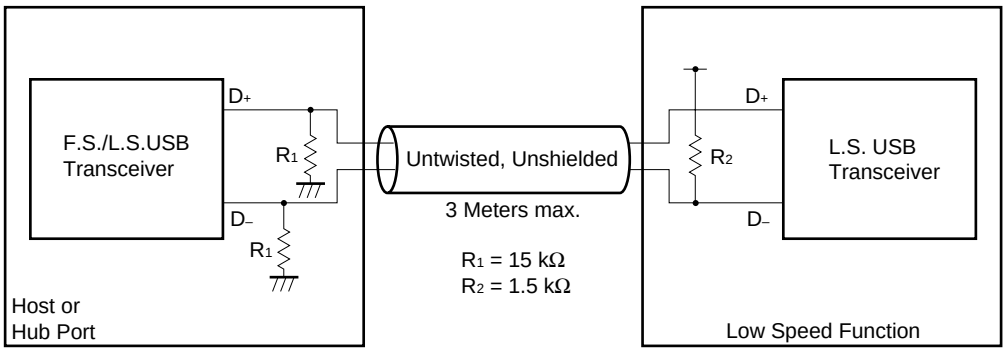


Figure 3-3. Low Speed Device Cable and Resistor Connections



The host schedules and manages data transfers. Consequently, transfers must always be started by the host, and all transfers are performed using up to three packets (token, data, and handshake packets). The token packet sends USB devices information on the processing direction, type of transaction, address, endpoint, etc. The USB device decodes the address field and determines whether or not it has been accessed. The data packet contains the data that is sent in the direction (from host to device or from device to host) that is specified by the token packet. The handshake packet is returned to the source of the transfer to indicate whether or not the transfer was successful. The following four types of transfers occur between USB hosts and USB devices.

- Interrupt transfer — This is a small data transfer which is used to send information from a USB device to client software. The HCD (Host Controller Driver) sends a token packet to a device within the period required by the device, after which the USB data transfer is executed.

- Isochronous transfer — This is a periodic data transfer that uses a constant data transfer rate.

- Control transfer — This is a non-periodic data transfer that is used to send information about configuration, commands, and status between the client software and a USB device.

- Bulk transfer — This is a non-periodic data transfer that is used to send large amounts of information between the client software and a USB device.

Under OpenHCI, data transfers are divided into two categories: periodic and non-periodic. Periodic transfers, which are executed within a specified period, are further divided into the interrupt and isochronous transfer types. Non-periodic transfers, which are not executed periodically, are divided into control and bulk transfer types.

To implement the following types of operations, a device called a USB host controller and software called the USB HCD must both be installed on the host computer. OpenHCI is the specifications that apply to the relation between the host controller and the HCD software. This device complies with the **Open HCI Specification Release 1.0** and **OpenHCI Legacy Support Interface Specification Release Version 1.01**.

3.2 Host Controller's Communication Method

The host controller (HC) and the host controller driver (HCD) communicate via the following two paths.

- Operational registers
- Host Controller Communications Area (HCCA)

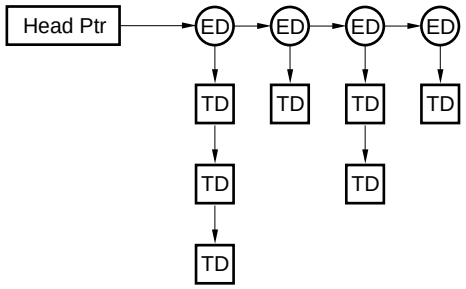
In communication that uses the operational registers which are built into the HC, the HC is the PCI target device. The operational registers are a set of registers that include control bits, status bits, list pointers, etc. They also include pointers that indicate the position of the HCCA (Host Controller Communications Area) within system memory. The HC becomes the PCI bus master for communications that are executed via the HCCA. The HCCA is a 256-byte system memory area that contains head pointers to the interrupt ED list, head pointers to the Done Queue, and frame-related status information. The software uses this system memory to directly control the HC's functions without reading from the HC, as long as operation conditions are normal (i.e., there are no errors). These two paths are used for handling HC control tasks and USB data transfer results.

The HCD executes communication between the HC and USB devices, based on the enqueued ED (Endpoint Descriptor) and TD (Transfer Descriptor). An ED contains information (maximum packet size, endpoint address, endpoint speed and data flow direction) that the HC requires to communicate with the endpoint, and the ED can also be used as the TD queue's anchor. The HCD generates EDs and assigns them to the various endpoints, when are then listed and linked.

A TD contains information (data toggle information, buffer positions in system memory, and complete status code) that is required for the data packet to be sent. Each TD also contains information (data buffer size ranging from 0 to 8192 bytes, with a maximum of 1024-byte transfer per data packet) that is related to at least one data packet. Enqueued TDs are serviced in FIFO order. The TD queue is linked with a certain endpoint's ED and the TDs are linked with the TD queue. The HCD generates data from this structure and passes the data to the HC for processing.

Figure 3-4 shows the relation between EDs and TDs.

Figure 3-4. Relation between EDs and TDs



ED lists are categorized into four types: bulk, control, interrupt, and isochronous. Three types of head pointers of ED list are held (one for each of the above types except isochronous). The isochronous ED list is simply linked following the interrupt ED. The head pointers to the bulk and control ED lists are held in the operational registers, while the head pointers to the interrupt ED list are held in the HCCA. There are 32 interrupt head pointers, and the head pointer that is used by a frame is determined based on the usage of the frame counter's low-order 5 bits (indicating the addresses of the 32 types). The interrupt ED list structure is a tree structure, as is shown in Figure 3-5, in which the execution interval is determined according to the depth of the points where several paths intersect. In other words, interrupt EDs that are linked to the root of the tree structure are allocated and executed at a rate of 1 ms per ED.

Figure 3-5. Interrupt ED List

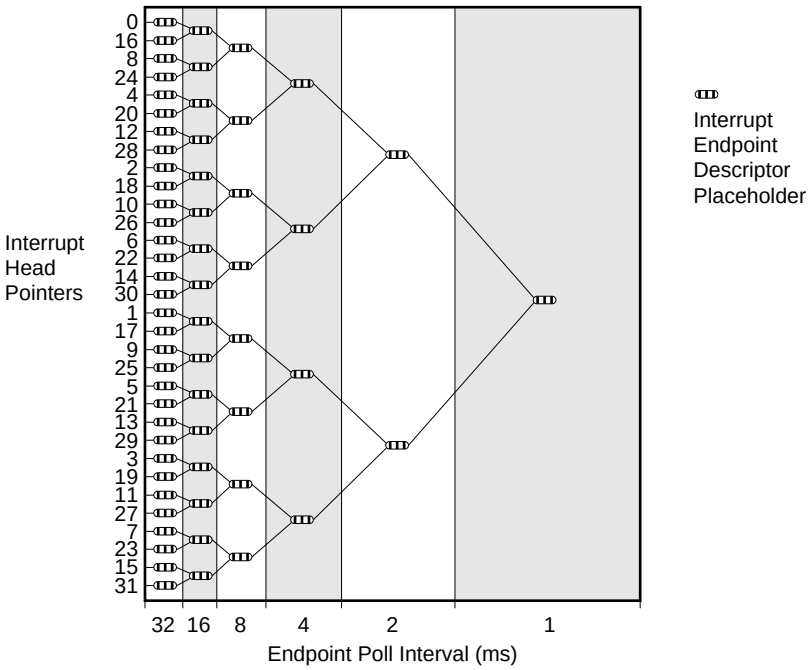
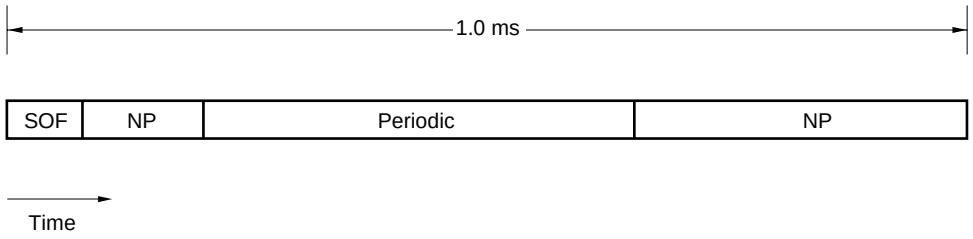


Figure 3-6 shows how the OpenHCI's bandwidth is allocated. The HC selects the list to be serviced based on a prioritization algorithm. Control and bulk lists take priority from the start of the frame to the point where HcFmRemaining becomes HcPeriodicStart.

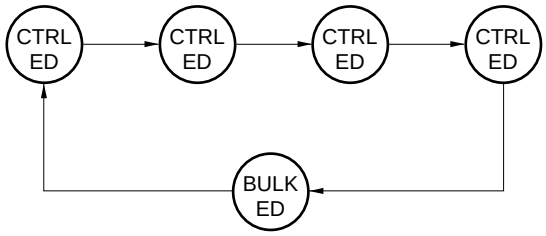
When HcFmRemaining becomes HcPeriodicStart, periodic list servicing takes priority. The priority of periodic list servicing is higher than that of control or bulk servicing up until the point where periodic list servicing is completed or the frame period is completed. After periodic list servicing is completed, control or bulk list servicing is resumed.

Figure 3-6. Allocation of Bandwidth



Interrupt/isochronous list servicing begins with servicing the interrupt ED head pointer that is serviced for the current frame. Since isochronous lists are attached after interrupt lists, interrupt lists must have a higher priority than isochronous lists. Bulk and control list servicing resumes at the point in each list where servicing was interrupted. When servicing reaches the end of the list, a value is loaded from the head pointer and servicing continues. The control endpoint is given access privileges that are at least equivalent to those of the bulk endpoint, and this service ratio is determined by ControlBulkServiceRatio in HcControl. Figure 3-7 shows an example where the control/bulk service ratio is 4:1. When control and bulk take priority, the HC executes ED servicing of each list according to the ControlBulkServiceRatio.

Figure 3-7. When Control/Bulk Service Ratio Is 4:1



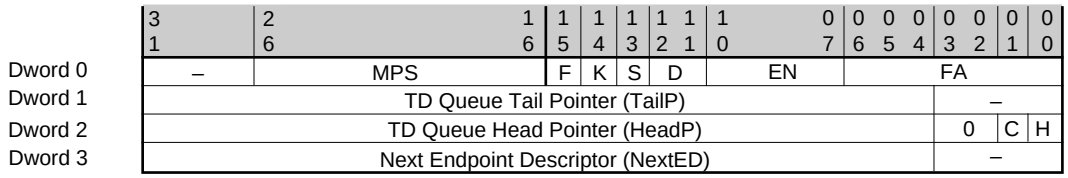
This control/bulk service ratio is retained over several frames. As soon as the HC services the data packet for one of the TDs included in an ED, it begins servicing the next ED.

3.3 Endpoint Descriptor

An ED is always allocated in 16-byte units to system memory. When the ED list is referenced, if it contains a TD that is linked to an ED, the HC executes the transfer specified by that TD. If the HCD must change the head pointer (HeadP) value, list servicing for all EDs that have the same transfer type as the ED to be deleted must be rendered invalid so as to prevent the HC from accessing the EDs. Therefore, the HCD sets a Skip bit.

3.3.1 Endpoint descriptor format

Figure 3-8. Endpoint Descriptor Format



3.3.2 Endpoint descriptor field definitions

Table 3-1. Description of Endpoint Descriptors

<table>
<tr><th>Name</th><th>HC Access</th><th>Description</th></tr>
<tr><td>FA</td><td>R</td><td>Function Address
USB address of function that includes the endpoint that is controlled by this ED</td></tr>
<tr><td>EN</td><td>R</td><td>Endpoint Number
Endpoint address in function</td></tr>
<tr><td>D</td><td>R</td><td>Direction
Indicates the data flow direction (IN or OUT). If neither IN nor OUT are specified, the transfer direction is defined by the TD's PID (Packet ID) field.
<table>
<tr><th>Code</th><th>Direction</th></tr>
<tr><td>00b</td><td>Get direction From TD</td></tr>
<tr><td>01b</td><td>OUT</td></tr>
<tr><td>10b</td><td>IN</td></tr>
<tr><td>11b</td><td>Get direction From TD</td></tr>
</table></td></tr>
<tr><td>S</td><td>R</td><td>Speed
This indicates the endpoint's speed.
• full-speed (S = 0)
• low-speed (S = 1)</td></tr>
<tr><td>K</td><td>R</td><td>Skip
When this bit is set, the HC proceeds to the next ED without accessing the TD queue or issuing a USB token to the endpoint.</td></tr>
<tr><td>F</td><td>R</td><td>Format
This indicates the format of a TD that is linked to this ED. For control, bulk, or interrupt endpoints, if F = 0, then the General TD format is used. For isochronous endpoints, if F = 1, the Isochronous TD format is used.</td></tr>
<tr><td>MPS</td><td>R</td><td>Maximum Packet Size
This field indicates the maximum number of bytes (1024 bytes) per data packet that can be received from the endpoint or sent to an endpoint. When a write operation (OUT or SETUP) is executed from the HC to the endpoint, the size of the data packet to be sent always becomes either the Maximum Packet Size or the size of the data in the buffer, whichever is smaller. When a read operation (IN) is executed from the endpoint to the HC, the data packet size is determined according to the endpoint.</td></tr>
<tr><td>TailP</td><td>R</td><td>TD Queue Tail Pointer
When TailP and HeadP have the same value, the list does not contain any TDs that can be serviced by the HC. When the TailP and HeadP values are different, the list contains TDs.</td></tr>
<tr><td>H</td><td>R/W</td><td>Halted
This bit is set by the HC to indicate when servicing of the endpoint TD queue has been suspended due to a normal TD servicing error.</td></tr>
<tr><td>C</td><td>R/W</td><td>toggle Carry
This bit is the data toggle carry bit. When a TD is retired, the final data toggle value (LSb in the data Toggle field) that was used by the retired TD is written. This field cannot be used by isochronous endpoints.</td></tr>
<tr><td>HeadP</td><td>R/W</td><td>TD Queue Head Pointer
This indicates the next TD to be serviced at this endpoint.</td></tr>
<tr><td>NextED</td><td>R</td><td>Next ED
When its value is other than zero, this bit indicates the next ED.</td></tr>
</table>

3.4 Transfer Descriptors

TDs (Transfer Descriptors) are used by the HC to indicate the buffer for the data that is sent to or from an endpoint. TDs are divided into two types: General TDs and Isochronous TDs. General TDs are used by interrupt, control, and bulk endpoints while Isochronous TDs are used for handling isochronous transfers.

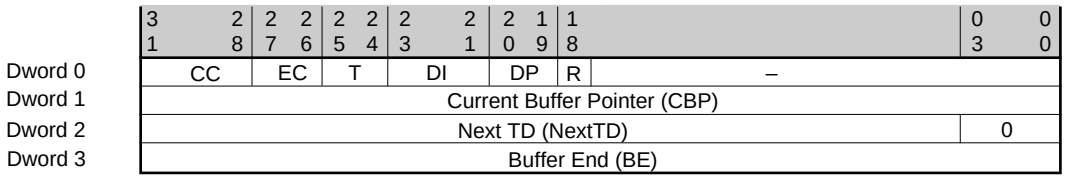
For both General and Isochronous TDs, buffers ranging from 0 bytes to 8,192 bytes can be indicated. Also, the data buffer described by one TD can be divided into two pages. This enables the elimination of various problems, such as problems related to forced physical connection of buffers or transfer of surplus data.

When the HCD appends a TD, the TD indicated by TailP is linked to the new TD, and TailP is then changed to indicate the appended TD. Therefore, the appended TD is always added to the end of the TD queue. The HC services the TD asynchronously in relation to servicing performed by the host processor. Consequently, when it is necessary to switch from the TD queue to something else, the HC's endpoint TD queue servicing must be suspended to avoid problems from occurring due to this switch. Suspension of TD servicing is achieved when the HCD sets the Skip bit in the ED to be deleted.

3.4.1 General transfer descriptor format

General TDs are used for control, bulk, or interrupt transfers, and they must always be allocated in 16-byte units to system memory.

Figure 3-9. General TD Format



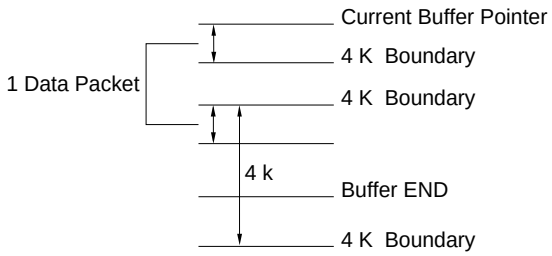
3.4.2 General transfer descriptor field definitions

Table 3-2. Description of General TD

<table>
<tr><th>Name</th><th>HC Access</th><th>Description</th></tr>
<tr><td>R</td><td>R</td><td>buffer Rounding
When this bit's value is “0”, the data buffer defined by the last data packet sent from the endpoint specified by the TD must be a completely full buffer. When its value is “1”, the data buffer defined by the last data packet is not full, even if there are no errors.</td></tr>
<tr><td>DP</td><td>R</td><td>Direction/PID
This indicates the data flow direction and PID used by a token. This field only has significance in relation to the HC when 00b or 11b is set to indicate that the ED's D field has delayed the PID judgment until the TD.
<table>
<tr><th>Code</th><th>PID Type</th><th>Data Direction</th></tr>
<tr><td>00b</td><td>SETUP</td><td>to endpoint</td></tr>
<tr><td>01b</td><td>OUT</td><td>to endpoint</td></tr>
<tr><td>10b</td><td>IN</td><td>From endpoint</td></tr>
<tr><td>11b</td><td>Reserved</td><td></td></tr>
</table></td></tr>
<tr><td>DI</td><td>R</td><td>Delay Interrupt
This indicates the time until a interrupt occurs as notification of completed TD servicing. When the TD has been completed, the HC delays the interrupt event until the frame indicated by this bit. When this bit's value is 111b, interrupts related to completion of this TD do not occur.</td></tr>
<tr><td>T</td><td>R/W</td><td>Data Toggle
This field is used to generate a comparison or occurrence of data PID values (DATA0 or DATA1). This field is updated after each successful transfer of a data packet. When the data Toggle field's Msb is “0”, the data Toggle field's Lsb, which was acquired from the ED's toggle Carry bit, is ignored. When data Toggle field's Msb is “1”, the data Toggle field's LSb indicates the data toggle.</td></tr>
<tr><td>EC</td><td>R/W</td><td>Error Count
This field is incremented after each transmission error. If an error occurs after the Error Count has reached “2”, the type of error is written to the Condition Code field and is transferred to the done queue. If servicing ends without any errors, the Error Count is reset to “0”.</td></tr>
<tr><td>CC</td><td>R/W</td><td>Condition Code
This field is updated each time processing is executed, regardless of whether or not the processing was successful. If it was successful, this field is set as NoError. If unsuccessful, it is set according to the type of error.</td></tr>
<tr><td>CBP</td><td>R/W</td><td>Current Buffer Pointer
This includes the next physical address in memory that will be accessed by a transfer from or to an endpoint.
A “0” value indicates either that the data packet has zero length or that all bytes have been transferred.</td></tr>
<tr><td>NextTD</td><td>R/W</td><td>Next TD
This specifies the next TD in the TD list linked to the endpoint.</td></tr>
<tr><td>BE</td><td>R</td><td>Buffer End
This indicates the physical address of the last byte in the TD's buffer.</td></tr>
</table>

The General TD's Current Buffer Pointer indicates the data buffer address used for a data packet transfer to or from an endpoint. If the transfer is completed without the occurrence of any kind of error, the HC advances the Current Buffer Pointer by exactly the number of transferred bytes. If the buffer address indicated by the Current Buffer Pointer exceeds the 4-K boundary during a data packet transfer, the high-order 20 bits of the Buffer End field is copied to the working value from the Current Buffer Pointer. The next buffer address becomes byte 0 in the same 4-K page space that is used when the final byte is retained.

Figure 3-10. Current Buffer Pointer/Buffer End and 4-K Boundary



3.4.3 Isochronous transfer descriptor format

Isochronous TDs are used only by isochronous endpoints. All TDs linked to the ED must use this format when F = 1. This TD is allocated to system memory in 32-byte units.

Figure 3-11. Isochronous TD Format

	31–28	27	26–24	23–21	20–16	15–12	11–5	4–0
Dword 0	CC	–	FC	DI	–	SF		
Dword 1	Buffer Page 0 (BP0)						–	
Dword 2	NextTD							0
Dword 3	Buffer End (BE)							
Dword 4	Offset1/PSW1					Offset0/PSW0		
Dword 5	Offset3/PSW3					Offset2/PSW2		
Dword 6	Offset5/PSW5					Offset4/PSW4		
Dword 7	Offset7/PSW7					Offset6/PSW6		

3.4.4 Isochronous transfer descriptor field definitions

Table 3-3. Description of Isochronous TD

Name	HC Access	Description
SF	R	Starting Frame This includes the low-order 16 bits of the number of frames sent by the Isochronous TD's first data packet.
DI	R	Delay Interrupt This indicates the time until a interrupt occurs following completion of Isochronous TD servicing.
FC	R	Frame Count This is the number of data packets indicated by the Isochronous TD. When Frame Count = 0, one data packet is included and when Frame Count = 7, eight data packets are included.
CC	R/W	Condition Code This field includes a completion code when an Isochronous TD has been transferred to the Done Queue.
BP0	R	Buffer Page 0 This is the physical page number of the first byte in the data buffer used by the Isochronous TD.
NextTD	R/W	Next TD This indicates the next Isochronous TD in the Isochronous TD queue linked to an ED.
BE	R	Buffer End This includes the physical address of the buffer's last byte.
OffsetN	R	Offset This is used to determine the size and start address of an isochronous data packet.
PSWN	W	Packet Status Word This includes the size of the completion code and the received isochronous data packet.

Isochronous TDs have a (Frame Count + 1) frame buffer with a continuous range from 1 to 8. The first data packet is sent when the low-order 16 bits of HcFmNumber matches the Isochronous TD's Starting Frame value. If the buffer address exceeds the 4-K boundary during a data packet transfer, the high-order 20 bits of the Buffer End field is used as the physical address of the next page. Consequently, the next buffer address becomes byte 0 in the same 4-K page space that is used when the final byte is retained.

3.5 Host Controller Communications Area

The HCCA (Host Controller Communications Area) is a 256-byte area in system memory that is used by the system software for sending and receiving control/status information to and from the HC. The system software always writes the address of the area to the HC's HcHCCA field.

3.5.1 Host controller communications area format

Table 3-4. Description of Host Controller Communications Area

Offset	Size (bytes)	Name	R/W	Description
0	128	HccaInterruptTable	R	This 32-Dword entry table is a pointer to ED interrupt lists.
0×80	2	HccaFrameNumber	W	This includes the current frame number. This value is updated by the HC before periodic list servicing of the frame begins.
0×82	2	HccaPad1	W	When the HC updates the HccaFrameNumber value, the HC sets "0" to this word.
0×84	4	HccaDoneHead	W	When the HC reaches the end of a frame and a decremented value of "0" is shown as the Delay Interrupt value, the HC writes the current HcDoneHead value to this field. At this point, interrupts occur as valid interrupts. The HC does not write again until the software clears the WD bit in the HcInterruptStatus register. If this field has a value of "0", interrupts can occur for reasons other than updating of HccaDoneHead, and the HcInterruptStatus register must be accessed to determine the cause of the interrupt. If this field's value is not "0", the interrupt is due to updating of the Done Queue. If this field's LSb is not "0", another interrupt event has occurred. The HcInterruptStatus field must be checked to determine the cause of that interrupt.
0×88	116	reserved	R/W	This field is reserved for use by the HC.

3.5.2 Host controller communications area description

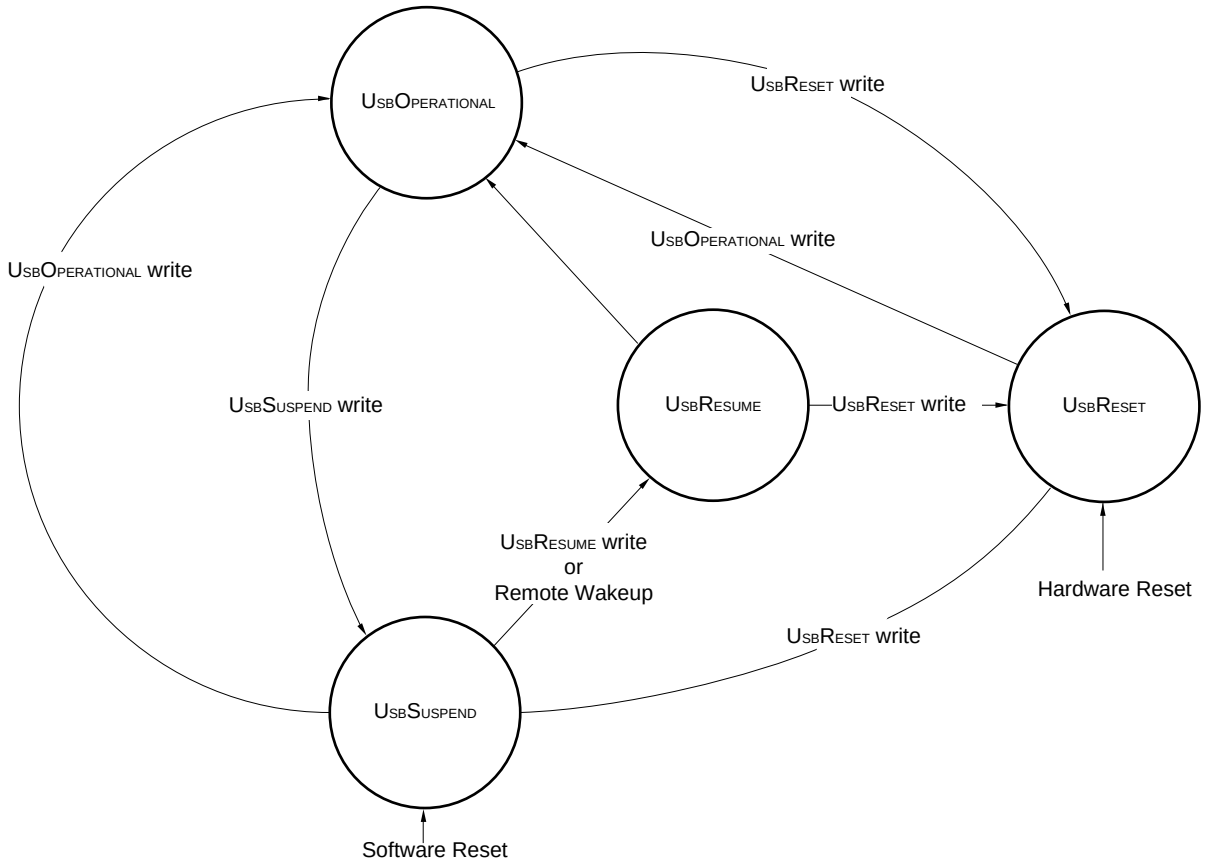
HccaInterruptTable is a 32-Dword entry table which functions as a pointer to the ED list's various interrupt lists. The more of these lists that an ED is linked to, the higher the execution rate. The execution rate is 32 ms for an ED that is in only one list, but it is 6 ms for an ED that is in two lists. An ED that is linked to all 32 lists is executed at a rate of once per frame. The last entry in each of the 32 interrupt lists must specify an isochronous list.

After an SOF (Start Of Frame) token is sent, the HC overwrites HccaFrameNumber using the FrameNumber value from HcFmNumber before it starting reading the ED to be serviced in a new frame.

3.6 HC Mode Changes

HostControllerFunctionalState indicates which of the four states (modes) the HC is in: UsbOperational, UsbReset, UsbSuspend, and UsbResume. The HCD can change USB modes only as shown in Figure 3-12 and the HC can execute only one change: from UsbSuspend to UsbResume during a remote wakeup event.

Figure 3-12. HC Mode Changes



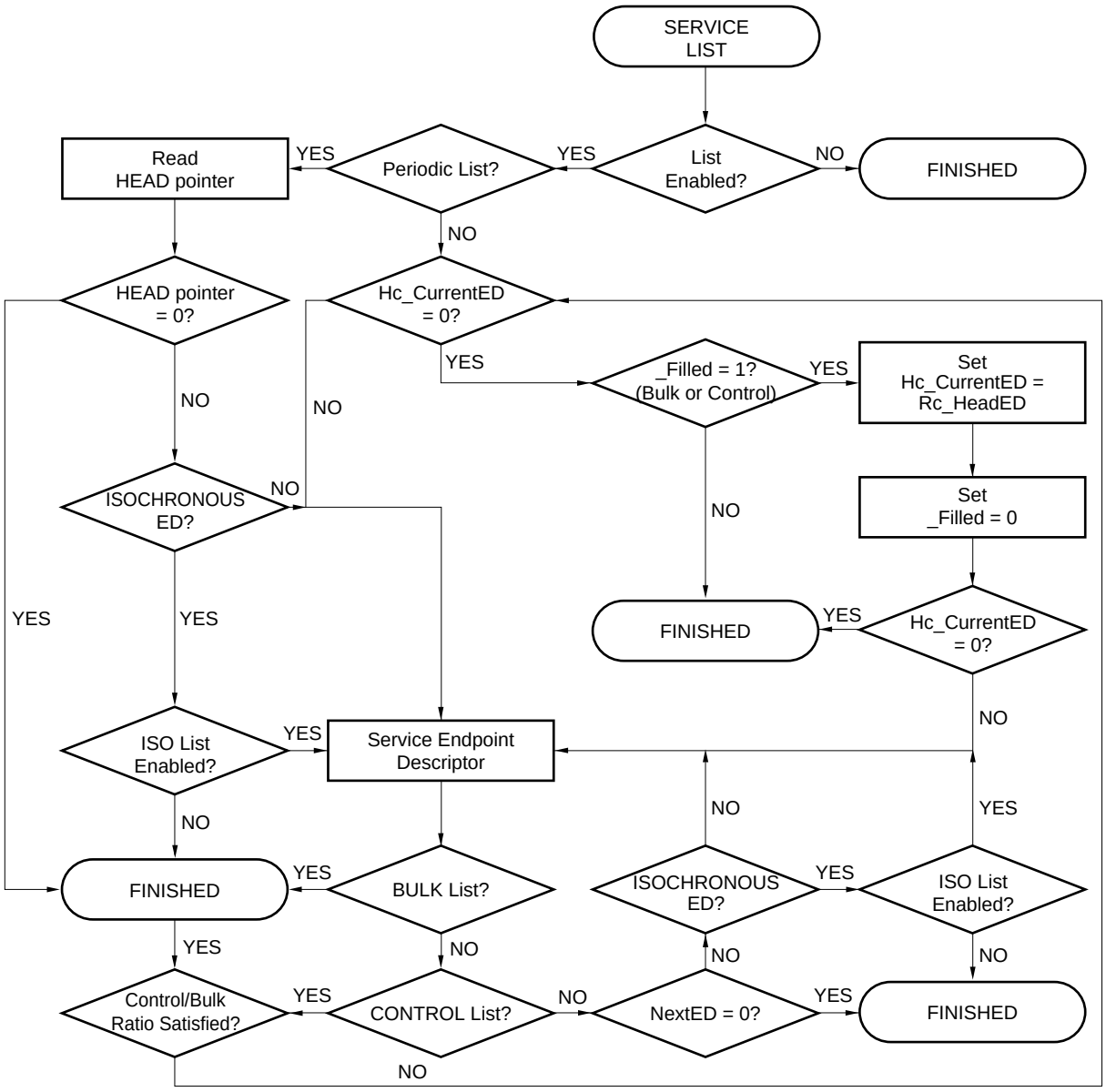
When in UsbOperational mode, the HC services lists and issues an SOF token. FrameInterval is loaded to FrameRemaining at the same time as the mode is being changed to UsbOperational.

The first SOF token to be sent after changing to UsbOperational mode is sent at the frame boundary when changing from FrameRemaining (value: “0”) to FrameInterval. At UsbReset, the HC forcibly sends a reset signal to the bus. After a hardware reset, the HC always changes to UsbReset mode. When in UsbSuspend mode, the USB is temporarily stopped. When in this mode, the HC monitors the USB wakeup operations. The HC can forcibly change to UsbResume mode according to the remote wakeup condition. This change may conflict with the change to UsbReset mode that is performed by the HCD. When such a conflict has occurred, the HCD’s change to UsbReset mode takes priority. A change to UsbResume mode is not possible during the first 5 ms following a change to UsbSuspend mode. When in UsbResume mode, the HC forcibly sends a resume signal to the bus. While in UsbResume mode, the root hub always passes a USB resume signal to downstream ports. The change to UsbResume is started by a remote wakeup signal sent by the HCD or the root hub.

3.7 List Service Flow

Figure 3-13 shows a list service flowchart. After the HC determines which list to service, list servicing is executed via this list service flow pattern. Since lists are periodically rendered invalid by the HCD due to ED switching (or other reasons), the HC must first check whether or not the target list is valid by checking each list enable bit in HcControl when servicing the list.

Figure 3-13. List Service Flowchart

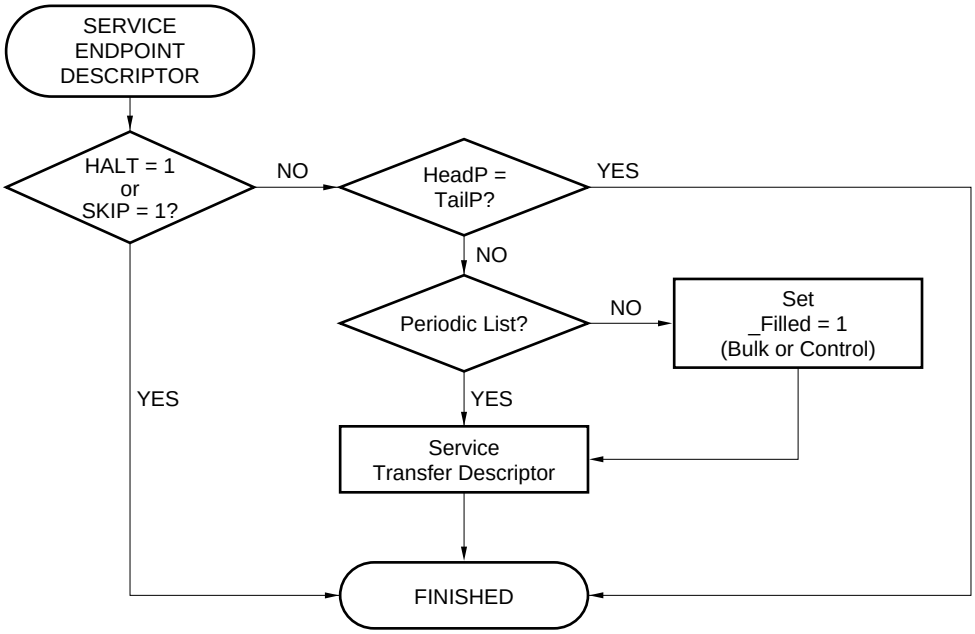


If the checked list is valid, the HC services the list. If it is invalid, the HC skips that list and proceeds to the next list. When a list is valid, the HC checks the position of the first ED for which servicing is requested. During periodic list servicing, if the head pointer value is “0”, it means there are no EDs in the list and the HC proceeds to the next list. By contrast, during non-periodic list servicing, if the “CurrentED” value in each list is “0”, the HC checks each “ListFilled” value. If it finds that the “ListFilled” value has been set to “1”, it means that there is at least one ED in the target list that requires servicing. In such cases, the HC copies the “HeadED” value to “CurrentED” and clears the “Filled” bit to “0”, then services the ED indicated by “CurrentED”. If the HC finds a “0” value when checking “ListFilled”, it proceeds to the next list.

After servicing the ED, if the current list is a periodic list, the HC checks NextED in the just-completed ED then continues servicing the next ED. If it finds that the NextED value is “0”, the HC proceeds to the non-periodic list. For bulk lists, the HC simply proceeds to the next list. For control lists, the next action varies depending on whether or not the number of control EDs indicated by the control/bulk service ratio has been serviced.

Figure 3-14 shows an ED service flowchart.

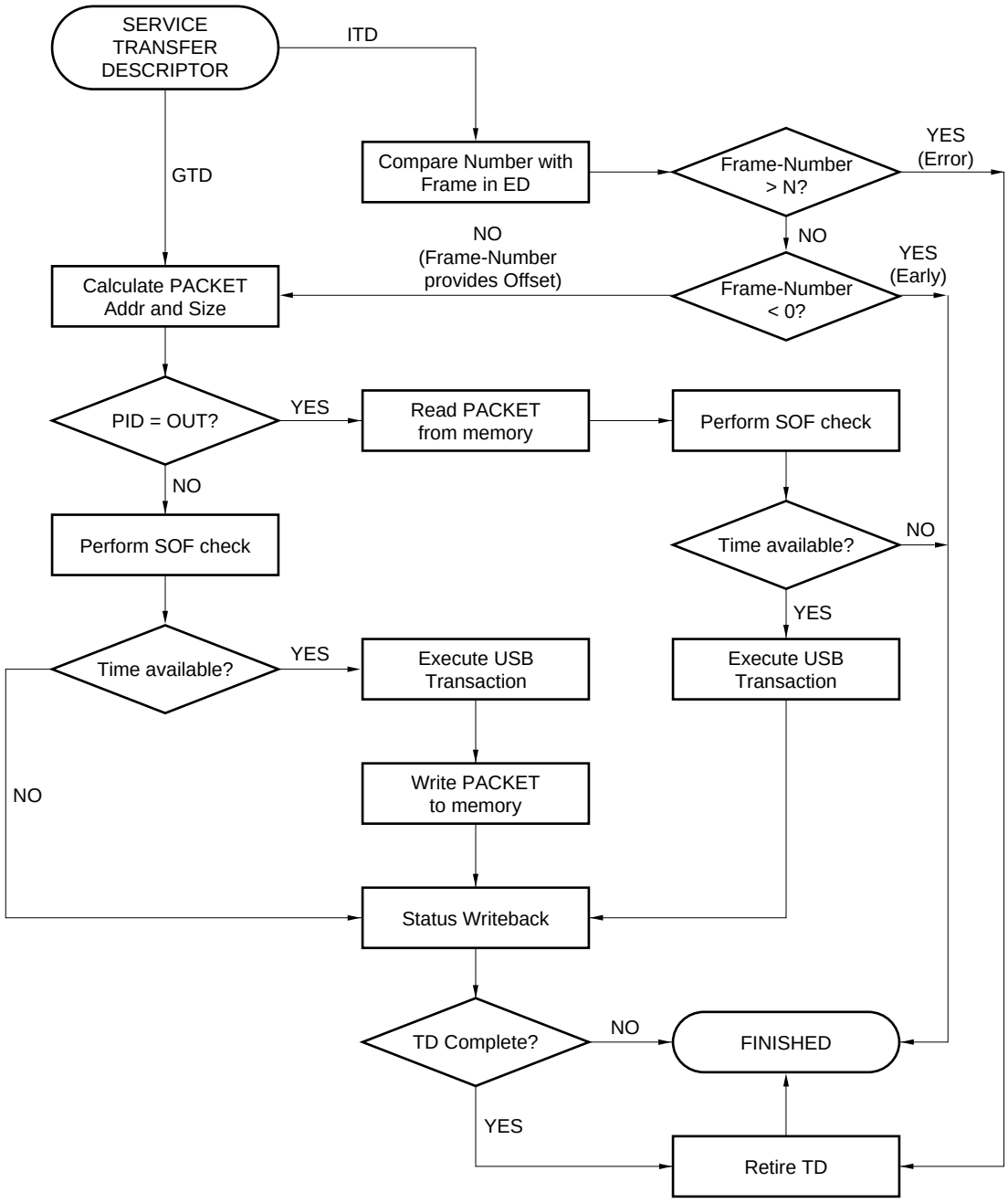
Figure 3-14. ED Service Flowchart



First, the HC reads the ED to be serviced from the system memory via the PCI bus. Next, the HC determines whether or not that ED actually needs to be serviced. If the ED’s Skip bit or Halted bit has a value of “1”, the HC skips the ED and proceeds to the next ED or list. If the HC determines that the ED needs to be serviced, it next determines whether or not there are any TDs that can be handled in a queue. The HC compares the ED’s TailP and HeadP values and, if the values match, it concludes that the list does not include any valid TDs, so it proceeds to the next ED or list. If the TailP and HeadP values differ, the HC services the corresponding TD.

Figure 3-15 shows a TD service flowchart. When the HC services an Isochronous TD, it first calculates the relative frame number to determine whether or not a packet should be sent during the current frame. This relative frame number is used to select Offset [R] and Offset [R+1]. If the relative frame number matches the TD’s FrameCount value, Offset [R+1] (BufferEnd+1) is selected. The data buffer size for each transfer is calculated by subtracting Offset [R] from Offset [R+1], and the address is determined based on Offset [R]. When bit 12 of Offset [R] is “0”, the Isochronous TD’s BufferPage0 is used as the high-order 20 bits of the address. When bit 12 of Offset [R] is “1”, the high-order 20 bits of BufferEnd are used as the high-order 20 bits of the address.

Figure 3-15. TD Service Flowchart



When servicing a General TD, the HC gets the next memory address from CurrentBufferPointer. When data is sent to or from the CurrentBufferPointer address, the data may be too large to fit onto one physical page and may therefore occupy several pages. In such cases, the high-order 20 bits of BufferEnd are used instead of the high-order 20 bits of CurrentBufferPointer as the address's high-order 20 bits. The maximum amount of data that can be transferred between devices is their the ED's MaximumPacketSize value or the remaining buffer size, whichever is smaller.

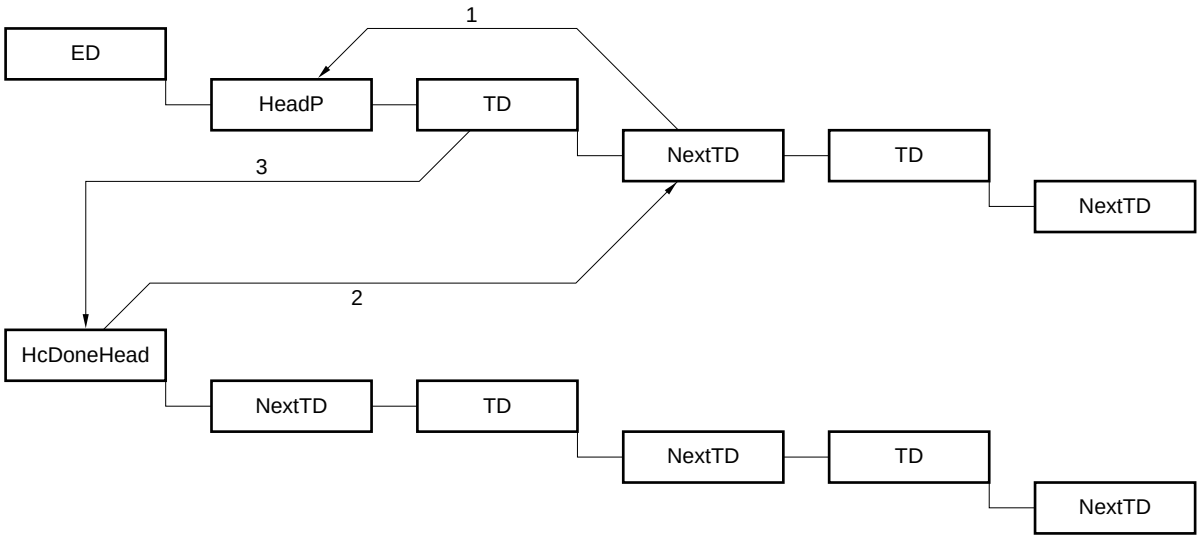
After determining the packet size, the HC must check whether or not it can send the packet before the end of the frame. If the value of the bit time request for the packet to be sent is greater than the frame's remaining bit time value, the packet cannot be sent.

After servicing the General TD, the HC updates four General TD fields: ConditionCode, DataToggle, ErrorCount, and CurrentBufferPointer.

Meanwhile, once Isochronous TD servicing is completed, the HC updates the Offset [R] value to the Packet Status Word.

If the TD is successfully serviced (all data is sent or received) or if an error has occurred, the HC moves the TD to the Done Queue and updates the Done Queue Interrupt Counter. Also, the HC updates the ED to change the values in the HeadP, ToggleCarry, and Halted fields. In order to enqueue the TD into the Done Queue, the HC first copies the current TD's NextTD value to the ED's HeadP field. Next, it writes the HcDoneHead value to the NextTD field of the TD to be enqueued. Finally, it writes the address of the TD to be enqueued to the HcDoneHead field (see Figure 3-16).

Figure 3-16. Done Queue Operations



At this point, the HC uses the TD's final data toggle value to update the ED's ToggleCarry field. If the TD is retired due to an error, the HC also updates the ED's Halted bit.

After the above series of operations, the HC writes the HcDoneHead value to the HCCA and updates the Done Queue Interrupt Counter using the Delay Interrupt value (based on number of issued SOF tokens), which defines the time until an interrupt is generated. However, this counter value is not updated if it is already greater than the Delay Interrupt value of TD.

The Done Queue Interrupt Counter is decremented after each SOF token, and when the counter value reaches "0", the HC writes the current HcDoneHead value to HccaDoneHead immediately at the boundary of the next frame.

After the HcDoneHead value has been written to the HCCA, the HC resets the HcDoneHead value to "0" and sets "1" to the WritebackDoneHead field in HcInterruptStatus, which triggers an interrupt. In this manner, the Done Queue is transferred from the HC to the HCD via the HCCA. The HCD services the Done Queue and supplies notification of completion to the software that requested the transfer.

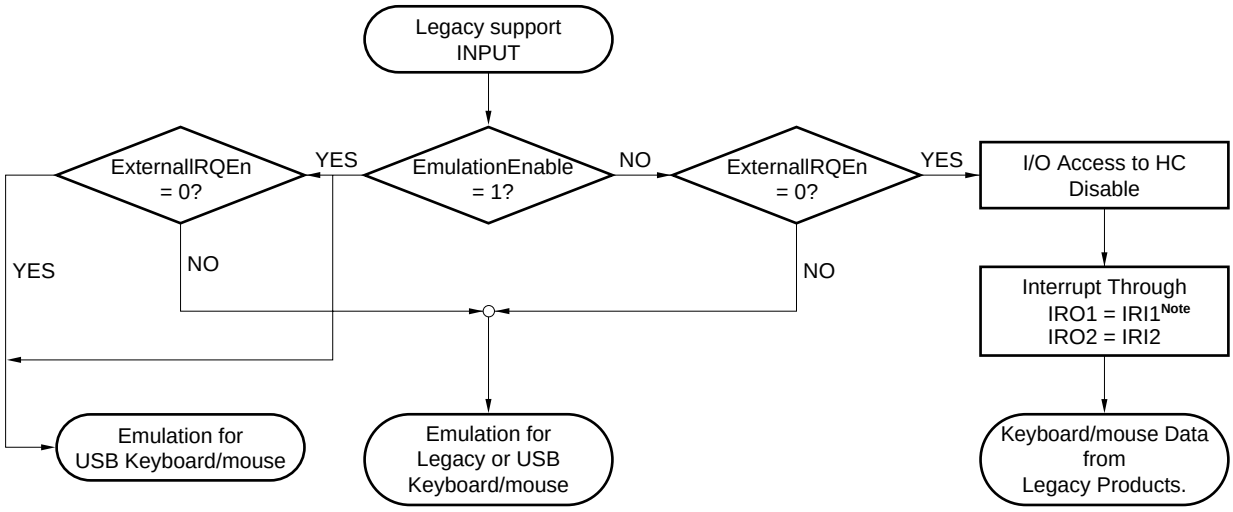
While WritebackDoneHead is being set, the HC does not write the HcDoneHead value to the HCCA. If another Done Queue has been set up to be received from the HC, WritebackDoneHead is cleared by the HCD.

3.8 Legacy Operations

This section describes legacy functions. Legacy functions are provided to directly support the software belonging to an older ("legacy") type of keyboard or mouse device by enabling data from USB keyboard or mouse devices to operate via a legacy keyboard or mouse device interface. These legacy functions are valid when the LEGC pin and AT pin are both clamped to "H". Operations are defined for three conditions: when all connected keyboard/mouse devices are legacy devices, when all are USB devices, and when one or more of each type of device is connected.

Figure 3-17 shows an operational flowchart of input-related legacy functions. When the legacy functions are valid (enabled), the HC first checks HceControl's EmulationEnable and ExternalIRQEn fields. If EmulationEnable has been set to "1", connected USB keyboard or mouse devices are emulated to operate like legacy keyboard or mouse devices (only USB keyboard or mouse devices are valid). If ExternalIRQEn has been set to "1", connected USB keyboard or mouse devices are emulated to operate like legacy keyboard or mouse devices, and compatibility of legacy keyboard/mouse operations is maintained (both USB and legacy keyboard or mouse devices are used).

Figure 3-17. Input-related Legacy Operation Flowchart

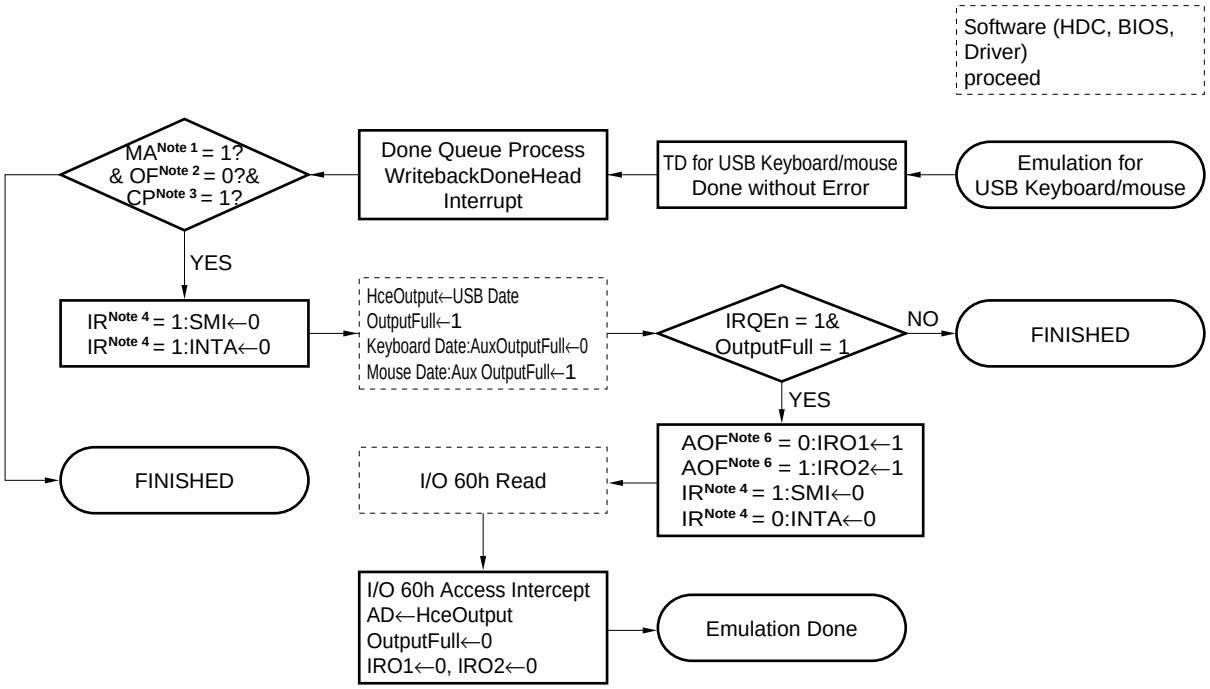


Note Even if IRI1 is ON, IRQ1Active remains at "L". Similarly, even if IRI2 is ON, IRQ12Active remains at "L".

When "0" is the value of both EmulationEnable and ExternalIRQEn, only legacy keyboard or mouse devices are valid, which means that IRQ1 (keyboard interrupt) and IRQ12 (mouse interrupt) are sent from the keyboard controller to the system directly via the HC. The HC does not receive I/O access (60h/64h), which is direct access to the keyboard controller, and does not perform any special processing.

Figure 3-18 shows an input emulation flowchart for USB keyboard or mouse devices. The HC always performs interrupt list service for each frame. When the transfer that is performed according to the TD is completed, the TD is linked to the Done Queue and a write operation to HccaDoneHead and the WritebackDoneHead interrupt occur after a specified amount of time (Delay Interrupt). If the correctly transferred data includes USB keyboard or mouse data, the system software sets "1" to CharacterPending in HceControl. The HC checks that Command Reg.'s Memory Access field has been set to "1", HceStatus's OutputFull field has been set to "0", HceStatus's CharacterPending field has been set to "1", and HceStatus's EmulationEnable field has been set to "1", after which an emulation interrupt occurs. The output destination for this interrupt is set via HcControl's InterruptRouting field.

Figure 3-18. Input Emulation Flowchart for USB Keyboard/Mouse



Notes 1. MA = PCI Command Reg. Memory Access

2. OF = OutputFull

3. CP = CharacterPending (set by system software)

4. IR = InterruptRouting

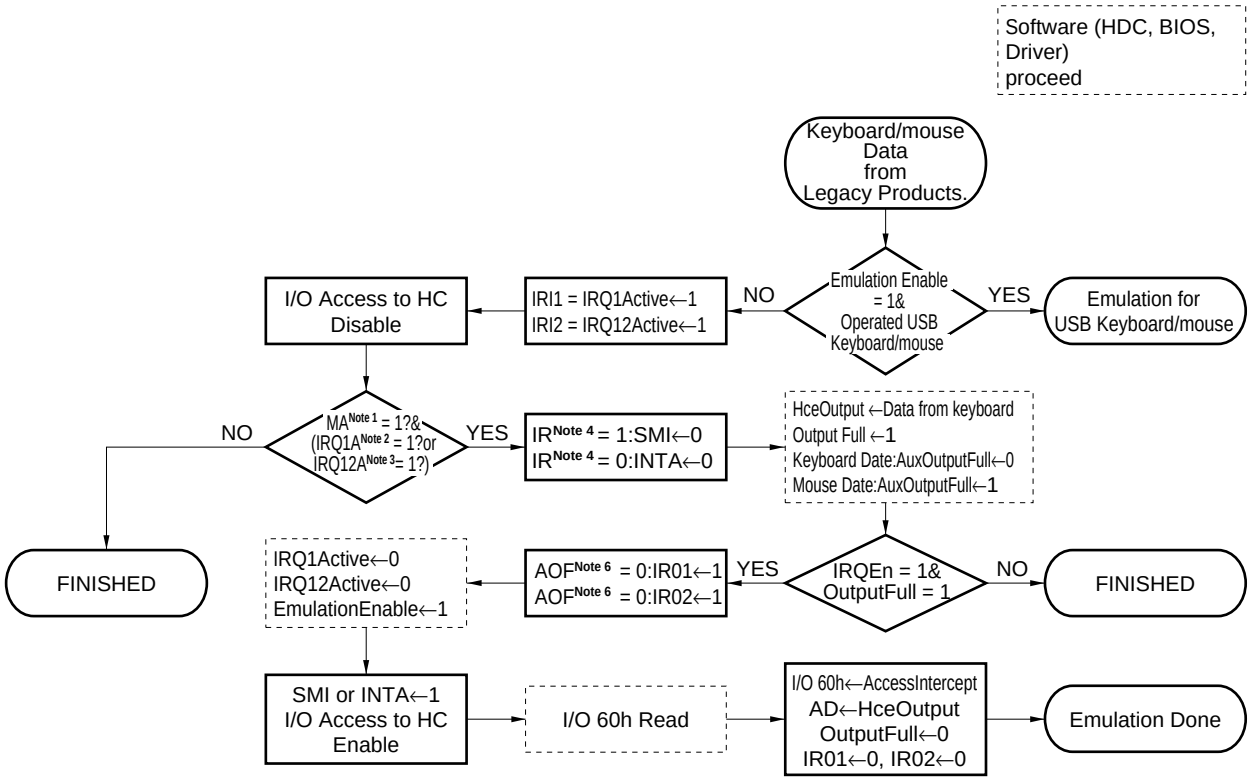
5. The WritebackDoneHead interrupt is generated at the same time as the emulation interrupt. The system software acknowledges these interrupts and must clear both of them.

6. AOF = AuxOutputFull

When the system software detects the emulation interrupt, the transferred data is written to HceOutput Reg. (108h) via a memory write operation and “1” is set to the OutputFull field. In addition, “0” is set to HceStatus’s AuxOutputFull field if the data is keyboard data and “1” is set to that field if the data is mouse data. At that point, the system software performs operations such as deleting the contents of the TD’s DoneQueue field or canceling interrupts. This setting asserts IRO1 (IRQ1) if for keyboard data or IRO2 (IRQ12) if for mouse data. In cases where assertion of the IRO1 or IRO2 signal causes the software to perform I/O read access to address 60h, the HC intercepts this access and outputs the HceOutput value to the data bus instead of the keyboard controller. Next, “0” is set to the OutputFull field, and IRO1 or IRO2 is deasserted. By performing this series of operations, the software is able to handle USB keyboard/mouse data in the same way as legacy keyboard/mouse data.

Figure 3-19 shows a flowchart for when input devices include a combination of USB keyboard or mouse devices and legacy keyboard or mouse devices. In this case, processing of the USB keyboard/mouse data uses the same flow as was described above. Meanwhile, legacy keyboard/mouse data is passed to the system software in the same way as during emulation processing of USB keyboard/mouse data. When “1” has been set to ExternalIRQEn, if an interrupt signal from the keyboard controller is detected, “1” is set to either the IRQ1Active bit or the IRQ12Active bit in HceControl in response to the interrupt signal. When “1” is set to either of these bits, the HC no longer acknowledges I/O access. Next, the HC checks that the Memory Access bit setting is “1”, the IRQ1Active or IRQ12Active bit setting is “1”, and the ExternalIRQEn bit setting is also “1”, then generates an emulation interrupt. At the point when the system software detects the emulation interrupt, data is read from the keyboard controller via 60h I/O access and is written to HceOutput Reg. (108h) via a memory write operation, then “1” is set to the OutputFull field. At the point when the system software confirms assertion of IRO1 (IRQ1) or IRO2 (IRQ12), the HC clears IRQ1Active or IRQ12Active to “0” so that it is again able to respond to I/O access. After this change, assertion of the IRO1 or IRO2 signal enables I/O read access to 60h. When I/O read access to 60h in software is performed, the HC intercepts this access and outputs the HceOutput value to the data bus instead of the keyboard controller, and it sets “0” to OutputFull and deasserts IRO1 or IRO2. During emulation, interrupts from the keyboard controller are masked and are not received.

Figure 3-19. Combination of USB Keyboard/Mouse and Legacy Keyboard/Mouse (Input Emulation)



Notes 1. MA = PCI Command Reg. Memory Access

2. IRQ1A = IRQ1Active

3. IRQ12A = IRQ12Active

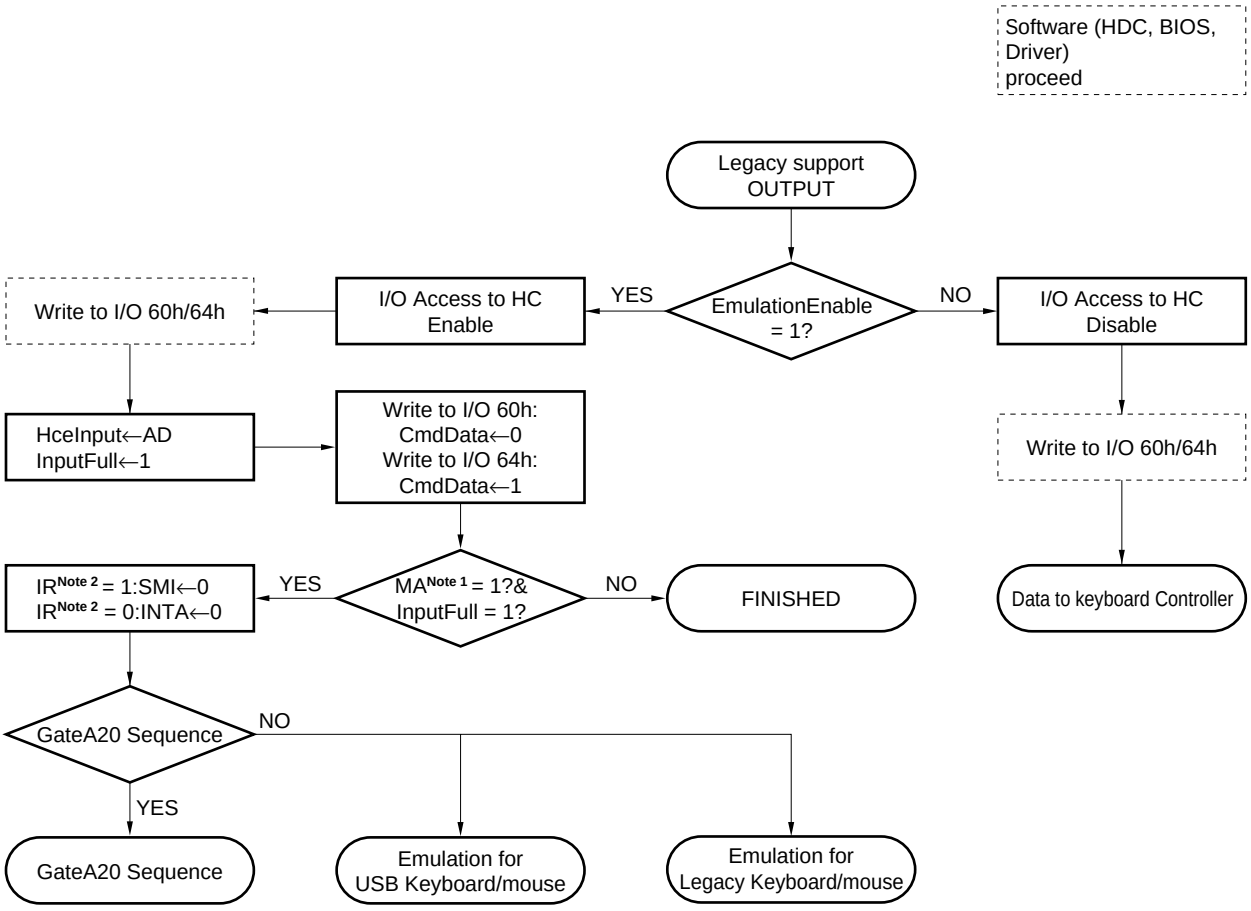
4. IR = InterruptRouting

5. An emulation interrupt is set independently of EmulationEnable.

6. AOF = AuxOutputFull

Figure 3-20 shows a legacy operation flowchart for output operations. When EmulationEnable is “0”, only legacy keyboard or mouse devices are valid. Consequently, the HC does not receive I/O access and write operations to I/O address 60h/64h are performed directly from the keyboard controller. When EmulationEnable is “1”, the HC intercepts the write operation to I/O address 60h/64h and writes the data to HceInput, then sets “1” to HceStatus’s InputFull field. In addition, it sets “0” to HceStatus’s CmdData field when data is written to 60h, and it sets “1” to that field when data is written to 64h. Once the HC confirms that “1” has been set to MemoryAccess, InputFull, and EmulationEnable, it generates an emulation interrupt. When writing to a USB keyboard or mouse, the system software reads from HceInput upon detecting the emulation interrupt, and then sets “0” to InputFull. Next, the system software generates data in the TD and USB formats, based on the data that was read, and processes this data via ordinary USB operations. Meanwhile, when writing to a legacy keyboard or mouse, the system software not only reads HceInput and sets “0” to InputFull, it also sets “0” to EmulationEnable. Since setting “0” to EmulationEnable means that the HC no longer receives I/O access, writing to I/O address 60h or 64h is performed by writing directly to the keyboard controller. The value of CmdData is checked to determine whether output is to I/O address 60h or 64h. If a GateA20 sequence occurs, it takes priority over the operations described above.

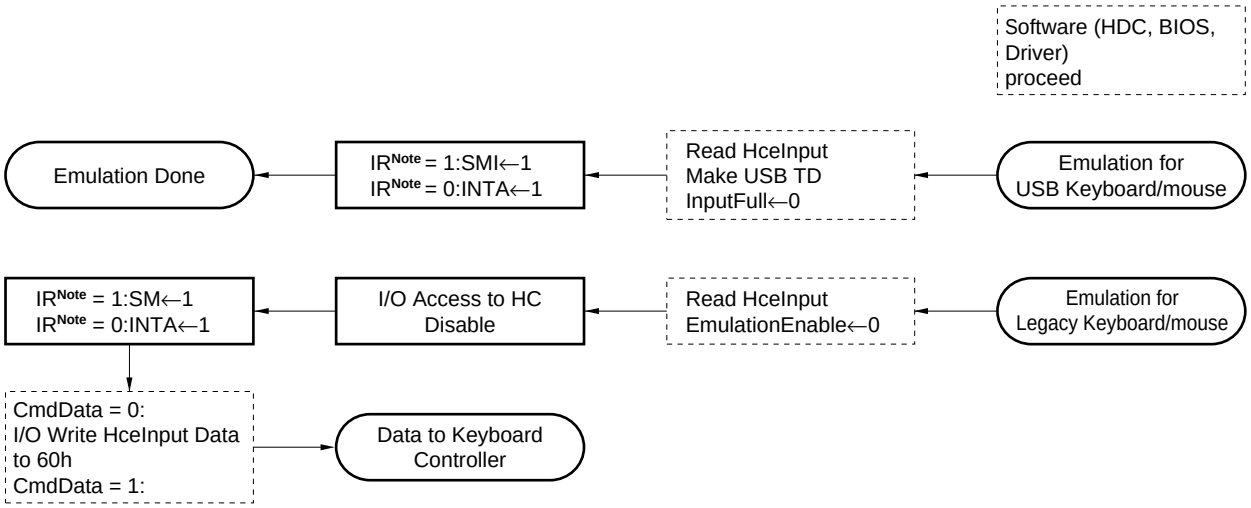
Figure 3-20. Output-related Legacy Operation Flowchart



Notes 1. MA = PCI Command Reg. Memory Access

2. IR = InterruptRouting

Figure 3-21. Distinctions between Legacy and USB



Note IR = InterruptRouting

GateA20 sequences occur frequently in DOS applications, where they mainly set A20 as valid or invalid. To reduce the number of SMIs that occur due to GateA20, the HC generates an SMI (System Management Interrupt) only when the GateA20 status is to be changed by a GateA20 sequence.

Table 3-5 lists operation conditions and HC operations.

Table 3-5. GateA20 Sequences

	Condition			HC	
	GateA20 Sequence	Value Written to I/O (64h)	Value Written to I/O (64h) (bit 1)	GateA20 Sequence	InputFull
1	0	D1h		0 → 1	0
2	0	FFh		0	1
3	0	Except D1h/FFh		0	1
4	1	D1h		1	0
5	1	FFh		1 → 0	0
6	1	Except D1h/FFh		1 → 0	1
7	1		Value does not match A20State	1	1
8	1		Value matches A20State	1	0

The system software first sets the A20State for HceControl. Next, it sets the GateA20 sequence as valid by writing D1h to I/O (64h), which sets GateA20Sequence for HceControl. When GateA20Sequence has been set, any data whose bit 1 value is not A20State is written to I/O port 60h and InputFull is set. At that point, HC confirms that “1” has been set to MemoryAccess, InputFull, and EmulationEnable, after which an interrupt occurs. When the system software detects this interrupt, processing of GateA20 begins.

[MEMO]

CHAPTER 4 POWER MANAGEMENT

4.1 Overview of Power Management

This device supports CLKRUN functions and PCI/USB clock stop functions in order to reduce power consumption. This chapter describes the power management approach and related control methods.

4.2 Bus States and Device States

In this device, power management provides separate control of PCI and USB operations. Therefore, to understand these operations, one must first understand the PCI bus states, USB bus states, and device states.

(1) PCI bus states

B0: PCI CLK = 33 MHz (includes CLKRUN operations)
B1: PCI CLK = Intermittent clock operation mode
B2: PCI CLK = Stop, PCI BUS power on
B3: PCI CLK = Stop, PCI BUS power off

(2) USB bus states

USB_Reset: Bus = Reset, USB system is stopped (except for state transition monitoring)
This state is entered when reset mode is canceled. This state can also be entered based on USB Operational Register settings.

USB_Operational: Bus = Active, USB system is operating normally
This state can be entered based on USB Operational Register settings.

USB_Suspend: Bus = Suspend, USB system is stopped (except for bus state and state transition monitoring)
This state can be entered based on USB Operational Register settings. The state transition can also be caused by S/W_Reset.

USB_Resume: Bus = Resume, USB system is operating normally
This state can be entered based on USB Operational Register settings. The state transition can also be caused by connecting or disconnecting devices or by a Wakeup request from a connected device.

(3) Device states

D0 : Normal operation mode (PCI = B0, USB = RESET, OPERATIONAL, SUSPEND, or RESUME)
The PCI state must be B0, USB state can be any state.

D2 : Device sleep mode (PCI = B0, B1, or B2; USB = RESET, SUSPEND/RESUME)
The PCI state can be normal operation, intermittent operation, or suspended operation, but the CPU can access the HC's configuration space and operational registers only during the normal operation state. This restriction exists in order to maintain synchronous periods between the HC and the HCD. The system software and HCD should be coordinated to provide contrast so as to prevent HC operation faults. While in this mode, if the USB state is SUSPEND, a Wakeup operation occurs if a new device connection or disconnection is detected or if the RESUME state is entered in response to a RESUME signal.

D3 : Device disable mode (PCI clock stop, USB = RESET, or power off)
The PCI state can be normal operation, intermittent operation, or suspended operation, but the CPU can access the HC's configuration space and operational registers only during the normal operation state. This restriction exists in order to maintain synchronous periods between the HC and the HCD. The system software and HCD should be coordinated to provide contrast so as to prevent HC operation faults. Wakeup operations do not occur.

4.3 Transition Conditions for Bus States and Device States

The following conditions must be met for a device state transition to occur.

Table 4-1. Device State Transition Conditions

State Transition	Transition Condition	Transition Request Source
D0 → D2	Register setting specifies USB = USB_RESET or SUSPEND state	System
D0 → D3	Register setting specifies USB = USB_RESET state and device's power is off or a HW_RESET occurs	System
D2 → D0	Register setting	System, USB_Wakeup
D3 → D0	Register setting	System
D2 → D3	Register setting specifies USB = USB_RESET state and device's power is off or a HW_RESET occurs	System

USB state transitions are defined in the USB specifications. The transition conditions are listed below.

Table 4-2. USB State Transition Conditions

State Transition	Transition Condition					
	Operational Register Setting	H/W_Reset	S/W_Reset	Wakeup Request	Attach Detection	Dettach Detection
Operational→Reset	○	○	×	×	×	×
Suspend→Reset	○	○	×	×	×	×
Resume→Reset	○	○	×	×	×	×
Reset→Operational	○	×	×	×	×	×
Operational→Suspend	○	×	○	×	×	×
Suspend→Operational	○	×	×	×	×	×
Suspend→Resume	○	×	×	○	○	○
Resume→Operational	○	×	×	×	×	×
Reset→Suspend	×	×	○	×	×	×
Resume→Suspend	×	×	○	×	×	×

Remark Wakeup: Wakeup request from USB device

The mutual relation between the device and the external (USB or PCI) interface is determined as follows, according to the previously described relations between the PCI bus and the device state as well as the device/USB state transition information.

Table 4-3. Mutual Relation between Device State and PCI or USB

Device State	PCI State	USB State	Source of Request from USB to PCI	Control Output
D0	B0	Operational	Transaction	INTA
		Reset	–	SMI
		Suspend		REQ
		Resume	Wakeup/Attach/Dettach	CRUN
D2	B0	Reset	–	–
		Suspend		
		Resume	Wakeup/Attach/Dettach	WAKE
	B1	Reset	–	–
		Suspend		
		Resume	Wakeup/Attach/Dettach	WAKE
	B2	Reset	–	–
		Suspend		
		Resume	Wakeup/Attach/Dettach	WAKE
D3	B0	Reset	–	–
	B1	Reset	–	–
	B2	Reset	–	–
	B3	Reset	–	–

Remarks 1. The INTA signal operates completely asynchronously in relation to the PCI clock.

2. When the device state is D2, the USB state must be a state other than Operational.

3. When the device state is D3, the USB state must be RESET, the HC must be in power-off state, or an HW_RST must occur.

4.4 Device State Transition Flow

To prevent faults in USB control operations from occurring due a transition between device states, such control operations must follow a predetermined flow during a state transition. Make sure that such transitions comply with the device state transition flow described in Table 4-4 below. Also, make sure that the HCD and System processing comply with the OpenHCI specifications.

Table 4-4. State Control

Device State	USB State	State Transition Control
D0 (PCI = CLKRUN)	Suspend → Resume	Transition is only when RESUME signal is sent from USB Flow A
	Operational (bus master REQ)	Flow B
	Operational (interrupt event)	Flow A
	Operational (write to internal register)	Flow C
	All other transitions	Normal HCD control
D2	Suspend → Resume	Flow D
D3	No transition	None
D0 → D2	All transitions	Flow E
D0 → D3	All transitions	Flow F
D2 → D3	Reset, Suspend	Flow F
D2 → D0	Reset, Suspend	Request from System Flow G USB Wakeup request Flow D
D3 → D0	Reset	Don't care

Flow A

(a) Assert INTA (HC)
(b) Normal clock supply (System)
(c) Interrupt servicing (System)
(d) Deassert INTA (HC)

INTA output is synchronized to a 12-MHz clock and there is a delay of up to 170 ns between clearing of the status register and clearing of INTA.

Flow B

(a) Assert CRUN (only when CLKRUN# is at high level) (HC)
(b) Normal clock supply (System)
(c) Assert REQ (HC)
(d) PCI bus master operation (HC)
(e) Deassert REQ (HC)
(f) Multiple Clock Continues operation using CRUN, when necessary (HC)

The maximum allowable time between assertion of CRUN and assertion of GNT to a device is 7 μs. This is a restriction that applies to REQ for cases where data that includes at least 64 bytes is transferred via an Isochronous Transaction. If more than 7 μs elapses before processing is started, some Isochronous data may be lost during transfer. See the specifications of PCI Mobile Design Guide for CRUN operations.

Flow C

(a) Assert CRUN (only when CLKRUN# is at high level) (HC)
(b) Normal clock supply (System)
(c) Multiple Clock Continues operation using CRUN, when necessary (HC)

The maximum allowable time between assertion of CRUN and reset to normal clock operation is 5 μs. See the specifications of PCI Mobile Design Guide for CRUN operations.

Flow D

(a) Send RESUME signal from USB
(only when HCFS = USB_SUSPEND) (USB)
(b) Assert WAKE and set WakeupStatus (HC)
(c) Reset to WAKEUP processing and normal clock (System)
(d) Clear WakeupStatus (System)
(e) Deassert WAKE (HC)
(f) Set device state to D0 and Wakeup Enable to 0 (System)
(g) Assert INTA (HC)
(h) Interrupt servicing (System)
(i) Deassert INTA (HC)

INTA and WAKE output are synchronized to a 12-MHz clock and there is a delay of up to 170 ns between clearing of the status register and clearing of INTA or WAKE.

Flow E

(a) Set HCFS in HcControl Register to USB_RESET or USB_SUSPEND (HCD)
(b) Set device state to D2 (System)
(c) Set StatusChangeStandby bit (HC)
(d) Set Wakeup Enable to 1 (System)
(e) Enable PCI bus state change (System)

When the PCI bus state changes, the system must wait until the StatusChangeStandby bit in the Power Management Control/Status Register goes high. When activating a wakeup via a resume signal from the USB, the HCFS must be set to USB_SUSPEND.

Flow F

(a) Set HCFS in HcControl Register to USB_RESET (HCD)
(b) Set device state to D3 (System)
(c) Set StatusChangeStandby bit (HC)
(d) Enable PCI bus state change (System)

When the PCI bus state changes, the system must wait until the StatusChangeStandby bit in the Power Management Control/Status Register goes high. Other methods for setting a transition to the D3 state include using power-off or HW_RST. If using HW_RST, make sure that synchronization is maintained between the HCD and the HC. In the case of a transition to D3 using HW_RST, the device does not acknowledge any kind of PCI access. After HW_RST is cleared, the device state is D0.

Flow G

(a) Normal clock supply (System)

(b) Set device state to D0 and Wakeup Enable to 0 (System)

Special device controls are not required when resetting from the D3 device state via system power-off or an HW_RST.

[MEMO]

CHAPTER 5 REGISTER INFORMATION

5.1 PCI Configuration Space

The configuration register is accessed in order to set up hardware resources, device characteristics or operations, etc. in PCI Local Bus. This chapter describes the PCI Configuration Space, which is the address space for the configuration register. For a more detailed description, see the **PCI Local Bus Specification Revision 2.1**.

Table 5-1. PCI Configuration Space

31 24	23 16	15 8	7 0	Offset
Device ID		Vender ID		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
BAR_OHCI Register				10h
I/O Address Register (PC/AT™)				14h
I/O Address Register (PC-98 Series)				18h
Base Address Register				1Ch 20h 24h
Cardbus CIS Pointer				28h
Subsystem ID		Subsystem Vender ID		2Ch
Expansion ROM Base Address				30h
Reserved				34h
Reserved				38h
Max_lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch
Reserved				40h . . DFh
Power Management Control/Status				E0h

Table 5-2. Register Information

Register	Address	bits	Read/ Write	Value (Default)	Comment
Vender ID	00h	15 : 0	R	1033h	NEC's vendor ID
Device ID	02h	15 : 0	R	0035h	This device's device ID
Command	04h	15 : 0	See Table 5-1.		
Status	06h	15 : 0	See Table 5-4.		
Revision ID	08h	7 : 0	R	02h	Version 2.0
Class Code-Base Class	09h	23 : 16	R	0Ch	Serial Bus Controller Device
-Sub_Class		16 : 8	R	03h	USB Device
-Programming Interface		7 : 0	R	10h	Open HCI Host Controller
Cache Line Size	0Ch	7 : 0	R	00h	Cache disabled
Latency Timer	0Dh	7 : 3	R/W	00000b	Time to continuation of bus cycle
		2 : 0	R	000b	
Header Type	0Eh	7 : 0	R	00h	Not a PCI-to-PCI Bridge
BIST	0Fh	7 : 0	R	00h	BIST is not supported.
Base Address Register	10h	31 : 0	See Table 5-5.		
I/O Address Register (PC/AT)	14h	31 : 0	See Table 5-6.		
I/O Address Register (PC-98 Series)	18h	31 : 0	N.A.		
Subsystem Vender ID	2Ch	15 : 0	R (/W)	0000h	Write enabled, according to setting of ID Write Mask bit
Subsystem ID	2Eh	15 : 0	R (/W)	0000h	
Interrupt Line	3Ch	7 : 0	R/W	00h	Indicates interrupt line's route
Interrupt Pin	3Dh	7 : 0	R	01h	Application of INTA#
Min_Gnt	3Eh	7 : 0	R	01h	Minimum request time for burst cycle
Max_lat	3Fh	7 : 0	R	15h	Frequency of bus access requests

Table 5-3. Command Register Information

Field	bit	Read/ Write	Value (Default)	Comment
I/O space	0	R/W	0b	Controls responses to I/O access
Memory space	1	R/W	0b	Controls responses to memory access
Bus Master	2	R/W	0b	Controls bus master operations
Special Cycles	3	R	0b	Ignores special cycles
Memory write and invalidate enable	4	R	0b	Sets memory write and invalidate as invalid
VGA palette snoop	5	R	0b	Sets VGA palette snoop as invalid
Parity Error response	6	R/W	0b	Controls response to parity error
Wait cycle control	7	R	0b	Address/data stepping is not supported.
SERR# enable	8	R/W	0b	Controls responses to system errors
Fast back-to-back enable	9	R	0b	Fast back-to-back access is not supported.
Reserved	15 : 10	R	000000b	Reserved

Table 5-4. Status Register Information

Field	bit	Read/ Write	Value	Comment
Reserved	4 : 0	R	00000b	Reserved
66MHz capable	5	R	0b	33-MHz operation
UDF supported	6	R	0b	UDF is not supported.
Fast back-to-back capable	7	R	0b	Fast back-to-back access is not supported.
Data Parity Error detected	8	R/W	"1" is set to this bit when the following three conditions are met. (1) Either PERR# was asserted by the parity error source or assertion of PERR# by the target source was detected. (2) The parity error source was the bus master during the bus cycle in which the data parity error occurred. (3) "1" has been set to the command register's Parity Error response bit.	
DEVSEL timing	10 : 9	R	01b	DEVSEL# assert timing: Medium speed
Signaled target abort	11	R/W	The target sets "1" if the bus cycle it is accessing ends due to a target abort condition.	
Received target abort	12	R/W	The master sets "1" if the bus cycle it is executing ends due to a target abort condition.	
Received master abort	13	R/W	The master sets "1" if the bus cycle it is executing ends due to a master abort condition.	
Signaled system error	14	R/W	"1" is set to this bit when SERR# is asserted.	
Detected parity error	15	R/W	"1" is set to this bit when data parity or address parity is detected.	

Table 5-5. Base Address (BAR_OHCI) Register Information

Field	bit	Read/ Write	Value (Default)	Comment
Memory space indicator	0	R	0b	Operational registers are mapped to main memory space.
Type	2 : 1	R	00b	Operational registers can be allocated in any part of the 4-G main memory space.
Prefetchable	3	R	0b	Prefetch is disabled.
Base address (LSB)	11 : 4	R	00h	Operational registers have a 4-Kbyte address space.
Base address (MSB)	31 : 12	R/W	000h	Indicates the high-order 20 bits of the base address in the Operational registers.

Table 5-6. I/O Address Register (PC/AT) Information

Field	bit	Read/ Write	Value (Default)	Comment
I/O space indicator	0	R	1b	Legacy register is mapped to the I/O space.
Reserved	1	R	0b	Reserved
Base address (LSB)	2	R	0b	Legacy register has an 8-byte address space.
Base address (MSB)	31 : 3	R/W	000h	Indicates the high-order 29 bits of the base address in the Legacy register.

Remark The I/O Address register is fixed to 0h when legacy support is invalid.
On the other hand, when legacy support is valid, the I/O Address Register (PC-98 Series: offset address 18h) is fixed at 0h.

Table 5-7. Power Management Control/Status Information

Field	bit	Read/ Write	Value (Default)	Comment
Power State	1 : 0	R/W	00b	Power State Control bit 00b = D0 (PCI CLK Full mode: Default) 01b = Reserved 10b = D2 (PCI CLK Stop and Device power on) 11b = D3 (PCI CLK Stop and Device power off)
Status Change Standby	2	R	0b	Indicates the device state in relation to control of Power State transitions 0b = Not Ready 1b = Ready
Bus Master Control	3	R/W	0b	Controls PCI command register's bit 2 (bus master bit) 0b = Bus master bit is invalid (ordinary bus master operation) 1b = Bus master bit is valid
Reserved	4	R	0b	Reserved
REQ_Enable	5	R/W	0b	REQ signal output timing control 0b = PCI clock synchronous output: Default 1b = PCI clock asynchronous output
PC_mode	6	R/W	0b	PC-98 Series / PC/AT switch setting control 0b = PC-98 Series mode: Default 1b = PC/AT mode
ID Write Mask	7	R/W	0b	Write protection of Subsystem ID and Subsystem Vendor ID 0b = Write Mask: Default 1b = Write Enable
Wakeup_Status	8	R/W	0b	"1" is set when a Wakeup request has been issued. Writing "1" clears the bit, but writing "0" does not change it.
Reserved	15 : 9	R	0b	Reserved
Wakeup_Enable	16	R/W	0b	Output control of WAKE signal 0b = WAKE signal is invalid: Default 1b = WAKE signal is valid
Reserved	31 : 17	R	0b	Reserved

Remarks 1. Be sure to use REQ_Enable the default. If used asynchronously, it may no longer comply with the PCI specifications.

2. The Power State bit is invalid when PC_mode = 0. The system has read/write access to the Power State bit. The HC has read-only access.

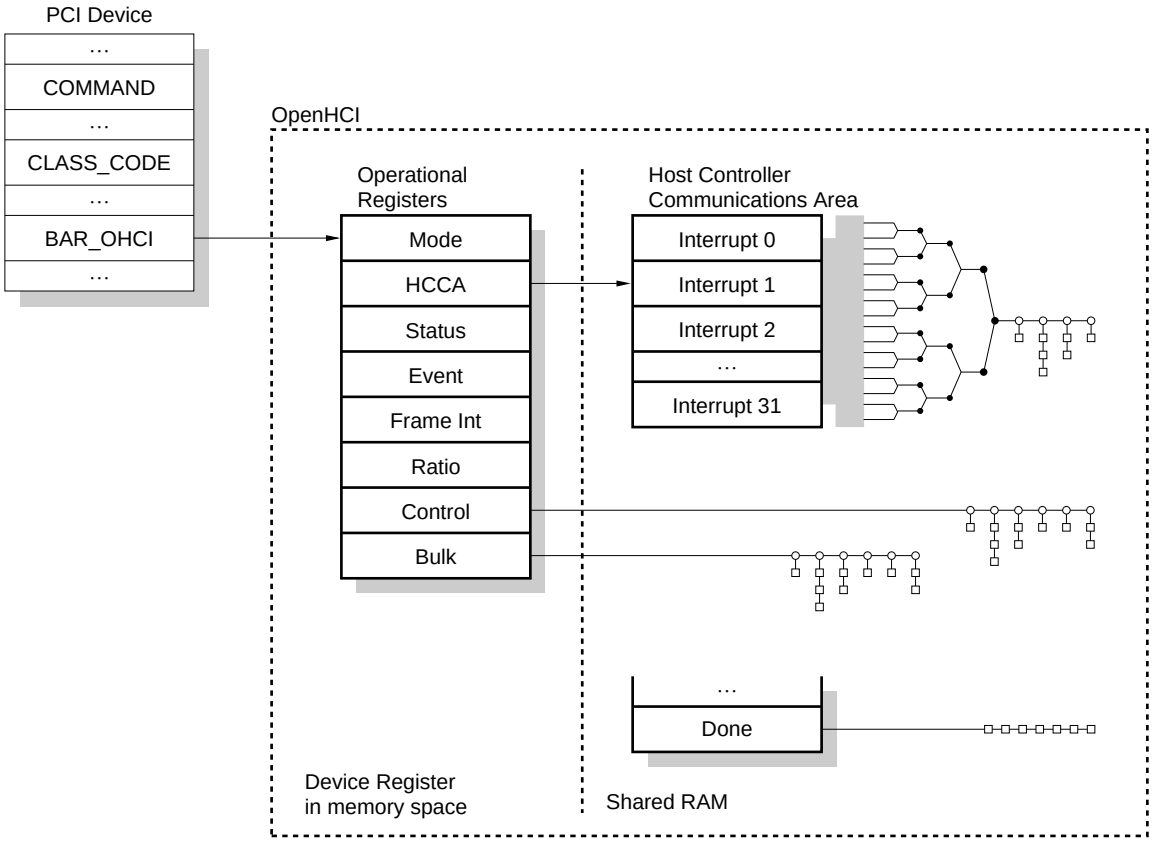
3. The Wakeup_Status bit is invalid when PC_mode = 0. When PC_mode = 1, Power State = 10, and HCFS = UsbSuspend, "1" is set when a RESUME signal from the USB is detected. At that point, if the Wakeup_Enable bit = 1, the WAKE signal is asserted. Writing "1" clears this bit and simultaneously deasserts WAKE. The above operations occur only when the HcInterruptEnable register's RHSC/RD bit has been set.

4. The Wakeup_Enable bit is invalid when PC_mode = 0.

5. After the Power State bit has been set as D2 or D3, "0" is output as the Status Change Standby value until the state transition is actually ready to occur, after which "1" is output. Once the Status Change Standby value becomes "1" after the Power State bit has been set as D2 or D3, it does not revert back to "0". This bit's value is always "0" when the Power State bit has been set as D0.

6. The Bus Master Control bit switches the command register's bus master bit's valid/invalid setting. When the Bus Master Control bit's value is "0", bus master operations are valid whether or not the bus master bit's value is set to "0".

Figure 5-1. OpenHCI's PCI Configuration Space



The PCI Configuration Space's Base Address (BAR_OHCI) Register is in an OpenHCI-compliant host controller. It indicates the base address of Operational Registers which are the starting point for communication with the host CPU.

5.2 Operational Registers

The host controller includes the Operational Registers, which are the starting point for communication with the host CPU. This set of registers is mapped to a 4-Kbyte range in the 4-Gbyte main memory space, where it is used by the HCD (Host Controller Driver). All of the registers in this set are read from or written to in Dword units. For a more detailed description, see the **Open HCI Specification Release 1.0** and **OpenHCI Legacy Support Interface Specification Release Version 1.01**.

Table 5-8. Host Controller Operational Registers

31 0	Offset
HcRevision	00h
HcControl	04h
HcCommandStatus	08h
HcInterruptStatus	0Ch
HcInterruptEnable	10h
HcInterruptDisable	14h
HcHCCA	18h
HcPeriodCurrentED	1Ch
HcControlHeadED	20h
HcControlCurrentED	24h
HcBulkHeadED	28h
HcBulkCurrentED	2Ch
HcDoneHead	30h
HcFmInterval	34h
HcFmRemaining	38h
HcFmNumber	3Ch
HcPeriodicStart	40h
HcLSThreshold	44h
HcRhDescriptorA	48h
HcRhDescriptorB	4Ch
HcRhStatus	50h
HcRhPortStatus1	54h
HcRhPortStatus2	58h

Table 5-9. Legacy Support Registers

31 0	Memory Offset	I/O Address
HceControl	100h	
HceInput	104h	60h/64h
HceOutput	108h	60h
HceStatus	10Ch	64h

5.2.1 Overview of operational registers

Register: HcRevision **Offset Address: 00h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
Revision	7 : 0	R	R	10h	Complies with OpenHCI R1.0
Legacy	8	R	R/W	Xb	Includes a legacy support register. It is set to suit the setting of external pin LEGC. LEGC = 0 → Set to "0" LEGC = 1 → Set to "1"
Reserved	31 : 9	R/W	R	Xh	Reserved

Register: HcControl **Offset Address: 04h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
ControlBulkServiceRatio (CBSR)	1 : 0	R/W	R	00b	Indicates the control/bulk service ratio between EDs. CBSR: No. of Control EDs Over Bulk EDs Served 0: 1 : 1 1: 2 : 1 2: 3 : 1 3: 4 : 1
PeriodicListEnable (PLE)	2	R/W	R	0b	Sets the next frame's periodic list servicing as valid or invalid. 1: Valid, 0: Invalid
IsochronousEnable (IE)	3	R/W	R	0b	Sets the next frame's isochronous ED servicing as valid or invalid. 1: Valid, 0: Invalid
ControlListEnable (CLE)	4	R/W	R	0b	Sets the next frame's control list servicing as valid or invalid. 1: Valid, 0: Invalid
BulkListEnable (BLE)	5	R/W	R	0b	Sets the next frame's bulk list servicing as valid or invalid. 1: Valid, 0: Invalid
HostControllerFunctionalState for USB (HCFS)	7 : 6	R/W	R/W	00b (H/W_R[Note 1]) 11b (S/W_R[Note 2])	00b: USBRESET 01b: USBRESUM 10b: USBOPERATIONAL 11b: USBSUSPEND
InterruptRouting (IR)[Note 3]	8	R/W	R	0b	This bit indicates the route of an interrupt that is triggered by an event registered in HcInterruptStatus. 1: SMI output, 0: INT output
RemoteWakeupConnected (RWC)[Note 3]	9	R/W	R/W	0b	This bit indicates whether or not remote wakeup signals are supported. 1: Supported, 0: Not supported
RemoteWakeupEnable (RWE)	10	R/W	R	0b	Sets remote wakeup signal as valid or invalid when upstream resume signal is detected.
Reserved	31 : 11	R/W	R	Xh	Reserved

Notes 1. H/W_R = Hardware Reset
2. S/W_R = Software Reset
3. Only Hardware Reset is available.

Register: HcCommandStatus Offset Address: 08h

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
HostControllerReset (HCR)	0	R/W	R/W	0b	HC software reset. This bit is set by the HCD and cleared by the HC.
ControlListFilled (CLF)	1	R/W	R/W	0b	Indicates whether or not a TD exists in the control list.
BulkListFilled (BLF)	2	R/W	R/W	0b	Indicates whether or not a TD exists in the bulk list.
OwnershipChangeRequest (OCR)	3	R/W	R/W	0b	This bit is set by the HCD to request modification of HC control.
Reserved	15 : 4	R/W	R	Xh	Reserved
SchedulingOverrunCount (SOC)	17 : 16	R	R/W	00b	This bit is incremented when a scheduling overrun error occurs. It is initialized by 00b and is returned to its previous value by 11b.
Reserved	31 : 18	R/W	R	Xh	Reserved

Register: HcInterruptStatus Offset Address: 0Ch

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
SchedulingOverrun (SO)	0	R/W	R/W	0b	This bit is set when an overrun occurs during USB scheduling of the current frame.
WritebackDoneHead (WDH)	1	R/W	R/W	0b	This bit is set when HcDoneHead has been written to HccaDoneHead. The HCD clears this bit after the contents of HccaDoneHead have been saved.
StartofFrame (SF)	2	R/W	R/W	0b	This bit is set at the start of a frame.
ResumeDetected (RD)	3	R/W	R/W	0b	This bit is set when a resume signal has been detected.
UnrecoverableError (UE)	4	R/W	R/W	0b	This bit is set when a system error that is unrelated to USB has been detected.
FrameNumberOverflow (FNO)	5	R/W	R/W	0b	This bit is set when the value of the MSb (bit 15) of HcFmNumber has changed from “0” to “1” or from “1” to “0”.
RootHubStatusChange (RHSC)	6	R/W	R/W	0b	This bit is set when the contents of either HcRhStatus or HcRhPortStatusX are changed.
Reserved	29 : 7	R/W	R	Xh	Reserved
OwnershipChange (OC)	30	R/W	R/W	0b	This bit is set by the HC when the HCD has set the OCR field in the HcCommandStatus register. If this event is not masked, it immediately triggers a system management interrupt (SMI).
other	31	R	R	0b	

Register: HcInterruptEnable Offset Address: 10h

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
SO	0	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Scheduling Overrun
WDH	1	R/W	R	0b	0: Ignore 1: Interrupt is triggered by HcDoneHead Writeback
SF	2	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Start of Frame
RD	3	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Resume Detect
UE	4	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Unrecoverable Error
FNO	5	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Frame Number Overflow
RHSC	6	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Root Hub Status Change
Reserved	29 : 7	R/W	R	Xh	Reserved
OC	30	R/W	R	0b	0: Ignore 1: Interrupt is triggered by Ownership Change
Master Interrupt Enable (MIE)	31	R/W	R	0b	0: Ignore 1: Interrupt triggering is enabled when an event other than those listed above occurs.

Register: HcInterruptDisable Offset Address: 14h

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
SO	0	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Scheduling Overrun
WDH	1	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by HcDoneHead Writeback
SF	2	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Start of Frame
RD	3	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Resume Detect
UE	4	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Unrecoverable Error
FNO	5	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Frame Number Overflow
RHSC	6	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Root Hub Status Change
Reserved	29 : 7	R/W	R	Xh	Reserved
OC	30	R/W	R	0b	0: Ignore 1: Interrupt is not triggered by Ownership Change
Master Interrupt Enable (MIE)	31	R/W	R	0b	0: Ignore 1: Interrupt triggering is disabled when an event other than those listed above occurs.

Register: HcHCCA **Offset Address: 18h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
Host Controller Communication Area (HCCA)	7 : 0	R	R	00h	This is the base address of the Host Controller Communication Area. Since it is allocated in 256-byte units, the low-order 8 bits are fixed at “0”.
	31 : 8	R/W	R	0h	

Register: HcPeriodCurrentED **Offset Address: 1Ch**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
PeriodCurrentED (PCED)	3 : 0	R	R	00h	This is the physical address of an Isochronous or Interrupt ED in the periodic list being serviced during the current frame. Since the ED is allocated in 16-byte units, the low-order 4 bits are fixed at “0”.
	31 : 4	R	R/W	0h	

Register: HcControlHeadED **Offset Address: 20h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
ControlHeadED (CHED)	3 : 0	R	R	00h	This is the physical address of the first ED in the control list.
	31 : 4	R/W	R	0h	

Register: HcControlCurrentED **Offset Address: 24h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
ControlCurrentED (CCED)	3 : 0	R	R	00h	This is the physical address of the current ED in the control list.
	31 : 4	R/W	R/W	0h	

Register: HcBulkHeadED **Offset Address: 28h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
BulkHeadED (BHED)	3 : 0	R	R	00h	This is the physical address of the first ED in the bulk list.
	31 : 4	R/W	R	0h	

Register: HcBulkCurrentED **Offset Address: 2Ch**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
BulkCurrentED (BCED)	3 : 0	R	R	00h	This is the physical address of the current ED in the bulk list.
	31 : 4	R/W	R/W	0h	

Register: HcDoneHead **Offset Address: 30h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
DoneHead (DH)	3 : 0	R	R	00h	This is the physical address of the last TD to be added to the Done queue.
	31 : 4	R	R/W	0h	

Register: HcFmInterval **Offset Address: 34h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
FrameInterval (FI)	13 : 0	R/W	R	2EDFh	This bit indicates a bit time value for the time interval per frame.
Reserved	15 : 14	R/W	R	Xh	Reserved
FSLargestDataPacket (FSMPS)	30 : 16	R/W	R	0000h	This is the maximum number of data bits that can be sent or received in one transaction.
FrameIntervalToggle (FIT)	31	R/W	R	0b	This is inverted when loading to FI.

Register: HcFmRemaining **Offset Address: 38h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
FrameRemaining (FR)	13 : 0	R	R/W	0h	This is a 14-bit down counter which indicates the remaining bit time in the current frame.
Reserved	30 : 14	R/W	R	Xh	Reserved
FrameRemainingToggle (FRT)	31	R	R/W	0b	When the value of FR becomes “0”, a value is loaded from the FIT field of the HcFmInterval register.

Register: HcFmNumber **Offset Address: 3Ch**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
FrameNumber (FN)	15 : 0	R	R/W	0h	This is a 16-bit counter that is incremented when HcFmRemaining is reloaded.
Reserved	31 : 16	R/W	R	Xh	Reserved

Register: HcPeriodicStart **Offset Address: 40h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
PeriodicStart (PS)	13 : 0	R/W	R	0h	This indicates that periodic list servicing should be started. The standard value is 3E67h.
Reserved	31 : 14	R/W	R	Xh	Reserved

Register: HcLSThreshold **Offset Address: 44h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
LSThreshold (LST)	11 : 0	R/W	R	0628h	This includes a value that is used to determine whether or not to send the LS packet before the EOF token.
Reserved	31 : 12	R/W	R	Xh	Reserved

Register: HcRhDescriptorA **Offset Address: 48h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
NumberDownstreamPorts (NDP)[Note]	7 : 0	R	R	02h	This bit indicates the number of downstream ports that are supported by the root hub.
PowerSwitchingMode (PSM)[Note]	8	R/W	R	1b	0: Power supply is applied to all ports at the same time. 1: Power supply is applied separately to each port.
NoPowerSwitching (NPS)[Note]	9	R/W	R	0b	0: Power supply to ports can be switched on and off. 1: Power supply to ports is always applied when HC's power is on.
DeviceType (DT)[Note]	10	R	R	0b	Indicates that the root hub is not a hybrid type of device.
OverCurrentProtectionMode (OCPM)[Note]	11	R/W	R	1b	0: Overcurrent status is reported to all downstream ports at once. 1: Overcurrent status is reported separately to each port.
NoOverCurrentProtection (NOCP)[Note]	12	R/W	R	0b	0: Overcurrent status is reported. 1: Overcurrent protection is not supported.
Reserved	23 : 13	R/W	R	Xh	Reserved
PowerOnToPowerGoodTime (POTPGT)[Note]	31 : 24	R/W	R	FFh	This bit indicates the amount of time that the HCD must wait before accessing the root hub port to which a power supply is applied.

Note This field can only be used for hardware resets.

Register: HcRhDescriptorB **Offset Address: 4Ch**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
DeviceRemovable (DR)[Note]	15 : 0	R/W	R	0000h	bit0: Reserved bit1: Device is connected to Port#1 bit2: Device is connected to Port#2 ⋮ bit15: Device is connected to Port#15
PortPowerControlMask (PPCM)[Note]	31 : 16	R/W	R	FFFEh	bit0: Reserved bit1: Power supply to Port#1 set is masked bit2: Power supply to Port#2 set is masked ⋮ bit15: Power supply to Port#15 set is masked

Note This field can only be used for hardware resets.

Register: HcRhStatus **Offset Address: 50h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
LocalPowerStatus (LPS)[Note]	0	R	R	0b	The root hub does not support local power status.
ClearGlobalPower (CGP)[Note]		W	R	0b	1: Power supply to all ports is off when PSM = 0. When PSM = 1, only PPS is cleared for ports where PPCM has not been set. 0: No change
OverCurrentIndicator (OCI)[Note]	1	R	R/W	0b	The following occurs when overcurrent status is reported to all downstream ports at once. 1: Overcurrent status exists 0: Normal power supply operations Be sure that this is set to “0” when overcurrent status is to be reported to each port.
Reserved	14 : 2	R/W	R	Xh	Reserved
DeviceRemoteWakeupEnable (DRWE)[Note]	15	R	R	0b	0: CSC is not a remote wakeup event 1: CSC is a remote wakeup event
SetRemoteWakeupEnable (SRWE)[Note]		W	R	0b	1: Sets RWE 0: No change
LocalPowerStatusChange (LPSC)[Note]	16	R	R	0b	The root hub does not support local power status.
SetGlobalPower (SGP)[Note]		W	R	0b	1: Power supply to all ports is on when PSM = 0. When PSM = 1, only PPS is set for ports where PPCM has not been set. 0: No change
OverCurrentIndicatorChange (CCIC)[Note]	17	R/W	R/W	0b	HC sets “1” when a change has occurred in OCI. It is cleared when the HCD writes “1”. There is no change when the HCD writes “0”.
Reserved	30 : 18	R/W	R	Xh	Reserved
ClearRemoteWakeupEnable (CRWE)[Note]	31	W	R	0b	1: Clears RWE 0: No change
other		R	R	0b	

Note This field can only be used for hardware resets.

Register: HcRhPortStatus [1:2] **Offset Address: 54h, 58h**

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
CurrentConnectStatus (CCS)[Note]	0	R	R/W	0b	This bit is set when a device has been connected. This bit is cleared when the device is disconnected or when the power to the port is turned off.
PortEnableStatus (PES)[Note]	1	R	R/W	0b	This bit is set by the following conditions. • When SPE is issued while CCS = 1 • When PRSC is set • When PSSC is set It is cleared by the following conditions. • When an overcurrent occurs • When a device is disconnected • When the port's power is off • When an operational error, such as bubble detection, occurs • When CPE is issued
PortSuspendStatus (PSS)[Note]	2	R	R/W	0b	This bit is set when SPS is issued while CCS = 1. It is cleared when PSSC or PRSC is set, when HCFS = 01b, or when the port's power is off.
PortOverCurrentIndicator (POCI)[Note]	3	R	R/W	0b	This bit is set when an overcurrent has occurred while NOCP = 0 and OCPM = 1. It is cleared when the setting condition is canceled.
PortResetStatus (PRS)[Note]	4	R	R/W	0b	This bit is set when SPR is issued while CCS = 1. It is cleared when PSSC or PRSC is set, when HCFS = 01b, or when the port's power is off.
PortPowerStatus (PPS)[Note]	8	R	R/W	0b	This bit is set by the following conditions. • When SGP is issued while NPS = 1 or NPS = 0, and PSM = 0. • When SGP is issued while NPS = 0, PSM = 1, and the corresponding bit in PPCM = 0 • When SPP is issued while NPS = 0, PSM = 1, and the corresponding bit in PPCM = 1 It is cleared by the following conditions. • When CGP is issued while NPS = 1 or NPS = 0, and PSM = 0 • When CGP is issued while NPS = 0, PSM = 1, and the corresponding bit in PPCM = 0 • When CPP is issued while NPS = 0, PSM = 1, and the corresponding bit in PPCM = 1 • When an overcurrent occurs
LowSpeedDeviceAttached (LSDA)[Note]	9	R	R/W	0b	This bit is set when a low-speed device is connected. It is cleared when a full-speed device is connected.
ConnectStatusChange (CSC)[Note]	16	R/W	R/W	0b	This bit is set by the following conditions. • By a change in CCS or by setting of the corresponding bit in DR • SPR/SPE/SPS is issued when CCS = 0. It is cleared when "1" is written by the HCD.

Field	Bit	Read/Write		Value (Default)	Comment
		HCD	HD		
PortEnableStatusChange (PESC)[Note]	17	R/W	R/W	0b	This bit is set by the following conditions. • When an overcurrent occurs • When a device is disconnected • When a port's power is off • When an operational error, such as bubble detection, occurs It is cleared when "1" is written by the HCD.
PortSuspendStatusChange (PSSC)[Note]	18	R/W	R/W	0b	This bit is set by completion of a RESUME signal. It is cleared when "1" is written by the HCD or when PRSC is set.
PortOverCurrentIndicator Change (OCIC)[Note]	19	R/W	R/W	0b	This bit is set when POCI changes. It is cleared when "1" is written by the HCD.
PortResetStatusChange (PRSC)[Note]	20	R/W	R/W	0b	This bit is set by completion of a RESET signal. It is cleared when "1" is written by the HCD.

Note This field can only be used for hardware resets.

5.2.2 Overview of legacy support registers

Register	Memory Address Offset	I/O Address	Read/Write	Comment
			HCD	
HceControl	100h		R/W	This register is used to transmit various types of status information such as setting emulation hardware as valid, and controlling it.
HceStatus	10Ch		R/W	This is the legacy status register for emulation. Input from port 64h indicates the current value of HceStatus without causing other operations.
		64h	R	
HceInput	104h		R/W	This is the legacy input buffer register for emulation. Output to port 60h sets “1” to InputFull and “0” to CmdData in the HceStatus register. Output to port 64h sets “1” to InputFull and CmdData in the HceStatus register.
		60h	W	
		64h	W	
HceOutput	108h		R/W	This is the legacy output buffer register for emulation in which software writes to a keyboard or mouse device. Input from port 60h sets “0” to OutputFull in the HceStatus register.
		60h	R	

Remark When emulation is enabled (valid), the HceStatus, HceInput, and HceOutput registers can be accessed via I/O addresses 60h and 64h.

Register: HceInput

Field	bit	Read/Write	Value (Default)	Comment
		HCD		
InputData	7 : 0	R/W	Xh	This bit retains the data that is written to I/O ports 60h and 64h when emulation is enabled.
Reserved	31 : 8	–	Xh	Reserved

Register: HceOutput

Field	bit	Read/Write	Value (Default)	Comment
		HCD		
OutputData	7 : 0	R/W	Xh	This bit retains the data that is returned when the application software reads from port 60h and emulation is enabled.
Reserved	31 : 8	–	Xh	Reserved

Register: HceStatus

Field	bit	Read/Write HCD	Value (Default)	Comment
OutputFull	0	R/W	0b	When I/O port 60h is read, “0” is set by the HC. When IRQEn has been set and AuxOutputFull has been set to “0”, IRQ1 occurs as long as this bit’s value is “1”. When IRQEn has been set and AuxOutputFull has been set to “1”, IRQ12 occurs as long as this bit’s value is “1”. When this bit’s value is “0” and HceControl’s CharacterPending value is “1”, the emulation interrupt condition has been met.
InputFull	1	R/W	0b	“1” is set to this bit during an I/O write operation to address 60h and 64h, except in the case of the GateA20 sequence. When this bit’s value is “1”, the emulation interrupt condition has been met as long as emulation is enabled.
Flag	2	R/W	0b	This bit is used as a system flag which ordinary software uses to indicate warm/cold boot status.
CmdData	3	R/W	0b	“0” is set by the HC when writing to port 60h and “1” is set by the HC when writing to port 64h.
Inhibit Switch	4	R/W	0b	This bit indicates the status of the keyboard inhibit switch. It is set when the keyboard is disabled (inhibit status).
AuxOutputFull	5	R/W	0b	“1” is set to OutputFull when this bit is set to “1”. IRQ12 is always asserted when the IRQEn bit has been set.
Timeout	6	R/W	0b	This bit is used to indicate a timeout condition.
Parity	7	R/W	0b	This bit indicates a keyboard/mouse data parity error.
Reserved	31 : 9	–	Xh	Reserved

Register: HceControl

Field	bit	Read/Write	Value (Default)	Comment
		HCD		
EmulationEnable	0	R/W	0b	When this bit's value is "1", the host controller is able to perform legacy emulation. The host controller decodes access to I/O registers 60h and 64h and IRQ1 or IRQ12 occur if the access is acceptable. The host controller may also generate an emulation interrupt when necessary to call up the emulation software.
EmulationInterrupt	1	R	–	This bit is used to passively decode emulation interrupt conditions. This bit's value becomes "1" when emulation interrupt status is ON.
CharacterPending	2	R/W	0b	When this bit has been set, an emulation interrupt occurs if the HceStatus register's OutputFull bit's value is "0".
IRQEn	3	R/W	0b	When this bit has been set, the host controller generates IRQ1 or IRQ12 if the HceStatus register's OutputFull bit's value is "1". Specifically, IRQ1 occurs when the HceStatus register's AuxOutputFull bit's value is "0" and IRQ12 occurs when it is "1".
ExternallRQEn	4	R/W	0b	When this bit's value is "1", an emulation interrupt is triggered by IRQ1 and IRQ12 from the keyboard controller. The function that controls this bit does not depend on the setting of the EmulationEnable bit in this register.
GateA20Sequence	5	R/W	0b	When D1h is written to I/O port 64h, this bit is set by the HC. When a value other than D1h is written to I/O port 64h, this bit is cleared.
IRQ1Active	6	R/W	0b	This bit indicates when a positive transition has occurred for IRQ1 from the keyboard controller. Software writes "1" to this bit in order to clear this setting (to "0"). Nothing occurs when software writes "0" to this bit.
IRQ12Active	7	R/W	0b	This bit indicates when a positive transition has occurred for IRQ12 from the keyboard controller. Software writes "1" to this bit in order to clear this setting (to "0"). Nothing occurs when software writes "0" to this bit.
A20State	8		0b	This bit indicates the current status of the keyboard controller's GateA20. When GateA20Sequence is active, this bit is used for comparison with the value that was written to 60h.
Reserved	31 : 9	–	–	This bit is reserved. It must always be set to "0".

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Buffer List

- 5 V schmitt buffer
  RST, SCLK, AT, LEGC

- 5 V I_{OL} = 12 mA N-ch Open Drain buffer
  SMI

- 5 V input buffer
  RCVBE

- 5 V excessive through current prevention buffer
  OCI (2:1), IRI1, IRI2

- 5 V I_{OL} = 6 mA Output buffer
  PPON (2:1), WAKE

- 5 V I_{OL} = 6 mA N-ch Open Drain buffer
  IRO1, IRO2, A20S

- 5 V PCI interface (3-V PCI interface with 5-V maximum voltage circuit)
  AD (31:00), CBE (3:0), PAR, FRAME, IRDY, TRDY, STOP, IDSEL, DEVSEL, REQ, GNT, PERR, SERR, INTA, PCLK, CRUN

- USB interface
  DP (2:1), DN (2:1)

Above, “5 V” refers to a 3-V buffer that is 5-V tolerant (has 5-V maximum voltage). Therefore, it is possible to have a 5-V connection for an external bus, but the output level will be only up to 3 V, which is the V_{DD} voltage. Similarly, “5 V PCI” above refers to a PCI buffer that has a 5-V maximum voltage circuit which meets the 3-V PCI standard; it does not refer to a PCI buffer that meets the 5-V PCI standard.

6.2 Absolute Maximum Ratings

Table 6-1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage, 5-V buffer	V_I	3.0 V ≤ V_{DD} ≤ 3.6 V V_I < V_{DD} + 3.0 V	–0.5 to +6.6	V
Output voltage, 5-V buffer	V_O	3.0 V ≤ V_{DD} ≤ 3.6 V V_O < V_{DD} + 3.0 V	–0.5 to +6.6	V
USB common mode voltage	V_{CM}		–0.5 to +3.8	V
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may deteriorate if an absolute maximum rating is exceeded for even one parameter or even momentarily. Absolute maximum ratings are the highest values at which physical damage will not occur. Therefore, be sure that none of these maximum ratings are exceeded when using this product.

6.3 Recommended Operating Conditions

Table 6-2. Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating voltage	V_{DD}		3.0	3.3	3.6	V
Input voltage	V_I	Except DP/DN pin	0		V_{DD}	V
DP/DN input voltage	V_{IU}		0		3.3	V

6.4 Pin Capacitance

Table 6-3. Pin Capacitance

Parameter	Symbol	Conditions	MIN	MAX	Unit
Input capacitance, 5-V buffer	C_I	V_{DD} = 0 V, T_A = 25°C	9	12	pF
Output capacitance, 5-V buffer	C_O	fc = 1 MHz	9	12	pF
I/O capacitance, 5-V buffer	C_{IO}	Unmeasured pins returned to 0 V	9	12	pF
PCI clock input pin capacitance	C_{clk}		9	12	pF
PCI IDSEL input pin capacitance	C_{IDSEL}			8	pF
Pin inductance	L_{pin}			20	nH
DPx/DNx pin capacitance	C_{IN}			20	pF

6.5 DC Characteristics (V_{DD} = 3.0 V to 3.6 V, T_A = 0 to +70°C)

Table 6-4. DC Characteristics

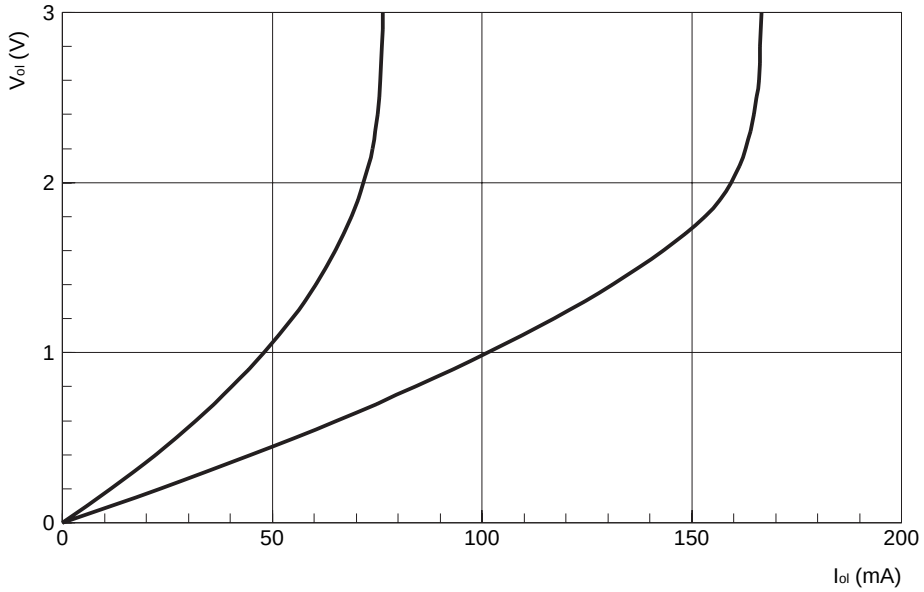
Parameter	Symbol	Conditions	MIN	MAX	Unit
Static current consumption	I_{DDSL}	PCI/USB clock is stopped, RCVBE = L		300	μA
	I_{DDSH}	PCI/USB clock is stopped, RCVBE = H		8	mA

Table 6-5. DC Characteristics (PCI Interface Block)

Parameter	Symbol	Conditions	MIN	MAX	Unit
High-level input voltage	V_{ih}		0.5 V_{DD}	V_{DD} + 0.5	V
Low-level input voltage	V_{il}		–0.5	0.3 V_{DD}	V
Input leakage current	I_{il}	0 < V_{in} < V_{DD}		±10	μA
High-level output voltage	V_{oh}	I_{OUT} = –500 μA	0.9 V_{DD}		V
Low-level output voltage	V_{ol}	I_{OUT} = 1500 μA		0.1 V_{DD}	V

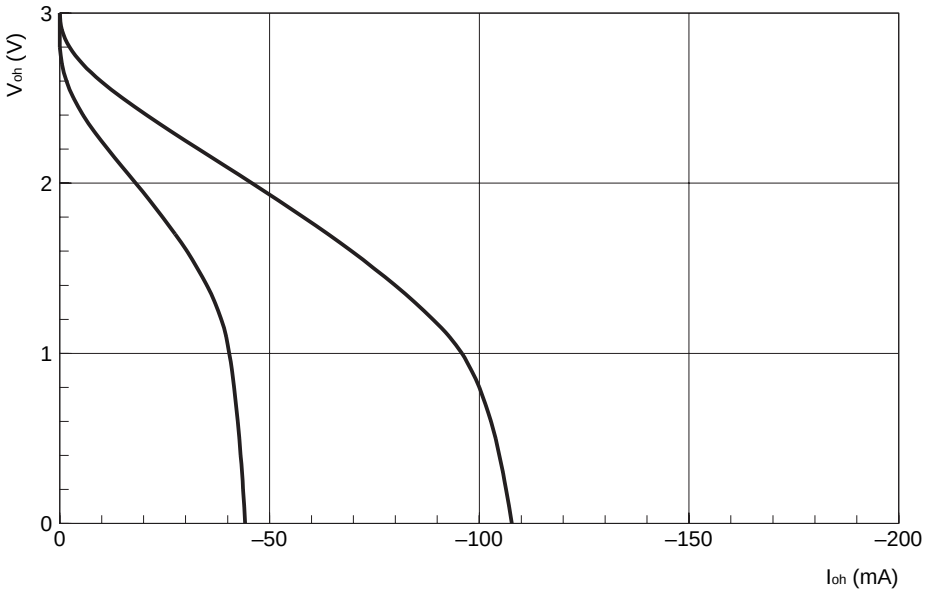
Figure 6-1. V_O vs. I_O (PCI Buffer)

(a) V_{ol} vs I_{ol} (V_{DD} = 3.0 V)



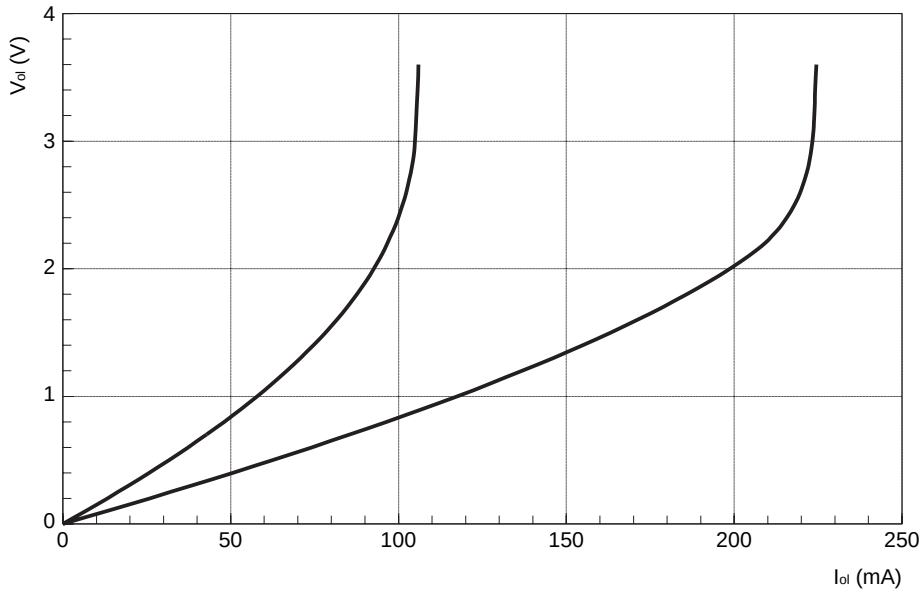
Remark Min value (process = worst, T_A = 70°C), max value (process = best, T_A = 0°C)

(b) V_{oh} vs I_{oh} (V_{DD} = 3.0 V)



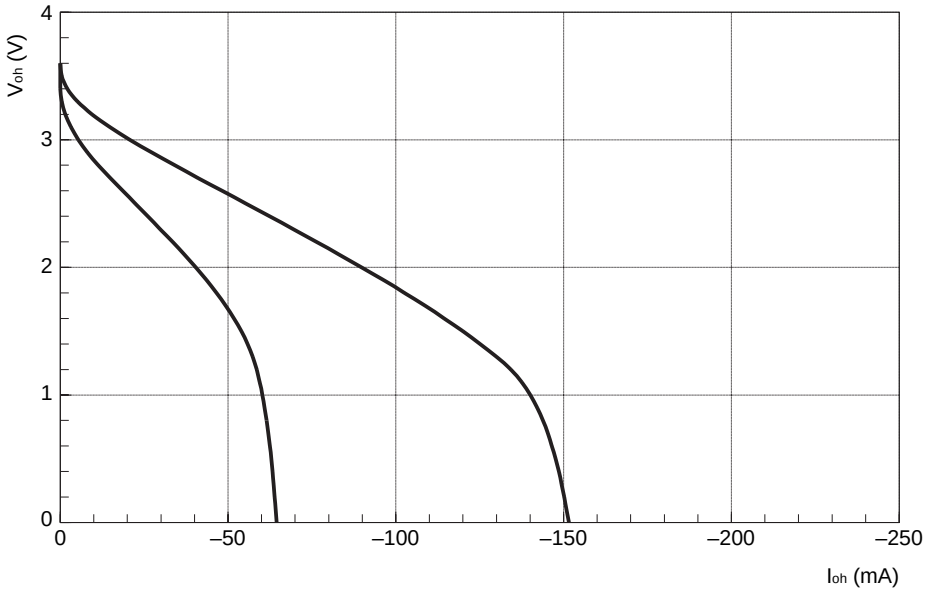
Remark Min value (process = worst, T_A = 70°C), max value (process = best, T_A = 0°C)

(c) V_{OL} vs I_{OL} (V_{DD} = 3.6 V)



Remark Min value (process = worst, T_A = 70°C), max value (process = best, T_A = 0°C)

(d) V_{OH} vs I_{OH} (V_{DD} = 3.6 V)



Remark Min value (process = worst, T_A = 70°C), max value (process = best, T_A = 0°C)

Table 6-6. DC Characteristics (USB Interface Block)

Parameter	Symbol	Conditions	MIN	MAX	Unit
Data line high impedance leakage current	I_{LO}	0 V < V_{IN} < 3.3 V		±10	μA
Differential input sensitivity	V_{DI}	| (D+) – (D–) |	0.2		V
Common mode voltage	V_{CM}		0.8	2.5	V
Single-ended 0 reception threshold	V_{SE}		0.8	2.0	V
High-level output voltage	V_{OH}	R_L of 15 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.5 kΩ to 3.6 V		0.3	V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Output pin impedance	Z_{DRV}		28	43	Ω

Remark The output pin impedance is a value for discrete buffers. In other words, an external series resistance is not required.

Figure 6-2. V_{CM} (Common Mode Voltage) vs. V_{DI} (Differential Input Sensitivity)

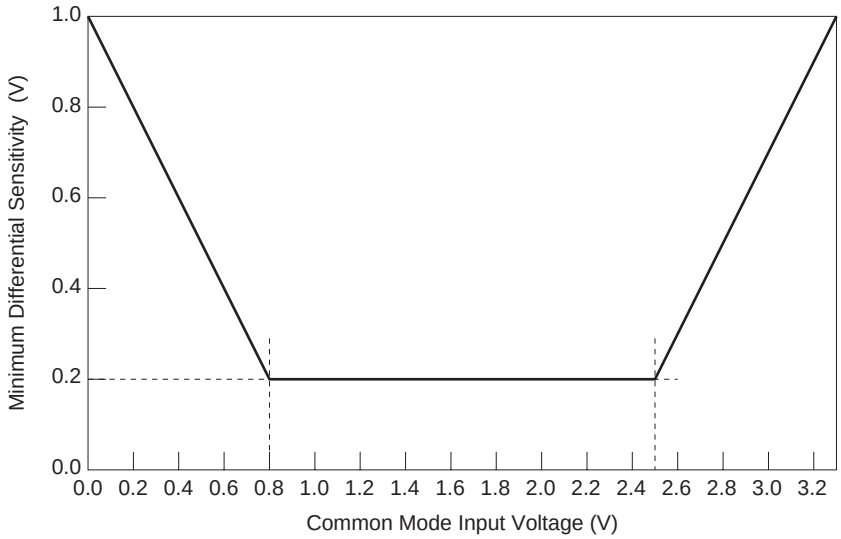


Table 6-7. DC Characteristics (Control Pin Block)

Parameter	Symbol	Conditions	MIN	MAX	Unit
High-level input voltage 5-V buffer	V_{IH}		2.0	5.5	V
Low-level input voltage 5-V buffer	V_{IL}		0	0.8	V
Positive trigger voltage 5-V buffer	V_P		2.2	2.55	V
Negative trigger voltage 5-V buffer	V_N		0.84	1.01	V
Hysteresis voltage 5-V buffer	V_H		1.1	1.5	V
Off-state output current 5-V buffer	I_{OZ}	$V_O = V_{DD}$ or GND		±14	μA
Input leakage current 5-V buffer	I_{IL}	$V_O = V_{DD}$ or GND		±10	μA
High-level output current 5-V buffer	I_{OH}	V_O = 0.4 V	–3.0		mA
Low-level output current 5-V buffer	I_{OL}	$V_O = V_{DD}$ – 0.4 V $V_O = V_{DD}$ – 0.4 V	12.0 6.0		mA mA
Output run-off current 5-V buffer	I_R	V_{PU} = 5.5 V, R_{PU} = 2 kΩ V_O = 3.0 V		14	μA

6.6 Power Consumption

Table 6-8. Power Consumption Characteristics

Parameter	Symbol	Conditions	TYP	Unit
Power consumption	P_{WD0_O}	Device state = D0, USB = Operational	500	mW
	P_{WD0_S}	Device state = D0, USB = Suspend/Reset	150	mW
	P_{WD2}	Device state = D2, USB = Suspend/Reset	100	mW
	P_{WD3}	Device state = D3, USB = Reset	100	mW

Remark When the device state = D0, the clock is defined as it is during normal operation.
When the device state = D2 or D3, the PCI clock is defined as when it is suspended.

6.7 System Clock Ratings

Table 6-9. System Clock Ratings

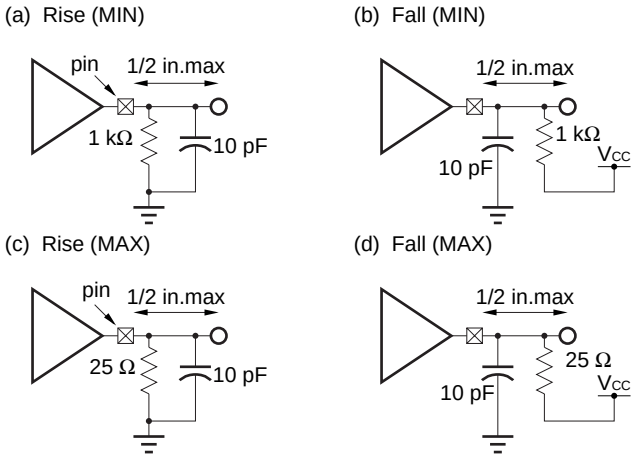
Parameter	Symbol	Ratings	Unit
Clock frequency	f_{CLK}	48 ±500 PPM	MHz
Clock Duty cycle	t_{DUTY}	±10	%
Input rise time	t_r	5 (from 0.4 V to 2.4 V)	ns
Input fall time	t_f	5 (from 2.4 V to 0.4 V)	ns

6.8 AC Characteristics (V_{DD} = 3.0 V to 3.6 V, T_A = 0 to +70°C)

Table 6-10. AC Characteristics (PCI Interface Block)

Parameter	Symbol	Conditions	MIN	MAX	Unit
PCI clock cycle time	t_{cyc}		30		ns
PCI clock pulse, high-level width	t_{high}		11		ns
PCI clock pulse, low-level width	t_{low}		11		ns
PCI clock, rise slew rate	S_{cr}	0.2 V_{DD} to 0.6 V_{DD}	1	4	V/ns
PCI clock, fall slew rate	S_{cf}	0.2 V_{DD} to 0.6 V_{DD}	1	4	V/ns
PCI reset active time (vs. power supply stability)	t_{rst}		1		ms
PCI reset active time (vs. CLK Start)	$t_{rst\text{-}clk}$		100		μs
Output float delay time (vs. RST↓)	$t_{rst\text{-}off}$			40	ns
PCI reset rise slew rate	S_{rr}		50		mV/ns
PCI bus signal output time (vs. PCLK↑)[Note 1]	t_{val}			T.B.D	ns
PCI point-to-point signal output time (vs. PCLK↑)[Note 1]	$t_{val\ (ptp)}$	REQ		T.B.D	ns
Output delay time (vs. PCLK↑)	t_{on}			T.B.D	ns
Output float delay time (vs. PCLK↑)	t_{off}			T.B.D	ns
PCI output rise slew rate[Note 2]	$slew_r$	0.2 V_{DD} to 0.6 V_{DD}	1	4	V/ns
PCI output fall slew rate[Note 2]	$slew_f$	0.2 V_{DD} to 0.6 V_{DD}	1	4	V/ns
Input setup time (vs. PCLK↑)	t_{su}		T.B.D		ns
Point-to-point input setup time (vs. PCLK↑)	$t_{su\ (ptp)}$	GNT	T.B.D		ns
Input hold time	t_h		T.B.D		ns
PCI clock reset allowable time (vs. CRUN↓)	$t_{crun\text{-}clk}$			5	μs
GNT assert allowable time (vs. CRUN↓)	$t_{crun\text{-}gnt}$	vs. ISO transaction that is at least 64 bytes in length		7	μs
INTA, SMI, WAKE cancellation time	t_{intc}	From when register is set		170	ns

Notes 1. The measurement conditions for tval are as follows.



2. The measurement conditions for the PCI output slew rate are the same as (a) and (b) above.

Table 6-11. AC Characteristics (USB Interface Block)

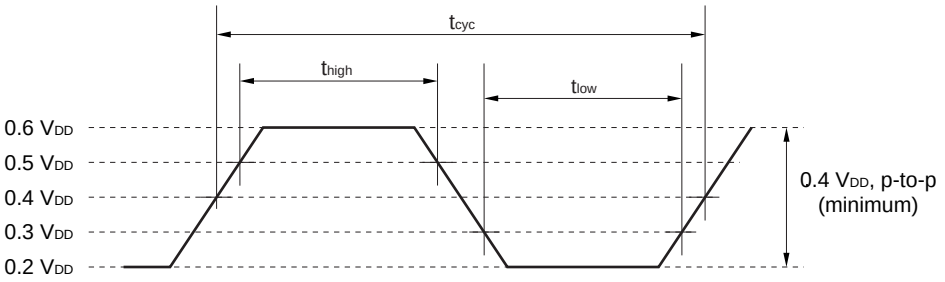
Parameter	Symbol	Conditions	MIN	MAX	Unit
Disconnect decision time	T_{dis}		2.5		μs
Connect decision time	T_{con}		2.5		μs
Rise time					
Full speed	T_R	C_L = 50 pF	4	20	ns
Low speed		C_L = 50 pF	75		ns
		C_L = 350 pF		300	ns
Fall time					
Full speed	T_F	C_L = 50 pF	4	20	ns
Low speed		C_L = 50 pF	75		ns
		C_L = 350 pF		300	ns
Rise/fall matching	T_{RFM}				
Full speed		(TR/TF)	90	110	%
Low speed		(TR/TF)	80	120	%
Data rate	T_{DRATE}				
Full speed			11.97	12.03	Mbs
Low speed			1.4775	1.5225	Mbs
Frame time interval	T_{FRAME}		0.9995	1.0005	ms
Jitter generated by differential driver					
Full speed					
Next Transition	T_{DJ1}		–3.5	3.5	ns
Paired Transition	T_{DJ2}		–4.0	4.0	ns
Low speed					
Next Transition	T_{DDJ1}		–75	75	ns
Paired Transition	T_{DDJ2}		–45	45	ns
Transmitter EOP pulse width	T_{EOPT}				
Full speed			160	175	ns
Low speed			1.25	1.50	μs
EOP pulse width skew	T_{DEOP}				
Full speed			–2	5	ns
Low speed			–40	100	ns
Differential receiver's allowable jitter					
Full speed					
Next Transition	T_{JR1}		–18.5	18.5	ns
Paired Transition	T_{JR2}		–9	9	ns
Low speed					
Next Transition	T_{UJR1}		–152	152	ns
Paired Transition	T_{UJR2}		–200	200	ns
Receiver EOP pulse width					
Full speed					
Rejection value	T_{EOPR1}		≤ 40		ns
Acceptance value	T_{EOPR2}		> 40		ns
Low speed[Note]					
Rejection value	T_{EOPR1}		≤ 330		ns
Acceptance value	T_{EOPR2}		> 330		ns

Note This applies up until the EOF1 token that defines the end of the Frame in the HUB. The rated Full Speed is applied between EOF1 and EOF2.

CHAPTER 7 TIMING CHARTS

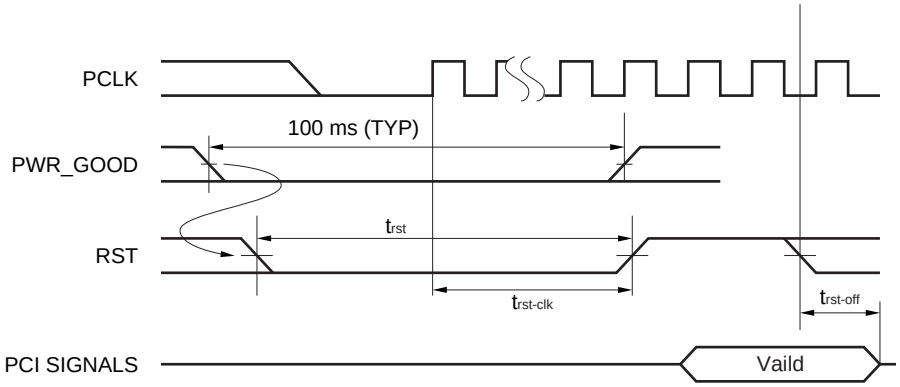
7.1 PCI Clock

Figure 7-1. PCI Clock Waveforms



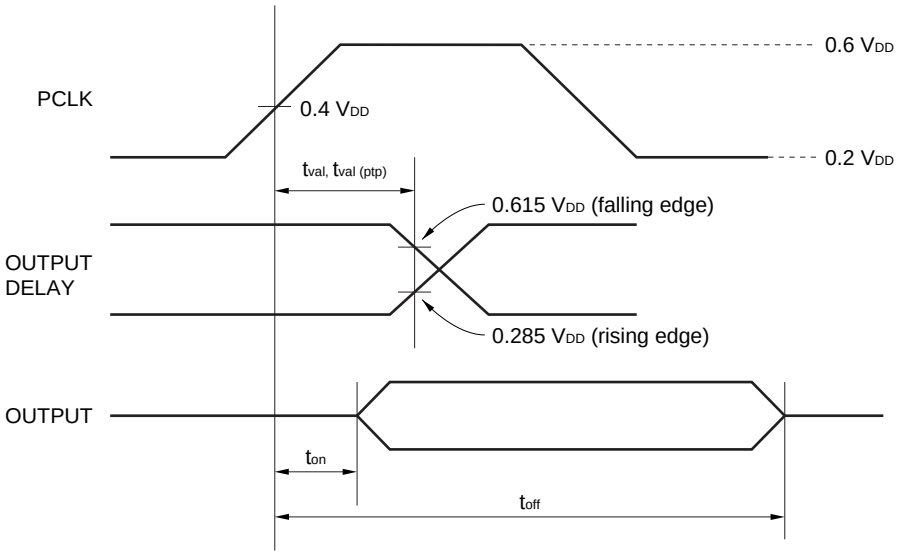
7.2 PCI Reset

Figure 7-2. PCI Reset Waveforms



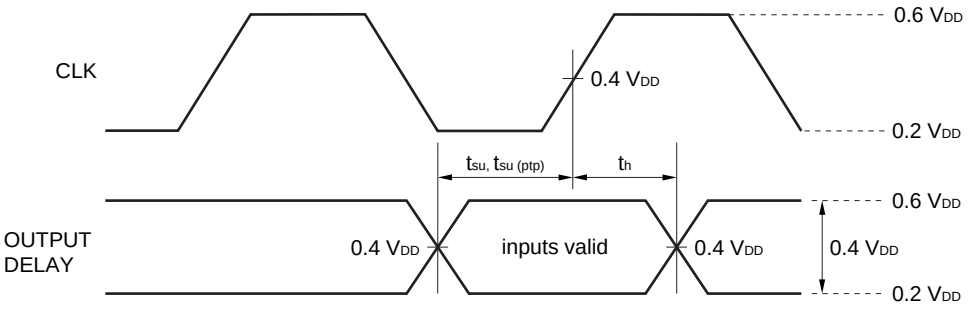
7.3 PCI Output Timing

Figure 7-3. PCI Output Timing



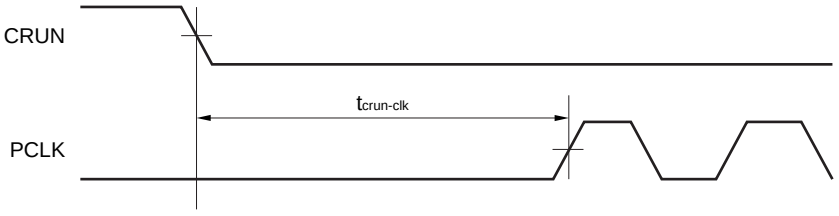
7.4 PCI Input Timing

Figure 7-4. PCI Input Timing



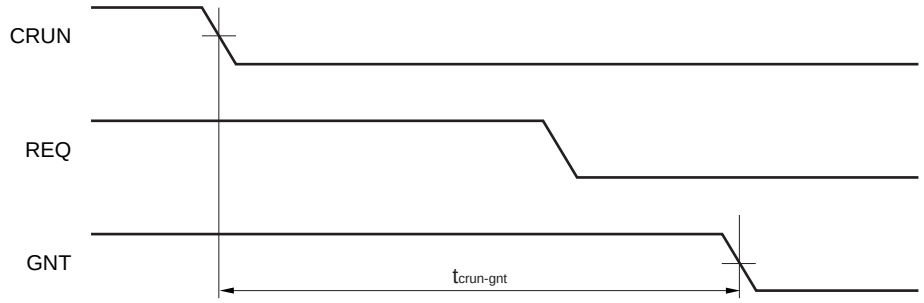
7.5 PCI Clock Reset

Figure 7-5. PCI Clock Reset



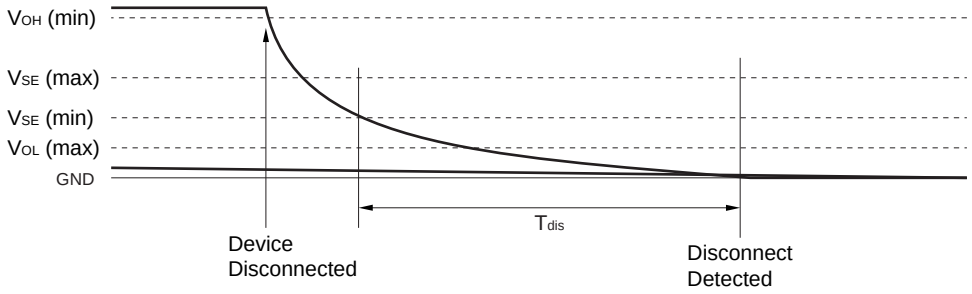
7.6 CRUN vs. GNT

Figure 7-6. CRUN vs. GNT



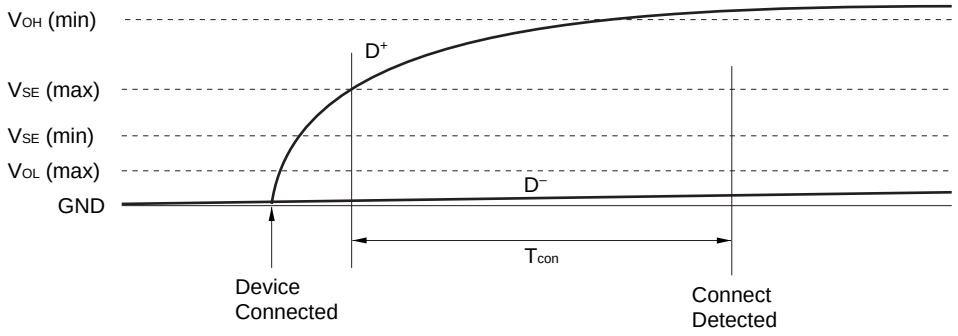
7.7 USB Device Disconnect Detection

Figure 7-7. USB Device Disconnect Detection



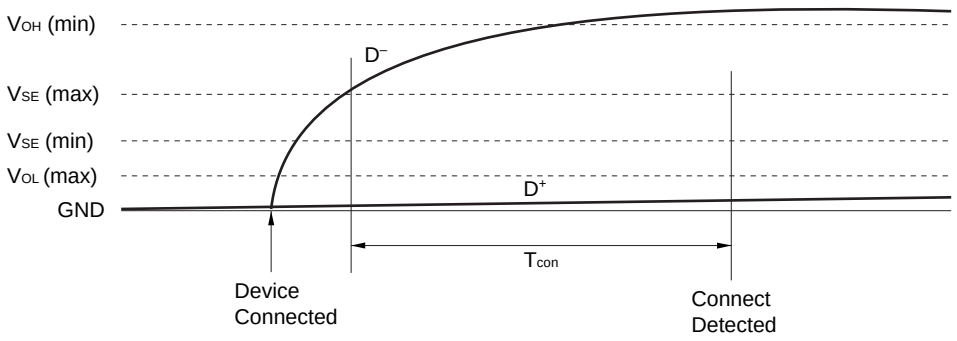
7.8 USB Full Speed Device Connect Detection

Figure 7-8. USB Full Speed Device Connect Detection



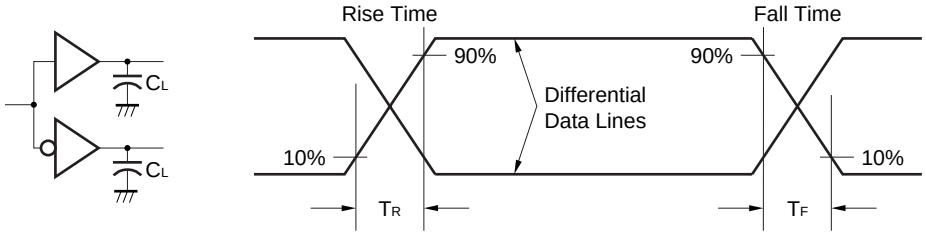
7.9 USB Low Speed Device Connect Detection

Figure 7-9. USB Low Speed Device Connect Detection



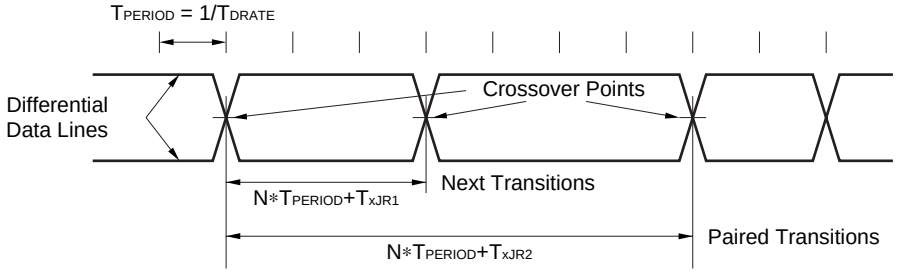
7.10 USB Signal Rise/Fall Timing

Figure 7-10. USB Signal Rise/Fall Timing



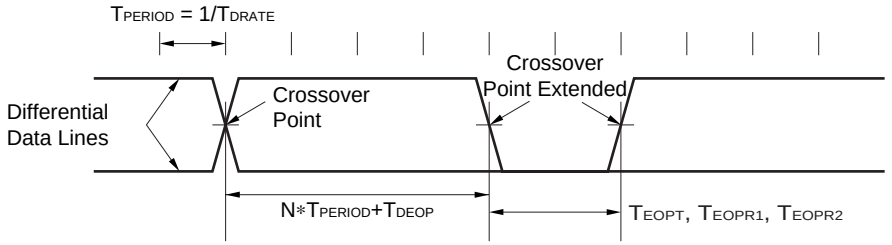
7.11 USB Differential Signal

Figure 7-11. USB Differential Signal



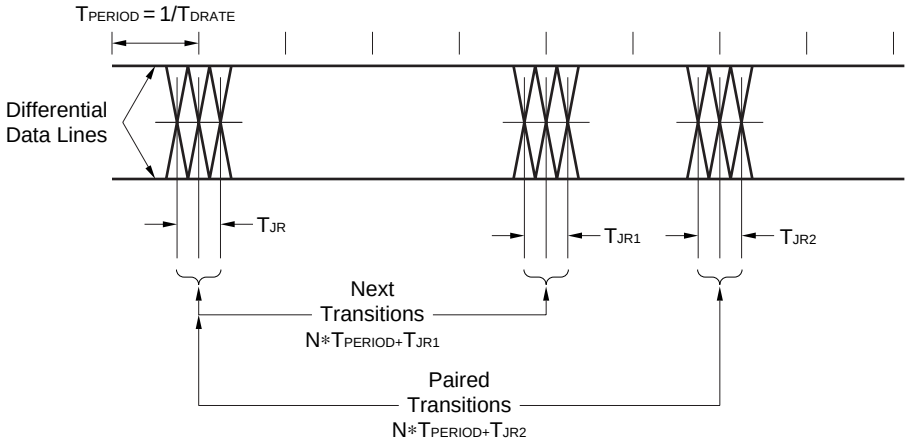
7.12 USB EOP Signal

Figure 7-12. USB EOP Signal



7.13 USB Differential Receiver Allowable Jitter

Figure 7-13. USB Differential Receiver Allowable Jitter Capacitance



[MEMO]

8.1 USB Host Controller Peripheral Circuit Example

This USB HC can be generally divided into four blocks: the PCI interface block, USB interface block, Legacy interface block, and test pin block. Since the PCI interface block complies with the **PCI Local Bus Specification Revision 2.1** and **PCI Mobile Design Guide Revision 1.0**, refer to these specifications before designing external circuits or peripheral circuits. The test pin block should be left with all pins unconnected on the board. The following diagrams show a peripheral circuit example in which this host controller is mounted onto an Add-in Board. The circuits in this example are for reference only: they are not guaranteed as peripheral circuits.

Figure 8-1. Circuit Example of USB Interface Block

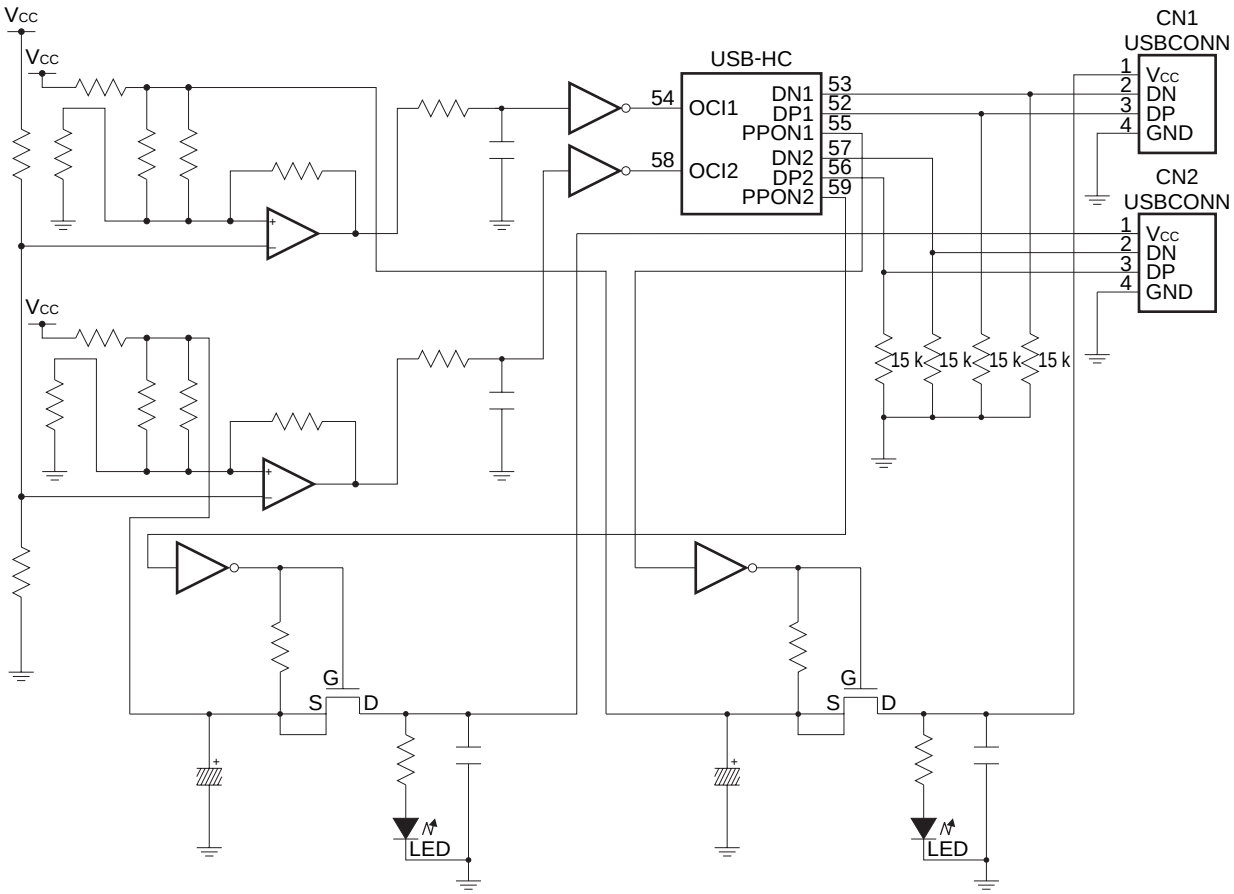
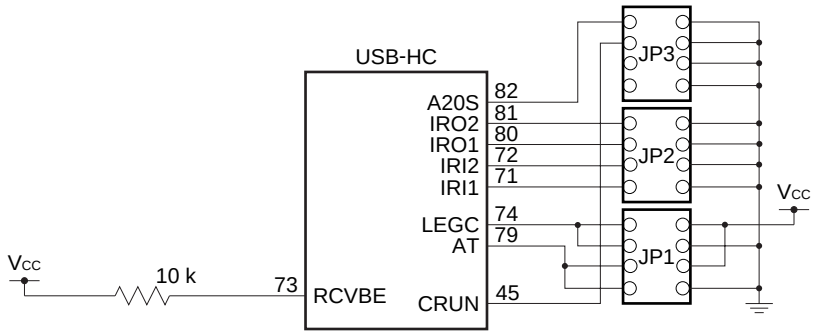


Figure 8-2. Circuit Example of Legacy Interface Block



The jumper settings are shown below.

Table 8-1. Jumper Settings

Pin	No Legacy	Legacy	CLKRUN
A20S	Open	A20S	
IRI1	Low	IRI1	
IRI2	Low	IRI2	
IRO1	Open	IRO1	
IRO2	Open	IRO2	
LEGC	Low	High	
AT	Low	High	
CRUN	Low	Low	CLKRUN#

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