

**TMS626402**  
**2097152-WORD BY 4-BIT BY 2-BANK**  
**SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY**  
 SMOS642A – FEBRUARY 1994 – REVISED JUNE 1995

- Organization . . . 2M x 4 x 2 Banks
- 3.3-V Power Supply (±10% Tolerance)
- Two Banks for On-Chip Interleaving (Gapless Accesses)
- High Bandwidth – Up to 100-MHz Data Rates
- Burst Length Programmable to 1, 2, 4, or 8
- Programmable Output Sequence – Serial or Interleave
- Chip Select and Clock Enable for Enhanced-System Interfacing
- Cycle-by-Cycle DQ-Bus Mask Capability
- Programmable Read Latency From Column Address
- Self-Refresh Capability
- High-Speed, Low-Noise LVTTTL
- Power-Down Mode
- Compatible With JEDEC Standards
- 4K Refresh (Total for Both Banks)
- 2-Bit Prefetch Architecture for High Speed Performance
- Performance Ranges:

	SYNCHRONOUS CLOCK CYCLE TIME	ACTV COMMAND TO READ OR WRITE COMMAND TIME	REFRESH TIME INTERVAL
TMS626402-10	10 ns	30 ns	64 ms
TMS626402-12	12.5 ns	35 ns	64 ms
TMS626402-15	15 ns	40 ns	64 ms

**description**

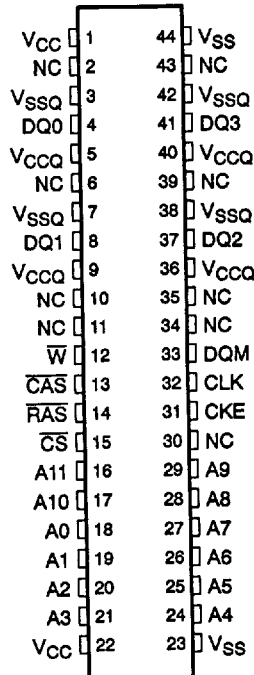
The TMS626402 series are high-speed 16777216-bit synchronous dynamic random-access memories organized as two banks of 2097152 words with four bits per word.

All inputs and outputs of the TMS626402 series are compatible with the low-voltage TTL (LVTTTL) interface.

The synchronous DRAM employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power. All inputs and outputs are synchronized with the CLK input to simplify system design and enhance use with high-speed microprocessors and caches.

The TMS626402 synchronous DRAM is available in a 400-mil, 44-pin surface-mount TSOP (II) package (DGE suffix).

**DGE PACKAGE  
(TOP VIEW)**



**PIN NOMENCLATURE**

A0–A10	Address Inputs
A0–A10	Row Addresses
A0–A9	Column Addresses
A10	Automatic-Precharge Select
A11	Bank Select
$\bar{CAS}$	Column-Address Strobe
CKE	Clock Enable
CLK	System Clock
$\bar{CS}$	Chip Select
DQ0–DQ3	SDRAM Data Input/Data Output
DQM	Data/Output Mask Enable
NC	No External Connect
$\bar{RAS}$	Row-Address Strobe
VCC	Power Supply (3.3 V Typ)
VCCQ	Power Supply for Output Drivers (3.3 V Typ)
VSS	Ground
VSSQ	Ground for Output Drivers
$\bar{W}$	Write Enable

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**operation**

All inputs of the '626402 synchronous DRAM are latched on the rising edge of the system (synchronous) clock. The outputs, DQ0-DQ3, are also referenced to the rising edge of CLK. The '626402 has two banks that are accessed independently. A bank must be activated before it can be accessed (read from or written to). Refresh cycles refresh both banks alternately.

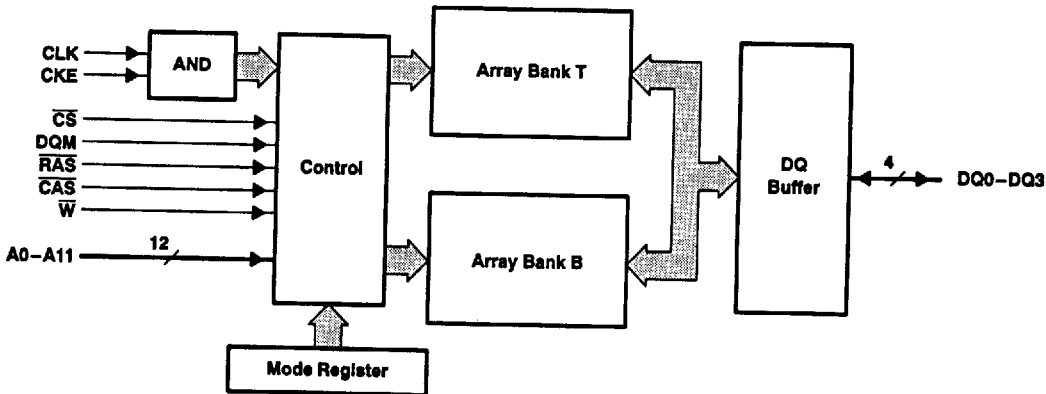
Six basic commands or functions control most operations of the '626402:

- Bank activate/row-address entry
- Column-address entry/write operation
- Column-address entry/read operation
- Bank deactivate
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  (CBR)
- Self-refresh entry

Additionally, operation can be controlled by three methods: using chip select ( $\overline{\text{CS}}$ ) to select/deselect the devices, using DQM to enable/mask the DQ signals on a cycle-by-cycle basis, or using CKE to suspend (or gate) the CLK input. The device contains a mode register that must be programmed for proper operation.

Tables 1 through 3 show the various operations that are available on the '626402. These truth tables identify the commands and/or operations and their respective mnemonics. Each truth table is followed by a legend that explains the abbreviated symbols. An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

**functional block diagram**



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operation (continued)

Table 1. Basic-Command Truth Table†

COMMAND	STATE OF BANK(S)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A11	A10	A9-A0	MNEMONIC
Mode register set	T = deac B = deac	L	L	L	L	X	X	A9=X A8=0 A7=0 A6-A0=V	MRS
Bank deactivate (precharge)	X	L	L	H	L	BS	L	X	DEAC
Deactivate all banks	X	L	L	H	L	X	H	X	DCAB
Bank activate/row-address entry	SB = deac	L	L	H	H	BS	V	V	ACTV
Column-address entry/write operation	SB = actv	L	H	L	L	BS	L	V	WRT
Column-address entry/write operation with autodeactivate	SB = actv	L	H	L	L	BS	H	V	WRT-P
Column-address entry/read operation	SB = actv	L	H	L	H	BS	L	V	READ
Column-address entry/read operation with autodeactivate	SB = actv	L	H	L	H	BS	H	V	READ-P
Burst stop	SB = actv	L	H	H	L	X	X	X	STOP
No operation	X	L	H	H	H	X	X	X	NOOP
Control input inhibit / no operation	X	H	X	X	X	X	X	X	DESL
CBR refresh‡	T = B = deac	L	L	L	H	X	X	X	REFR

† For execution of these commands on cycle n, CKE (n) must be high and satisfy tCESP from power-down exit (PDE), tCES and nCLE from clock-suspend (HOLD) exit, and tCESP and tPC from self-refresh (SLFR) exit. DQM (n) is a don't care.

‡ CBR or self-refresh entry requires that all banks be deactivated or in an idle state prior to the command entry.

Legend:

- L = Logic low
- H = Logic high
- X = Don't care
- V = Valid
- T = Bank T
- B = Bank B
- actv = Activated
- deac = Deactivated
- BS = Logic high to select bank T; logic low to select bank B
- SB = Bank selected by A11 at cycle n

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operation (continued)

**Table 2. CKE-Use Command Truth Table†**

COMMAND	STATE OF BANK(S)	CKE (n-1)	CKE (n)	CS (n)	RAS (n)	CAS (n)	W (n)	MNEMONIC
Self-refresh entry	T = B = deac	H	L	L	L	L	H	SLFR
Power-down entry at n + 1	T = B = no access operation‡	H	L	L	H	H	H	PDE
		H	L	H	X	X	X	PDE
Self-refresh exit	T = B = self refresh	L	H	L	H	H	H	—
		L	H	H	X	X	X	—
Power-down exit	T = B = power down	L	H	X	X	X	X	—
CLK suspend at n + 1	T or B = access operation‡	H	L	X	X	X	X	HOLD
CLK suspend exit at n + 1	T or B = access operation‡	L	H	X	X	X	X	—

† For execution of these commands, A0-A11 (n) and DQM (n) are don't cares.

‡ An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

Legend:

- n = CLK cycle number
- L = Logic low
- H = Logic high
- X = Don't care
- T = Bank T
- B = Bank B
- deac = Deactivated



operation (continued)

Table 3. DQM-Use Command Truth Table<sup>†</sup>

COMMAND	STATE OF BANK(S)	DQM (n)	DATA IN (n)	DATA OUT (n+2)	MNEMONIC
—	T = deac and B = deac	X	N/A	HI-Z	—
—	T = actv and B = actv (no access operation) <sup>‡</sup>	X	N/A	HI-Z	—
Data-in enable	T = write or B = write	L	V	N/A	ENBL
Data-in mask	T = write or B = write	H	M	N/A	MASK
Data-out enable	T = read or B = read	L	N/A	V	ENBL
Data-out mask	T = read or B = read	H	N/A	HI-Z	MASK

<sup>†</sup> For execution of these commands, CKE (n) must be high and satisfy t<sub>CESP</sub> from power-down exit (PDE), t<sub>CES</sub> and nCLE from clock-suspend (HOLD) exit, and t<sub>CESP</sub> and t<sub>RC</sub> from self-refresh (SLFR) exit.  $\overline{CS}$  (n),  $\overline{RAS}$  (n),  $\overline{CAS}$  (n),  $\overline{W}$  (n), and A0-A11 (n) are don't cares.

<sup>‡</sup> An access operation refers to any READ (READ-P) or WRT (WRT-P) command in progress at cycle n. Access operations include the cycle upon which the READ (READ-P) or WRT (WRT-P) command is entered and all subsequent cycles through the completion of the access burst.

Legend:

- n = CLK cycle number
- L = Logic low
- H = Logic high
- X = Don't care
- V = Valid
- M = Masked input data
- N/A = Not applicable
- T = Bank T
- B = Bank B
- actv = Activated
- deac = Deactivated
- write = Activated and accepting data in on cycle n
- read = Activated and delivering data out on cycle n + 2

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**burst sequence**

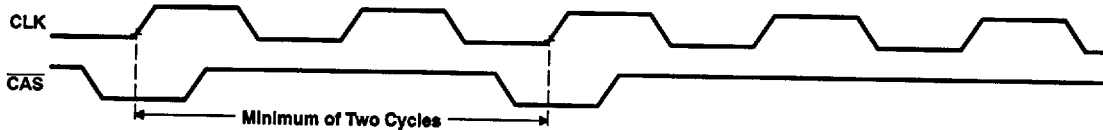
All data for the '626402 is written or read in a burst fashion; that is, a single starting address is entered into the device and the '626402 internally accesses a sequence of locations based on that starting address. Some of the subsequent accesses after the first can be at preceding as well as succeeding column addresses, depending on the starting address entered. This sequence can be programmed to follow either a serial burst or an interleave burst (see Tables 4 through 6). The length of the burst sequence can be user programmed to be either 1-, 2-, 4-, or 8-bit accesses. After a read burst is completed (as determined by the programmed burst length), the outputs are in the high-impedance state until the next read access is initiated.

**Table 4. 2-Bit Burst Sequences**

	INTERNAL COLUMN ADDRESS A0			
	DECIMAL		BINARY	
	START	2ND	START	2ND
Serial	0	1	0	1
	1	0	1	0
Interleave	0	1	0	1
	1	0	1	0

**Table 5. 4-Bit Burst Sequences**

	INTERNAL COLUMN ADDRESS A1-A0							
	DECIMAL				BINARY			
	START	2ND	3RD	4TH	START	2ND	3RD	4TH
Serial	0	1	2	3	00	01	10	11
	1	2	3	0	01	10	11	00
	2	3	0	1	10	11	00	01
	3	0	1	2	11	00	01	10
Interleave	0	1	2	3	00	01	10	11
	1	0	3	2	01	00	11	10
	2	3	0	1	10	11	00	01
	3	2	1	0	11	10	01	00



NOTE: For burst sequence of one, subsequent read or write commands must be done at least two clock cycles from initial read or write command (see timing diagram above).

**Figure 1. Subsequent Read or Write CMD for BL = 1**



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**burst sequence (continued)**

**Table 6. 8-Bit Burst Sequences**

	INTERNAL COLUMN ADDRESS A2-A0															
	DECIMAL								BINARY							
	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH	START	2ND	3RD	4TH	5TH	6TH	7TH	8TH
Serial	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	2	3	4	5	6	7	0	001	010	011	100	101	110	111	000
	2	3	4	5	6	7	0	1	010	011	100	101	110	111	000	001
	3	4	5	6	7	0	1	2	011	100	101	110	111	000	001	010
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	6	7	0	1	2	3	4	101	110	111	000	001	010	011	100
	6	7	0	1	2	3	4	5	110	111	000	001	010	011	100	101
	7	0	1	2	3	4	5	6	111	000	001	010	011	100	101	110
Interleave	0	1	2	3	4	5	6	7	000	001	010	011	100	101	110	111
	1	0	3	2	5	4	7	6	001	000	011	010	101	100	111	110
	2	3	0	1	6	7	4	5	010	011	000	001	110	111	100	101
	3	2	1	0	7	6	5	4	011	010	001	000	111	110	101	100
	4	5	6	7	0	1	2	3	100	101	110	111	000	001	010	011
	5	4	7	6	1	0	3	2	101	100	111	110	001	000	011	010
	6	7	4	5	2	3	0	1	110	111	100	101	010	011	000	001
	7	6	5	4	3	2	1	0	111	110	101	100	011	010	001	000

**latency**

The beginning data-output cycle of a read burst can be programmed to occur 1, 2, or 3 CLK cycles after the read command (see setting the mode register). This feature allows the user to adjust the '626402 to operate in accordance with the system's capability to latch the data output from the '626402. The delay between the READ command and the beginning of the output burst is known as read latency (also known as CAS latency). After the initial output cycle begins, the data burst occurs at the CLK frequency without any intervening gaps. Use of minimum read latencies is restricted based on the particular maximum frequency rating of the '626402.

There is no latency for data-in cycles (write latency). The first data-in cycle of a write burst is entered at the same rising edge of CLK on which the WRT command is entered. The write latency is fixed and not determined by the mode-register contents.

**two-bank operation**

The '626402 contains two independent banks that can be accessed individually or in an interleaved fashion. Each bank must be activated with a row address before it can be accessed. Each bank must then be deactivated before it can be activated again with a new row address. The bank-activate/row-address-entry command (ACTV) is entered by holding  $\overline{RAS}$  low,  $\overline{CAS}$  high,  $\overline{W}$  high, and A11 valid on the rising edge of CLK. A bank can be deactivated either automatically during a READ (READ-P) or a WRT (WRT-P) command or by use of the deactivate-bank (DEAC) command. Both banks can be deactivated at once by use of the DCAB command (see Table 1 and the bank deactivation description).

**two-bank row-access operation**

The two-bank feature allows the user to access information on random rows at a higher rate of operation than is possible with a standard DRAM. This is accomplished by activating one bank with a row address, and while the data stream is being accessed to/from that bank, activating the second bank with another row address.



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**two-bank row-access operation (continued)**

When the data stream to/from the first bank is complete, the data stream to/from the second bank can begin without interruption. After the second bank is activated, the first bank can be deactivated to allow the entry of a new row address for the next round of accesses. In this manner, operation can continue in an interleaved fashion. Figure 27 is an example of two-bank row interleaving with automatic deactivate for the case of a read latency of 3 and a burst length of 8.

**two-bank column-access operation**

The availability of two banks allows the access of data from random starting columns between banks at a higher rate of operation. After activating each bank with a row address (ACTV command), A11 can be used to alternate READ or WRT commands between the banks to provide gapless accesses at the CLK frequency, provided all specified timing requirements are met. Figure 28 is an example of two-bank column interleaving with a read latency of 3 and a burst length of 2.

**bank deactivation (precharge)**

Both banks can be simultaneously deactivated (placed in precharge) by using the DCAB command. A single bank can be deactivated by using the DEAC command. The DEAC command is entered identically to the DCAB command except that A10 must be low and A11 selects the bank to be precharged as shown in Table 1. A bank can also be deactivated automatically by using A10 during a READ or WRT command. If A10 is held high during the entry of a READ or WRT command, the accessed bank (selected by A11) automatically deactivates upon completion of the access burst. If A10 is held low during READ or WRT command entry, that bank remains active following the burst. The READ and WRT commands with automatic deactivation are denoted as READ-P and WRT-P.

**chip select ( $\overline{CS}$ )**

$\overline{CS}$  can be used to select or deselect the '626402 command entry, which might be required for multiple memory-device decoding. If  $\overline{CS}$  is held high on the rising edge of CLK (DESL command), the device does not respond to  $\overline{RAS}$ ,  $\overline{CAS}$ , or  $\overline{W}$  until the device is selected again. Device select is accomplished by holding  $\overline{CS}$  low on the rising edge of CLK. Any other valid command can be entered simultaneously on the same rising CLK edge of the select operation. The device can be selected/deselected on a cycle-by-cycle basis (see Tables 1 and 2). The use of  $\overline{CS}$  does not affect an access burst that is in progress; the DESL command can only restrict  $\overline{RAS}$ ,  $\overline{CAS}$ , and  $\overline{W}$  input to the '626402.

**data/output mask**

Masking of individual data cycles within a burst sequence can be accomplished by use of the MASK command (see Table 3). If DQM is held high on the rising edge of CLK during a write burst, the incident data word (referenced to the same rising edge of CLK) on DQ0–DQ3 is ignored. If DQM is held high on the rising edge of CLK for a read burst, DQ0–DQ3 referenced to the second rising edge of CLK are in the high-impedance state. The application of DQM to data output cycles (READ burst) involves a latency of two CLK cycles, but the application of DQM to data-in cycles (WRITE burst) has no latency. The MASK command (or its opposite, the ENBL command) is performed on a cycle-by-cycle basis, allowing the user to gate any individual data cycle or cycles within either a read- or a write-burst sequence. Figure 31 shows an example of data/output masking.

NOTE: Data masking using DQM input is not supported when the mode register is set for read latency of one and burst length of one. If the mode register is in this mode, the DQM pin should be held low.

**CLK suspend/power-down mode**

For normal device operation, CKE should be held high to enable CLK. If CKE goes low during the execution of a READ (READ-P) or WRT (WRT-P) operation, the state of the DQ bus at the immediate next rising edge of CLK is frozen at its current state, and no further inputs are accepted until CKE is returned high.



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### CLK suspend/power-down mode (continued)

This CLK suspend/power-down mode is known as a CLK suspend operation, and its execution is denoted as a HOLD command. The device resumes operation from the point at which it was placed in suspension, beginning with the second rising edge of CLK after CKE is returned high.

If CKE is brought low when no READ (READ-P) or WRT (WRT-P) command is in progress, the device enters power-down mode. If both banks are deactivated when power-down mode is entered, power consumption is reduced to the minimum. Power-down mode can be used during row-active or CBR-refresh periods to reduce input-buffer power. After power-down mode has been entered, no further inputs are accepted until CKE returns high. To ensure data in the device remains valid during the power-down mode, the self-refresh command (SLRF) must be executed concurrently with the power-down entry command (PDE). When exiting power-down mode, new commands can be entered on the first CLK edge after CKE returns high, provided that the setup time ( $t_{CESP}$ ) is satisfied. Table 2 shows the command configuration for a CLK suspend/power-down operation, and Figures 18 and 19 show an example of the procedure.

### setting the mode register

The '626402 contains a mode register that the user should program with the read latency, the burst type, and the burst length. This is accomplished by executing an MRS command with the information entered on address lines A0–A8. A logic 0 should always be entered on A7 and A8, but A9–A11 are don't-care entries for the '626402. Figure 2 shows the valid combinations for a successful MRS command. Only valid addresses allow the mode register to be changed. If the addresses are not valid, the previous contents of the mode register remain unaffected. The MRS command is executed by holding RAS, CAS, and  $\bar{W}$  low, and the input-mode word valid on A0–A8 on the rising edge of CLK (see Table 1). The MRS command can be executed only when both banks are deactivated.

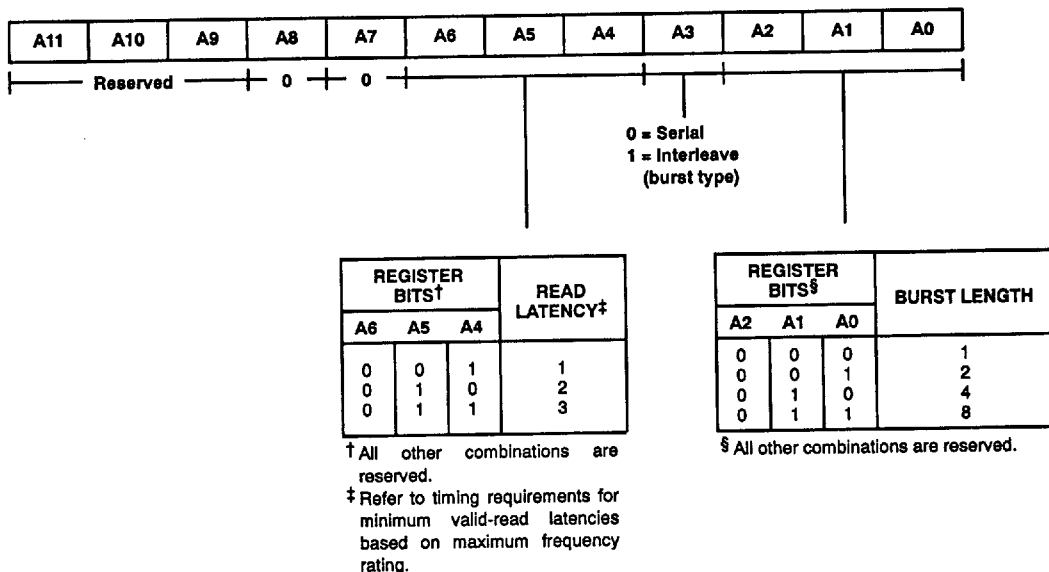


Figure 2. Mode-Register Programming

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**refresh**

The '626402 must be refreshed at intervals not exceeding  $t_{REF}$  (see timing requirements) or data cannot be retained. Refresh can be accomplished by performing a read or write access to every row in both banks, by performing 4096  $\overline{CAS}$ -before- $\overline{RAS}$  (REFR) commands, or by placing the device in self refresh. Regardless of the method used, refresh must be accomplished before  $t_{REF}$  has expired.

**$\overline{CAS}$ -before- $\overline{RAS}$  (CBR) refresh**

Before performing a  $\overline{CAS}$ -before- $\overline{RAS}$  refresh, both banks must be deactivated (placed in precharge). To enter a REFR command,  $\overline{RAS}$  and  $\overline{CAS}$  must be low and  $\overline{W}$  must be high upon the rising edge of CLK (see Table 1). The refresh address is generated internally such that after 4096 REFR commands, both banks of the '626402 are refreshed. The external address and bank select (A11) are ignored. The execution of a REFR command automatically deactivates both banks upon completion of the internal CBR cycle. This allows consecutive REFR-only commands to be executed, if desired, without any intervening DEAC commands. The REFR commands do not necessarily have to be consecutive, but all 4096 must be completed before  $t_{REF}$  expires.

**self refresh**

To enter self refresh, both banks of the '626402 must first be deactivated and a SLFR command must be executed (see Table 2). The SLFR command is identical to the REFR command except that  $\overline{CKE}$  is low. For proper entry of the SLFR command,  $\overline{CKE}$  is brought low for the same rising edge of CLK that  $\overline{RAS}$  and  $\overline{CAS}$  are low and  $\overline{W}$  is high.  $\overline{CKE}$  must be held low to stay in self-refresh mode. In the self-refresh mode, all refreshing signals are generated internally for both banks with all external signals (except  $\overline{CKE}$ ) being ignored. Data can be retained by the device automatically for an indefinite period when power is maintained (consumption is reduced to a minimum). To exit self-refresh mode,  $\overline{CKE}$  must be brought high. New commands are issued after  $t_{RC}$  has expired. If CLK is made inactive during self refresh, it must be returned to an active and stable condition before  $\overline{CKE}$  is brought high to exit self refresh (see Figure 21).

Upon exiting self-refresh, the normal refresh scheme must begin immediately. If the burst-refresh scheme is used, 4096 REFR commands must be executed before continuing with normal device operations. If a distributed-refresh scheme utilizing CBR is used (e.g., two rows every 32  $\mu s$ ), the first set of refreshes must be performed before continuing with normal device operation. This ensures that the SDRAM is fully refreshed.

**Interrupted bursts**

A read or write can be interrupted before the burst sequence has been completed with no adverse effects to the operation. This is accomplished by entering certain superseding commands as listed in Tables 7 and 8, provided that all timing requirements are met. The command interrupting either a read or write burst must be entered only on an even number of cycles (2n rule) from the initial burst command (nCCD). nCCD is defined as the number of clock cycles from the initial command to the interrupting command. In the case when the number of clock cycles between a read/write command and the following command is greater than the burst length, the "2n rule" and nCCD does not apply. A DEAC command is considered an interrupt only if it is issued to the same bank as the preceding READ or WRITE command. The interruption of READ-P and WRT-P operations is not supported.

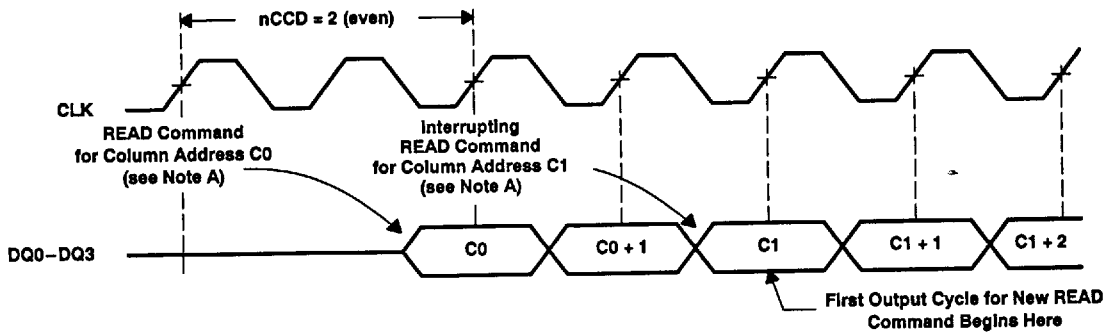


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Interrupted bursts (continued)

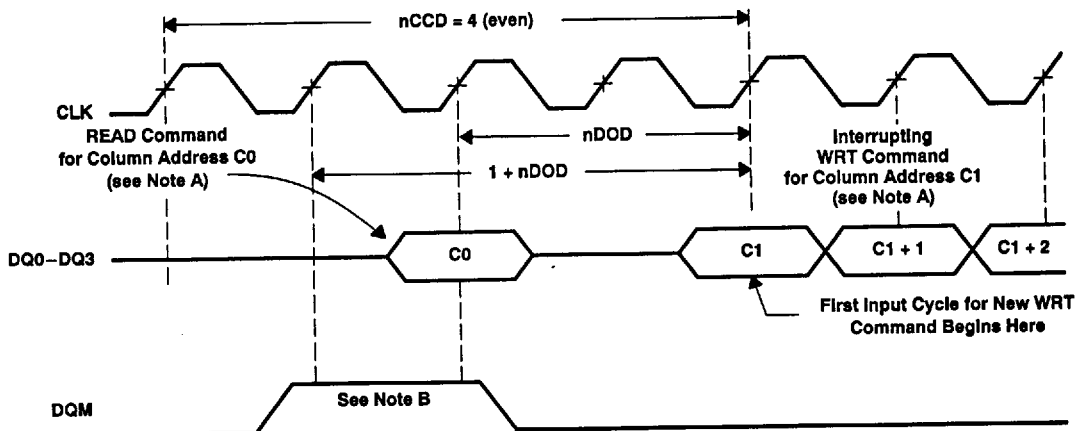
Table 7. Read-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING READ BURST
DEAC, DCAB	The DQ bus is placed in the high-impedance state when nHZP cycles are satisfied or upon completion of the read burst, whichever occurs first (see Figures 5 and 21).
WRT, WRT-P	The WRT command immediately supersedes the read burst in progress, but DQM must be high nDOD+1 and nDOD cycles previous to the WRT (WRT-P) command (see Figure 4).
READ, READ-P	Current output cycles continue until the programmed latency from the superseding READ (READ-P) command is met, and new output cycles begin (see Figure 3).
STOP	The DQ bus is placed in the high-impedance state two clock cycles after the stop command is entered or upon completion of the read burst, whichever occurs first. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 5).



NOTE A: For the purposes of this example, read latency = 2 and burst length > 2.

Figure 3. Read Burst Interrupted by Read Command

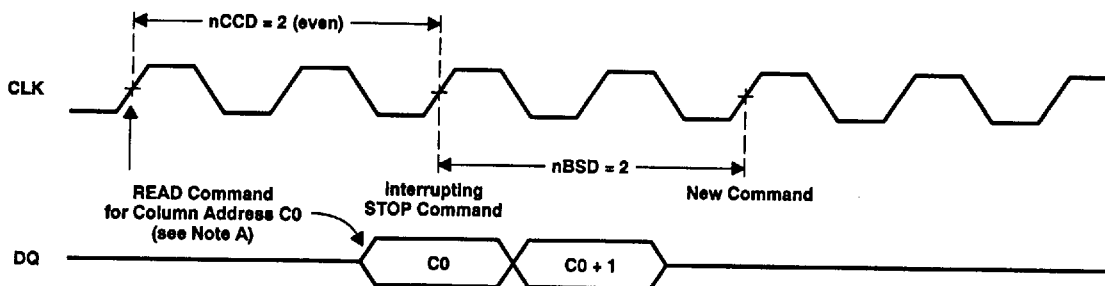


NOTES: A. For the purposes of this example, read latency = 2 and burst length > 2.  
 B. DQM is held high for 2 CLK cycles (2 rising edges). DQM is held high for nDOD+1 to mask out bit prior to interrupting WRT command. DQM is held high for nDOD as specified spec.

Figure 4. Read Burst Interrupted by Write Command

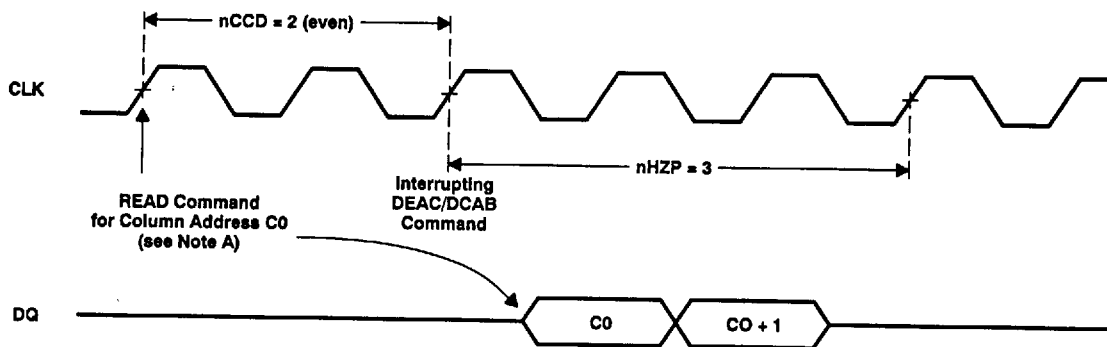


**Interrupted bursts (continued)**



NOTE A: For this example, read latency = 2 and burst length > 2.

**Figure 5. Read Burst Interrupted by STOP Command**



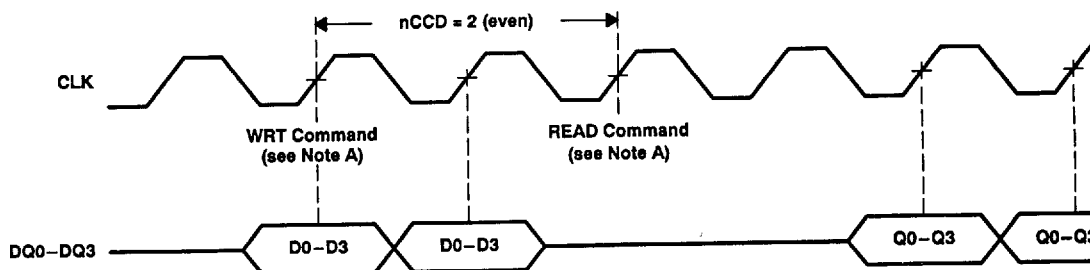
NOTE A: For this example, read latency = 3 and burst length > 2.

**Figure 6. Read Burst Interrupted by DEAC Command**

Interrupted bursts (continued)

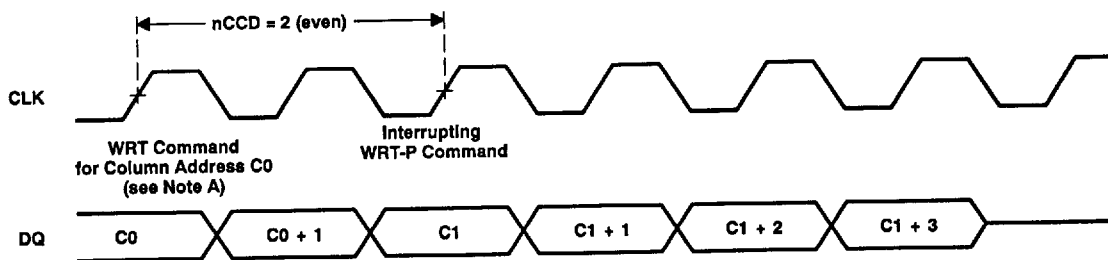
Table 8. Write-Burst Interruption

INTERRUPTING COMMAND	EFFECT OR NOTE ON USE DURING WRITE BURST
DEAC, DCAB	The DEAC/DCAB command immediately supersedes the write burst in progress. DQM must be used to mask the DQ bus such that the write-recovery specification ( $t_{RWL}$ ) is not violated by the interrupt (see Figure 10).
WRT, WRT-P	The new WRT (WRT-P) command and data immediately supersedes the write burst in progress (see Figure 8).
READ, READ-P	Data in on previous cycle is written. No further data input is accepted (see Figure 7).
STOP	The data on the input pins at the time of the burst STOP command is not written, and no further data is accepted. The bank remains active. A new read or write command cannot be entered for at least two cycles after the STOP command (see Figure 9).



NOTE A: For this example, read latency = 2 and burst length > 2.

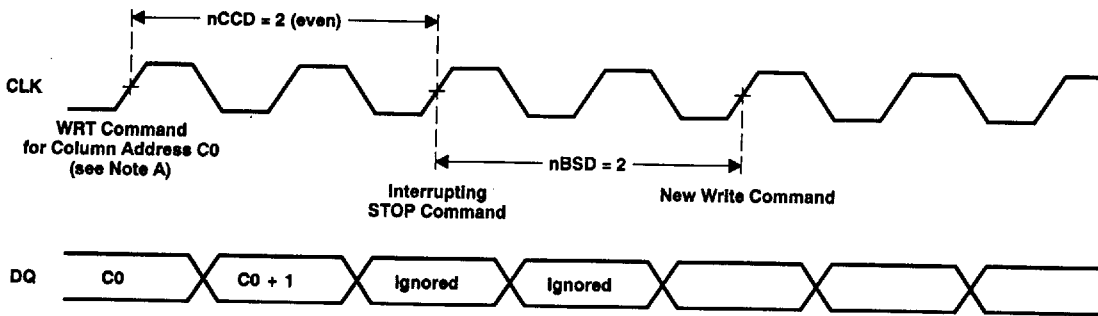
Figure 7. Write Burst Interrupted by Read Command



NOTE A: For this example, burst length > 2.

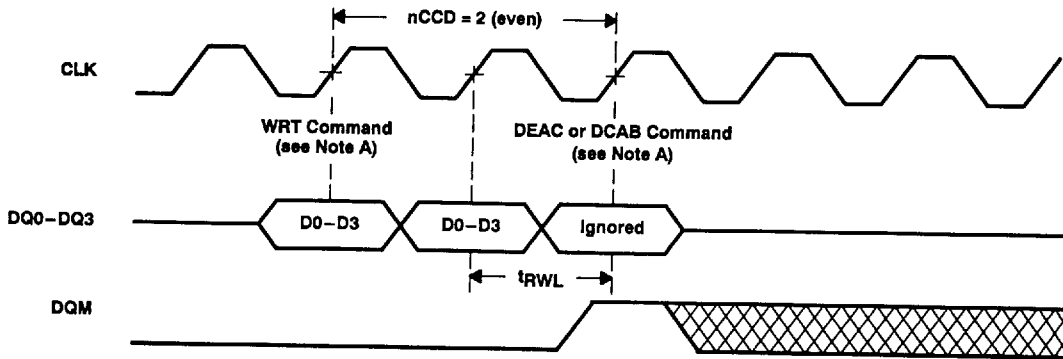
Figure 8. Write Burst Interrupted by Write Command

**Interrupted bursts (continued)**



NOTE A: For this example, burst length > 2.

**Figure 9. Write Burst Interrupted by STOP Command**



NOTE A: For this example, read latency = 2, burst length > 2, and  $t_{CK} = t_{RWL}$ .

**Figure 10. Write Burst Interrupted by DEAC/DCAB Command**

**power up**

Device initialization should be performed after a power up to the full  $V_{CC}$  level. After power is established, a 200- $\mu$ s interval is required (with no inputs other than CLK). After this interval, both banks of the device must be deactivated. Eight REFR commands must be performed, and the mode register must be set to complete the device initialization.

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	- 0.5 V to 4.6 V
Supply voltage range for output drivers, $V_{CCQ}$ .....	- 0.5 V to 4.6 V
Voltage range on any pin (see Note 1) .....	- 0.5 V to 4.6 V
Short-circuit output current .....	50 mA
Power dissipation .....	1 W
Operating free-air temperature range, $T_A$ .....	0°C to 70°C
Storage temperature range, $T_{stg}$ .....	- 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to  $V_{SS}$ .

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	3	3.3	3.6	V
$V_{CCQ}$ Supply voltage for output drivers	3	3.3	3.6	V
$V_{SS}$ Supply voltage		0		V
$V_{SSQ}$ Supply voltage for output drivers		0		V
$V_{IH}$ High-level input voltage	2		$V_{CC} + 0.3$	V
$V_{IL}$ Low-level input voltage	- 0.3		0.8	V
$T_A$ Operating free-air temperature	0		70	°C



electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS	'626402-10		'626402-12		'626402-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub> High-level output voltage	I <sub>OH</sub> = -2 mA	2.4	0.4	2.4	0.4	2.4	0.4	V
V <sub>OL</sub> Low-level output voltage	I <sub>OL</sub> = 2 mA							V
I <sub>I</sub> Input current (leakage)	0 V ≤ V <sub>I</sub> ≤ V <sub>CC</sub> + 0.3 V, All other pins = 0 V to V <sub>CC</sub>		±10		±10		±10	µA
I <sub>O</sub> Output current (leakage)	0 V ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.3 V, Output disabled		±10		±10		±10	µA
I <sub>CC1</sub> Average read or write current	t <sub>RC</sub> = MIN, t <sub>CK</sub> = MIN, Read latency = 3	1 bank active		90	80	70		
		Burst length = 1 or 2						
		Burst length = 4 or 8		110	100	90		
		2 banks active interleaving		150	120	100		
I <sub>CC2</sub> Standby current	Both banks deactivated One or both banks active	C <sub>KE</sub> = V <sub>IH</sub> . See Note 3		16	16	16		
		C <sub>KE</sub> = V <sub>IL</sub>		2	2	2		
		C <sub>KE</sub> = 0 V (CMOS)		1	1	1		
		C <sub>KE</sub> = V <sub>IL</sub>		6	6	6		
I <sub>CC3</sub> Consecutive CBR commands	t <sub>RC</sub> = MIN			90	80	70		
		ACTV not allowed, 2-bank interleaved		70	60	50		
I <sub>CC4</sub> Burst current, gapless burst	t <sub>CK</sub> = MIN, Read latency = 1 Read latency = 2 Read latency = 3			100	90	80		
				140	120	100		
				2	2	2		
I <sub>CC6</sub> Self-refresh current	C <sub>KE</sub> = V <sub>IL</sub> C <sub>KE</sub> = 0 V (CMOS)			1	1	1		
				1	1	1		

NOTES: 2. All specifications apply to the device after power-up initialization.  
3. All control and address inputs must be stable and valid.



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capacitance over recommended ranges of supply voltage and operating free-air temperature,  $f = 1$  MHz (see Note 4)

	MIN	MAX	UNT
$C_i(S)$ Input capacitance, CLK		7	pF
$C_i(AC)$ Input capacitance, A0–A11, $\overline{CS}$ , DQM, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{W}$		5	pF
$C_i(E)$ Input capacitance, $\overline{CKE}$		5	pF
$C_o$ Output capacitance		8	pF

NOTE 4:  $V_{CC} = 3.3 \pm 0.3$  V and bias on pins under test is 0 V.

ac timing requirements over recommended ranges of supply voltage and operating free-air temperature †‡

		'626402-10		'626402-12		'626402-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{CK}$	Cycle time, CLK (system clock)	Read latency = 1	30	36	40	ns		
		Read latency = 2	15	18	20			
		Read latency = 3	10	12	15			
$t_{CKH}$	Pulse duration, CLK (system clock) high	3	3.5	4	ns			
$t_{CKL}$	Pulse duration, CLK (system clock) low	3	3.5	4	ns			
$t_{AC}$	Access time, CLK $\uparrow$ to data out (see Note 5)	Read latency = 1	29	33	38	ns		
		Read latency = 2	14	15	18			
		Read latency = 3	9	10	12			
$t_{OH}$	Hold time, CLK $\uparrow$ to data out	3	3	3	ns			
$t_{LZ}$	Delay time, CLK to DQ in the low-impedance state (see Note 6)	0	0	0	ns			
$t_{HZ}$	Delay time, CLK to DQ in the high-impedance state (see Note 7)	Read latency = 1	20	20	20	ns		
		Read latency = 2	12	13	14			
		Read latency = 3	9	10	11			
$t_{DS}$	Setup time, data in	2	2	2	ns			
$t_{AS}$	Setup time, address	2	2	2	ns			
$t_{CS}$	Setup time, control input ( $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{W}$ , DQM)	2	2	2	ns			
$t_{CES}$	Setup time, $\overline{CKE}$ (suspend entry/exit, power-down entry)	2	2	2	ns			
$t_{CESP}$	Setup time, $\overline{CKE}$ (power-down/self-refresh exit) (see Note 8)	8	10	12	ns			
$t_{DH}$	Hold time, data in	2	3	4	ns			
$t_{AH}$	Hold time, address	2	3	4	ns			
$t_{CH}$	Hold time, control input ( $\overline{CS}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{W}$ , DQM)	2	3	4	ns			
$t_{CEH}$	Hold time, $\overline{CKE}$	2	3	4	ns			
$t_{RC}$	REFR command to ACTV, MRS, REFR or SLFR command; ACTV command to ACTV, MRS, REFR or SLFR command; Self-refresh exit to ACTV, MRS, REFR or SLFR command	100	110	125	ns			

† See Parameter Measurement Information for load circuits

‡ All references are made to the rising transition of CLK, unless otherwise noted.

- NOTES: 5.  $t_{AC}$  is referenced from the rising transition of CLK that is previous to the data-out cycle. For example, the first data-out  $t_{AC}$  is referenced from the rising transition of CLK that is read latency – 1 cycles after the READ command. An access time is measured at output reference level 1.4 V.
6.  $t_{LZ}$  is measured from the rising transition of CLK that is read latency – 1 cycles after the READ command.
7.  $t_{HZ}$  (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
8. If  $t_{CESP} > t_{CK}$ , NOOP or DESL commands must be entered until  $t_{CESP}$  is met. CLK must be active and stable (if CLK was turned off for power down) before  $\overline{CKE}$  is returned high.



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ac timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)<sup>†‡</sup>

		'626402-10		'626402-12		'626402-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RAS</sub>	ACTV command to DEAC or DCAB command	60	100 000	70	100 000	80	100 000	ns
t <sub>RCD</sub>	ACTV command to READ or WRT command	30		35		40		ns
t <sub>RP</sub>	DEAC or DCAB command to ACTV, MRS, SLFR, or REFR command	40		40		45		ns
t <sub>APR</sub>	Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command	t <sub>RP</sub> + (nEP × t <sub>CK</sub> )						ns
t <sub>APW</sub>	Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command (see Note 10)	Burst length = 1	1 clock+60	1 clock+60	1 clock+75			ns
		Burst length > 1	60	60	75			
t <sub>RWL</sub>	Final data in to DEAC or DCAB command (see Note 11)	Burst length = 1	1 clock+20	1 clock+20	1 clock+30			ns
		Burst length > 1	20	20	30			
t <sub>RRD</sub>	ACTV command for one bank to ACTV command for the other bank	20		25		30		ns
t <sub>T</sub>	Transition time, all inputs (see Note 9)	1	5	1	5	1	5	ns
t <sub>REF</sub>	Refresh interval	64		64		64		ms

<sup>†</sup> See Parameter Measurement Information for load circuits

<sup>‡</sup> All references are made to the rising transition of CLK, unless otherwise noted.

NOTES: 9. Transition time, t<sub>T</sub>, is measured between V<sub>IH</sub> and V<sub>IL</sub>.

10. for BL=1 only

SPEED

-10, -12 = t<sub>APW</sub> is 60 ns from first unsuspended clock edge after last data in

-15 = t<sub>APW</sub> is 80 ns from first unsuspended clock edge after last data in

11. for BL = 1 only

SPEED

-10, -12 = t<sub>RWL</sub> is 20 ns from first unsuspended clock edge after last data in

-15 = t<sub>RWL</sub> is 30 ns from first unsuspended clock edge after last data in



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**clock timing requirements over recommended ranges of supply voltage and operating free-air temperature†**

		'626402-10		'626402-12		'626402-15		UNIT‡
		MIN	MAX	MIN	MAX	MIN	MAX	
nEP	Final data out to DEAC or DCAB command	Burst length = 1, Read latency = 1		1	1	1	1	cycles
		Burst length = 1, Read latency = 2		0	0	0	0	
		Burst length = 1, Read latency = 3		-1	-1	-1	-1	
		Burst length > 1, Read latency = 1		0	0	0	0	cycles
		Burst length > 1, Read latency = 2		-1	-1	-1	-1	
		Burst length > 1, Read latency = 3		-2	-2	-2	-2	
nHZP	DEAC or DCAB interrupt of data out burst to DQ in the high-impedance state (see Note 12)	Read latency = 1		1	1	1	1	cycles
		Read latency = 2		2	2	2	2	
		Read latency = 3		3	3	3	3	
nCCD	READ or WRT command to interrupting STOP, READ, WRT, DEAC, or DCAB command (l = 1, 2, 3, . . .) (see Note 13)	2l		2l	2l	2l	2l	cycles
nCWL	Final data in to READ or WRT command in either bank	Burst length = 1		2	2	2	2	cycles
		Burst length > 1		1	1	1	1	cycles
nWCD	WRT command to first data in	0	0	0	0	0	0	cycles
nDID	ENBL or MASK command to data in	0	0	0	0	0	0	cycles
nDOD	ENBL or MASK command to data out	2	2	2	2	2	2	cycles
nCLE	HOLD command to suspended CLK edge; HOLD operation exit to entry of any command	1	1	1	1	1	1	cycles
nRSA	MRS command to ACTV, REFR, SLFR, or MRS command	2		2		2		cycles
nCDD	DESL command to control input inhibit	0	0	0	0	0	0	cycles
nBSD	STOP command to READ or WRT command	2		2		2		cycles

† All references are made to the rising transition of CLK, unless otherwise noted.

‡ A CLK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CLK cycles occurring during the time when CKE is asserted low).

NOTES: 12. A data-out burst can be interrupted only on an even number of clock cycles after the initial READ command is entered (refer to nCCD).

13. A read or write burst can be interrupted only at an even number of clock cycles after entry of the initial READ or WRT command. The nCCD parameter is only required in the case of a burst interruption.

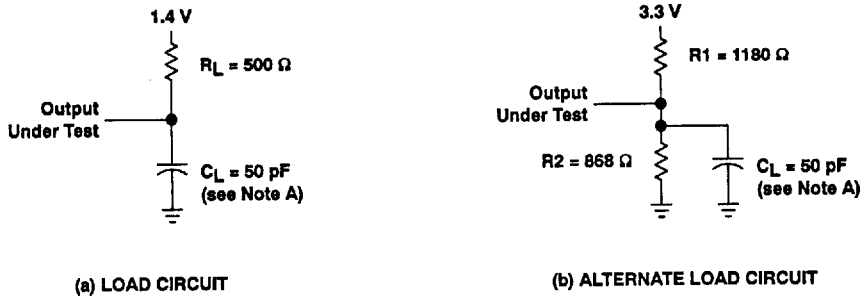




**PARAMETER MEASUREMENT INFORMATION**

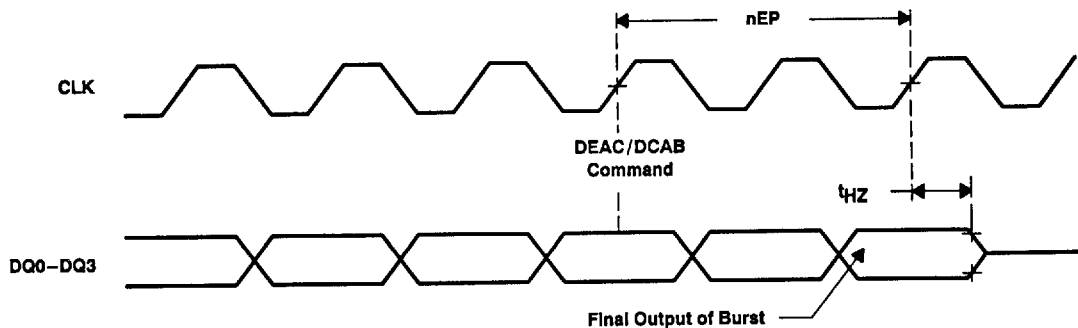
**general information for ac timing measurements**

The ac timing measurements are based on signal rise and fall times equal to 1 ns ( $t_T = 1$  ns) and a midpoint reference level of 1.4 V for LVTTTL. For signal rise and fall times greater than 1 ns, the reference level should be changed to  $V_{IH}$  min and  $V_{IL}$  max instead of the midpoint level. All specifications referring to READ commands are also valid for READ-P commands unless otherwise noted. All specifications referring to WRT commands are also valid for WRT-P commands unless otherwise noted. All specifications referring to consecutive commands are specified as consecutive commands for the same bank unless otherwise noted.



NOTE A:  $C_L$  includes probe and fixture capacitance.

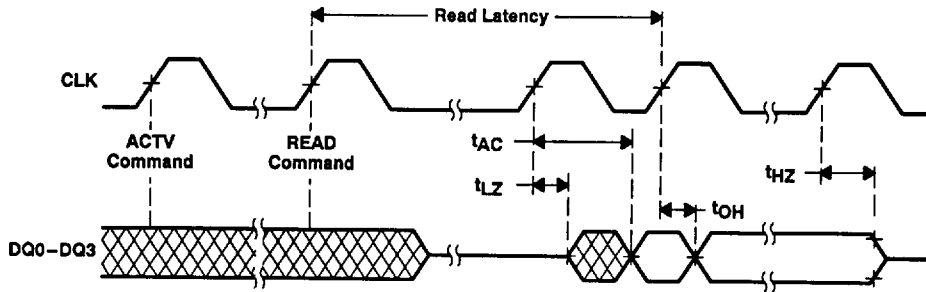
Figure 11. Load Circuits



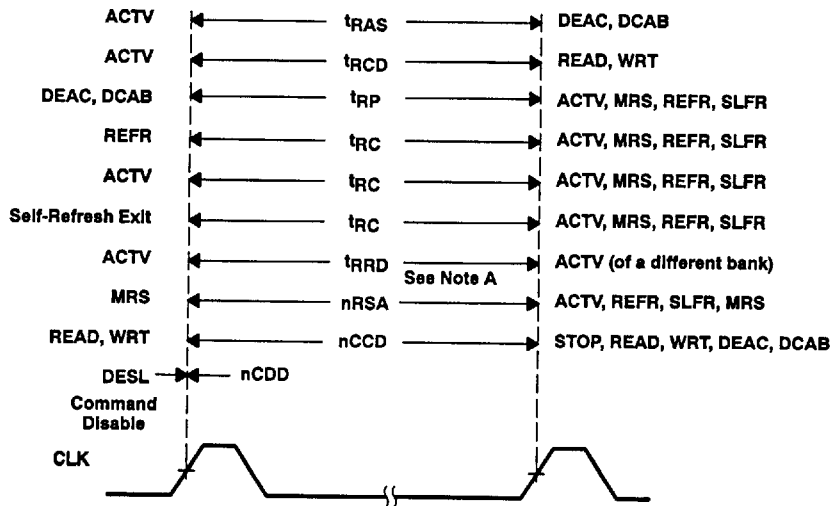
NOTE A: For this example, assume read latency = 3 and burst length > 1.

Figure 12.  $nEP$ , Final Data Output to DEAC or DCAB Command

**PARAMETER MEASUREMENT INFORMATION**



**Figure 13. Output Parameters**



NOTE A: t<sub>RRD</sub> is specified for command execution in one bank to command execution in the other bank.

**Figure 14. Command-to-Command Parameters**

**PARAMETER MEASUREMENT INFORMATION**

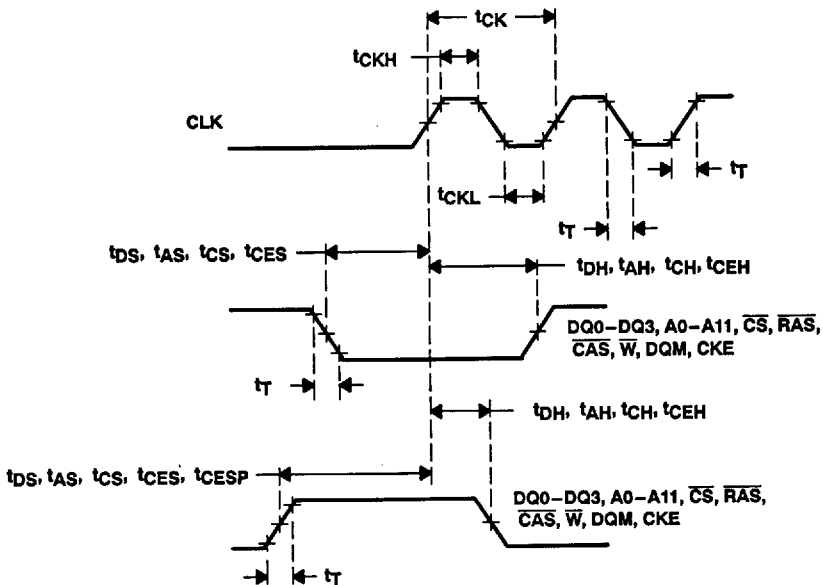
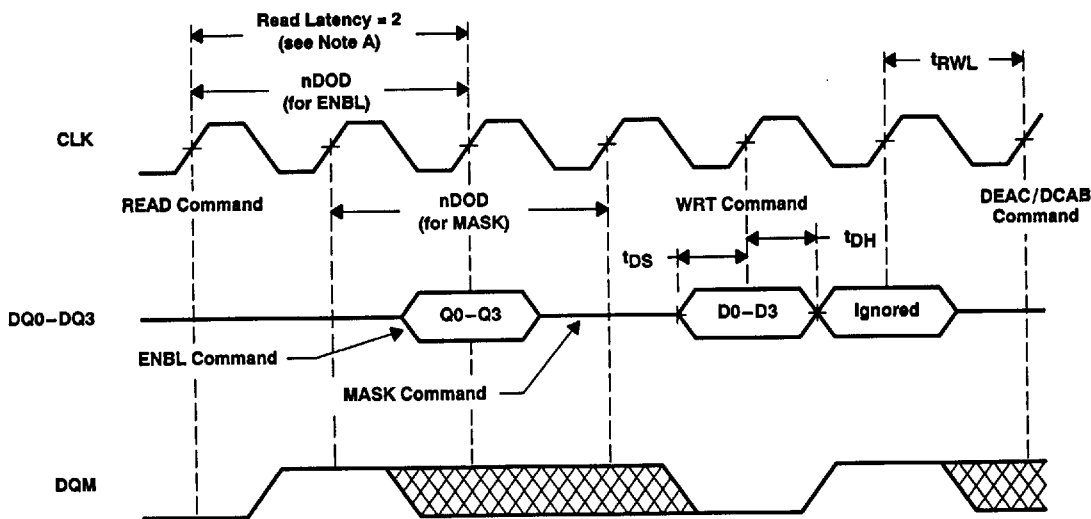


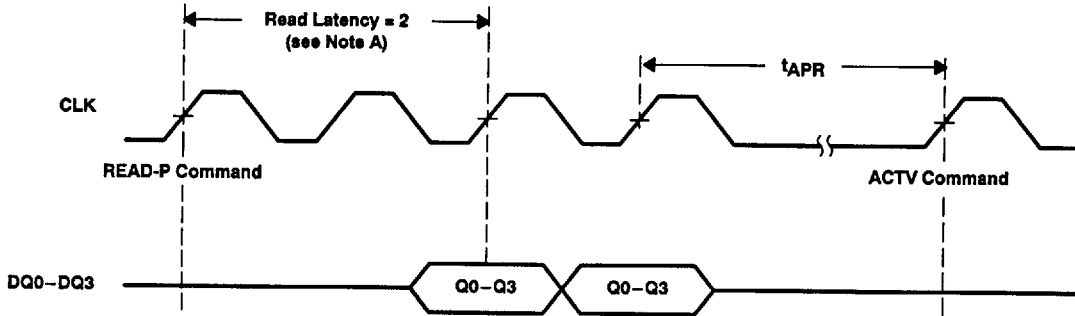
Figure 15. Input-Attribute Parameters



NOTE A: For this example, assume read latency = 2 and burst length = 2.

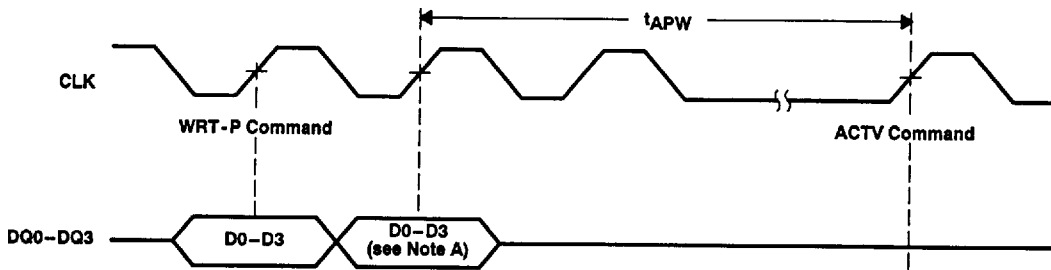
Figure 16. DQ Masking

PARAMETER MEASUREMENT INFORMATION



NOTE A: For this example, assume read latency = 2 and burst length = 2.

Figure 17. Read-Automatic Deactivate (Autoprecharge)



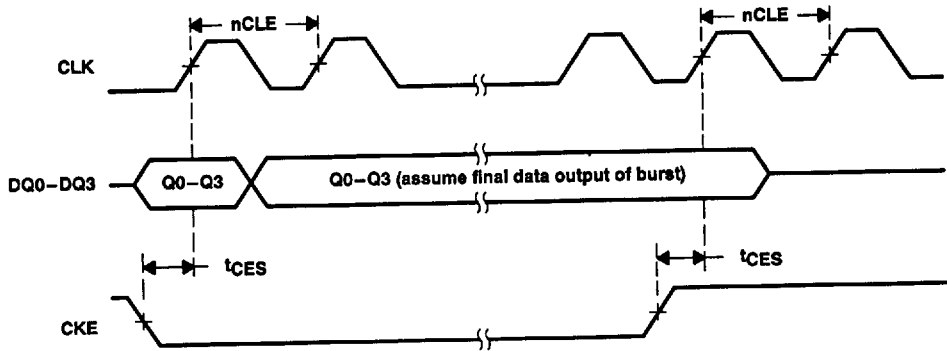
NOTE A: For this example, the burst length = 2.

Figure 18. Write-Automatic Deactivate (Autoprecharge)

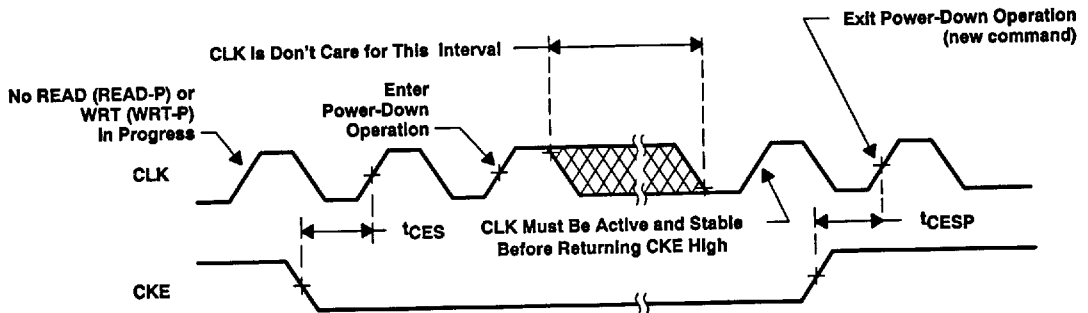


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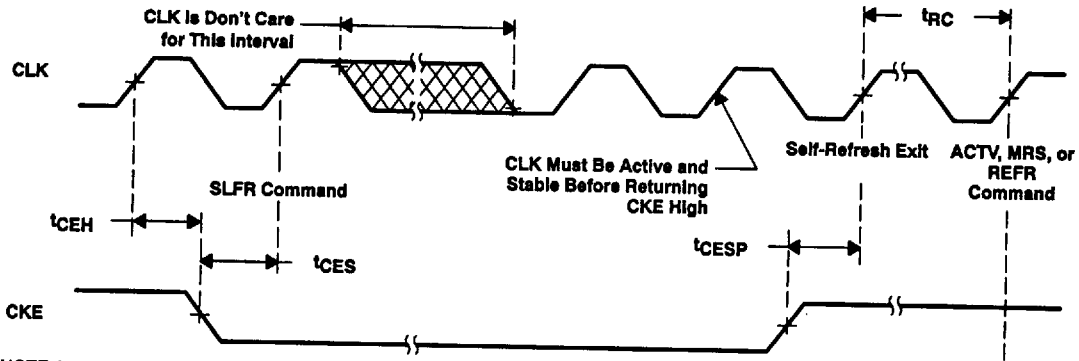


**Figure 19. CLK-Suspend Operation**



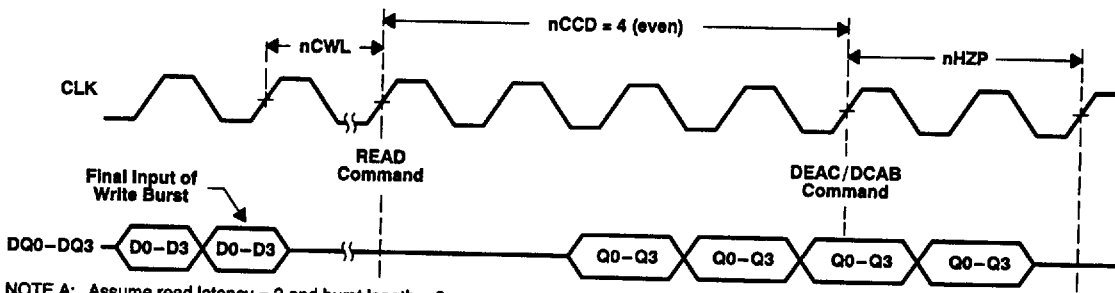
**Figure 20. Power-Down Operation**

**PARAMETER MEASUREMENT INFORMATION**



NOTE A: Assume both banks are previously deactivated.

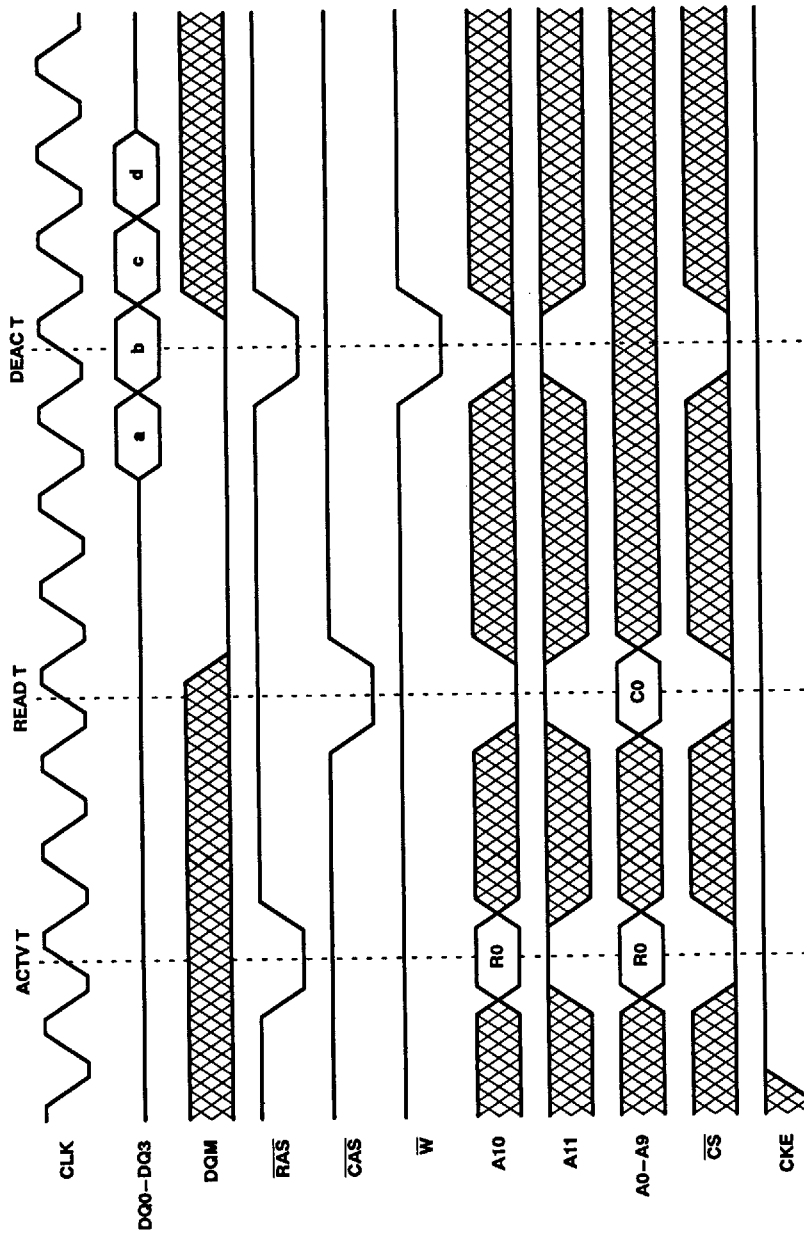
**Figure 21. Self-Refresh Entry/Exit**



NOTE A: Assume read latency = 2 and burst length = 8.

**Figure 22. Write Burst Followed by DEAC/DCAB-Interrupted Read**

**PARAMETER MEASUREMENT INFORMATION**

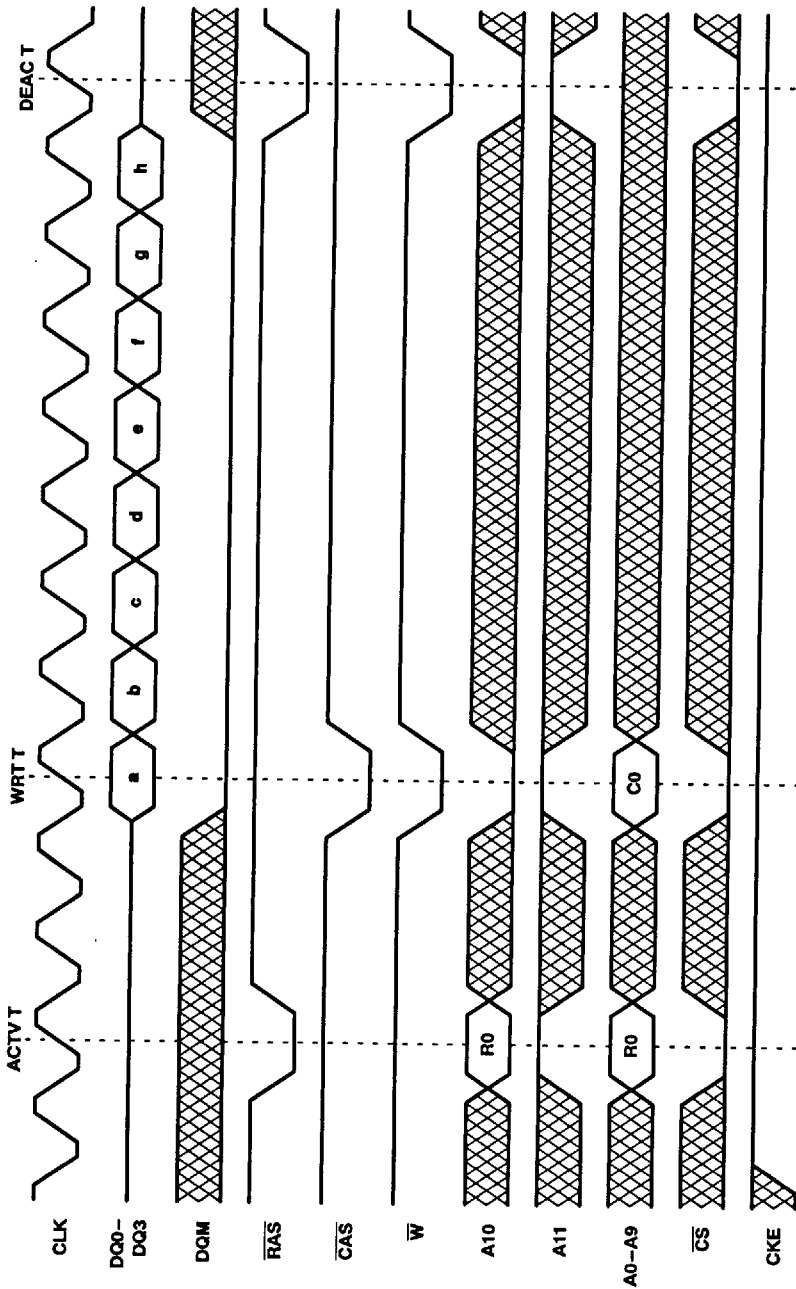


BURST TYPE	BANK	ROW	BURST CYCLE			
(D/Q)	(B/T)	ADDR	a	b	c	d
Q	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).  
 NOTE A: This example illustrates minimum  $t_{PCD}$  and  $nEP$  for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

**Figure 23. Read Burst (read latency = 3, burst length = 4)**

PARAMETER MEASUREMENT INFORMATION

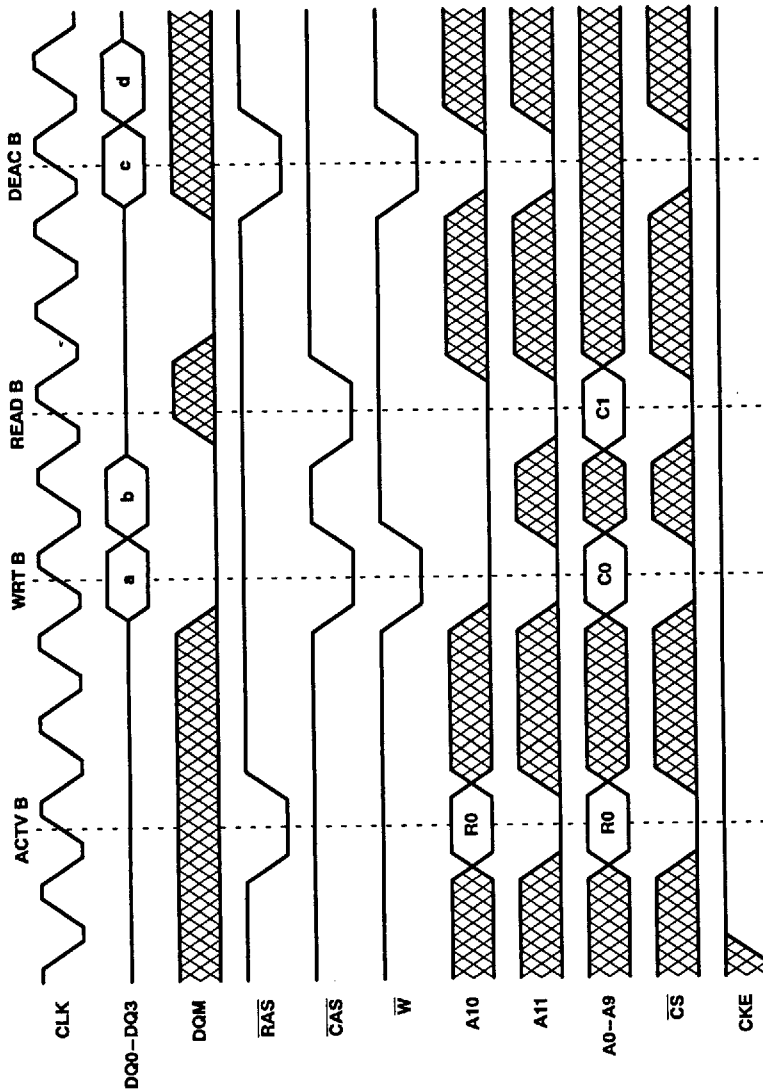


BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
D	T	R0	C0†	C0 + 1	C0 + 2	C0 + 3	C0 + 4	C0 + 5	C0 + 6	C0 + 7

† Column-address sequence depends on programmed burst type and C0 (see Table 6).  
 NOTE A: This example illustrates minimum tRWL for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 24. Write Burst (burst length = 8)

**PARAMETER MEASUREMENT INFORMATION**



BURST TYPE	BANK	ROW	BURST CYCLE			
(D/Q)	(B/T)	ADDR	a	b	c	d
D	B	R0	C0†	C0 + 1	C1‡	C1 + 1
Q	B	R0				

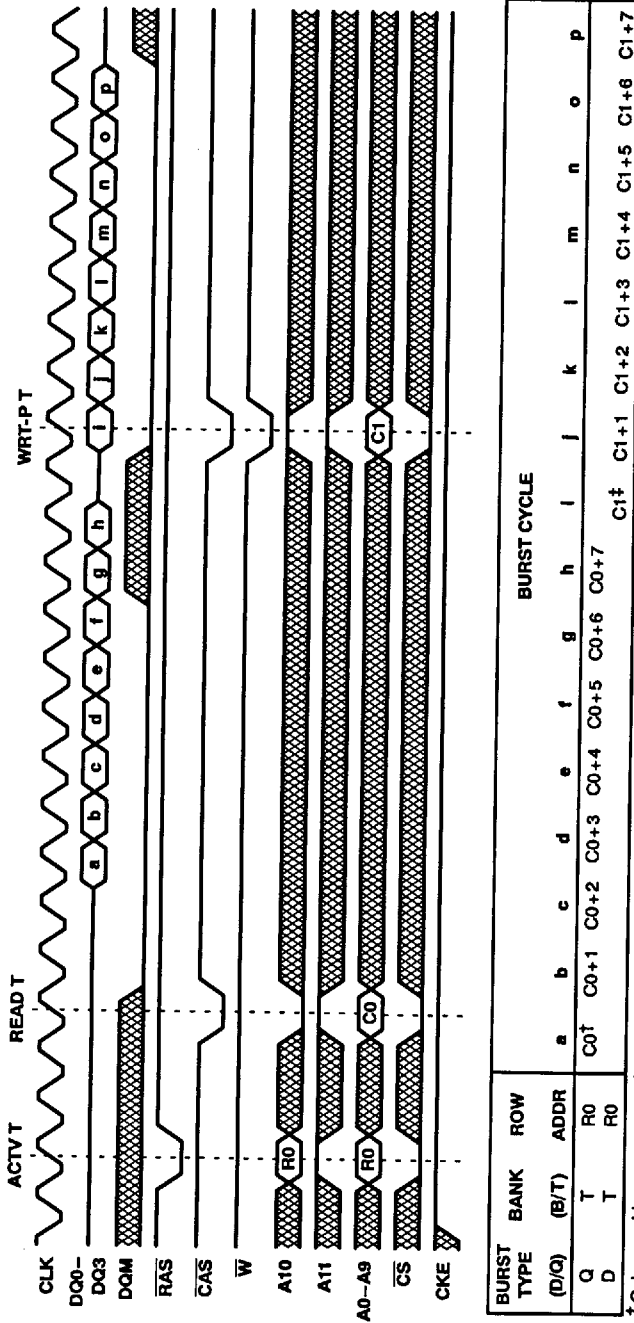
† Column-address sequence depends on programmed burst type and C0 (see Table 4).

‡ Column-address sequence depends on programmed burst type and C1 (see Table 4).

NOTE A: This example illustrates minimum t<sub>PCD</sub> for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

**Figure 25. Write-Read Burst (read latency = 3, burst length = 2)**

PARAMETER MEASUREMENT INFORMATION

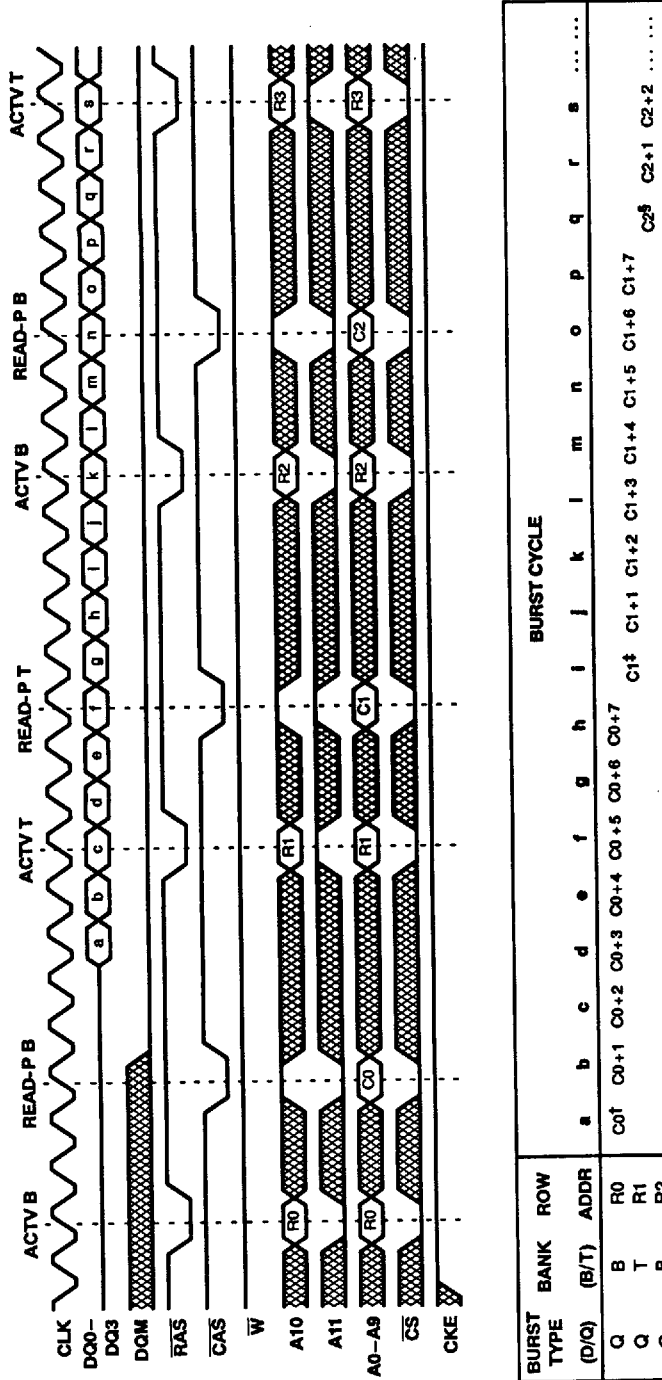


† Column-address sequence depends on programmed burst type and C0 (see Table 6).  
 ‡ Column-address sequence depends on programmed burst type and C1 (see Table 6).  
 NOTE A: This example illustrates minimum t<sub>RC</sub>D for the '626402-10 at 100 MHz, the '626402-15 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 26. Read-Write Burst With Automatic Deactivate (read latency = 3, burst length = 8)



**PARAMETER MEASUREMENT INFORMATION**

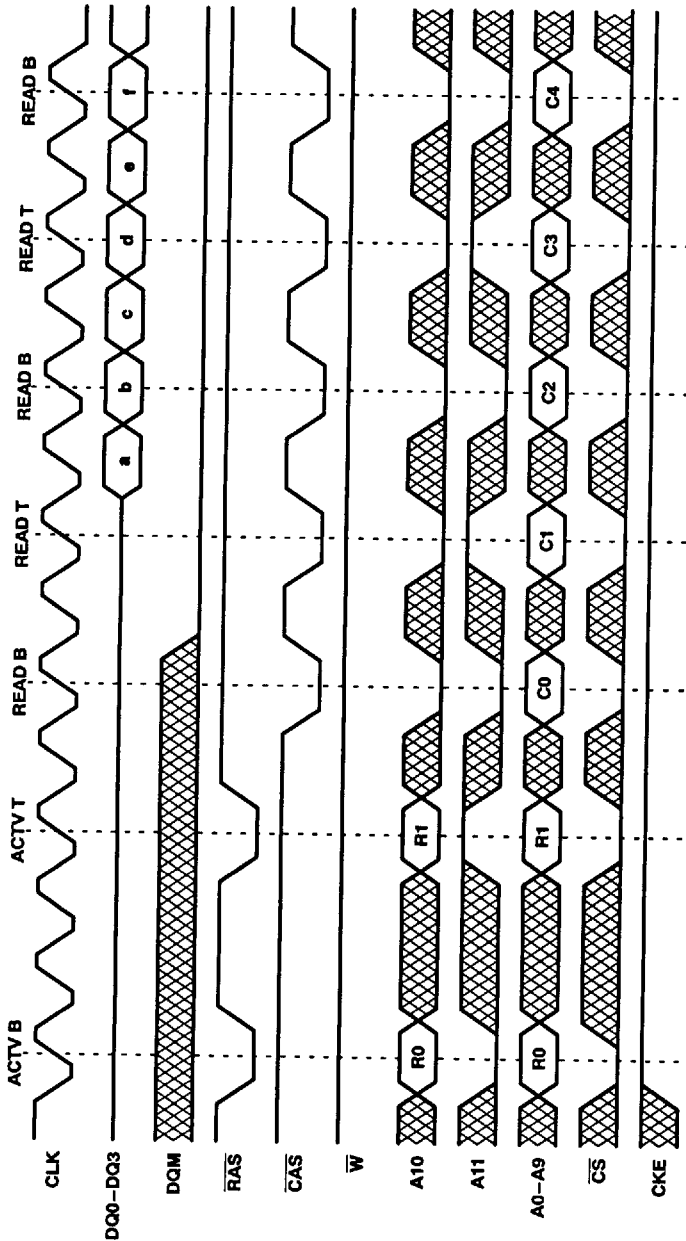


**Figure 27. Two-Bank Row-Interleaving Read Bursts With Automatic Deactivate (read latency = 3, burst length = 8)**

† Column-address sequence depends on programmed burst type and C0 (see Table 6).  
 ‡ Column-address sequence depends on programmed burst type and C1 (see Table 6).  
 § Column-address sequence depends on programmed burst type and C2 (see Table 6).  
 NOTE A: This example illustrates minimum t<sub>QCD</sub> for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.



PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK (B/T)	ROW ADDR	BURST CYCLE					
Q	B	R0	a	b	c	d	e	f
Q	T	R1	C0†	C0+1	C1†	C1+1	C2‡	C2+1
Q	B	R0						
...	...	...						

† Column-address sequence depends on programmed burst type and C0 (see Table 4).

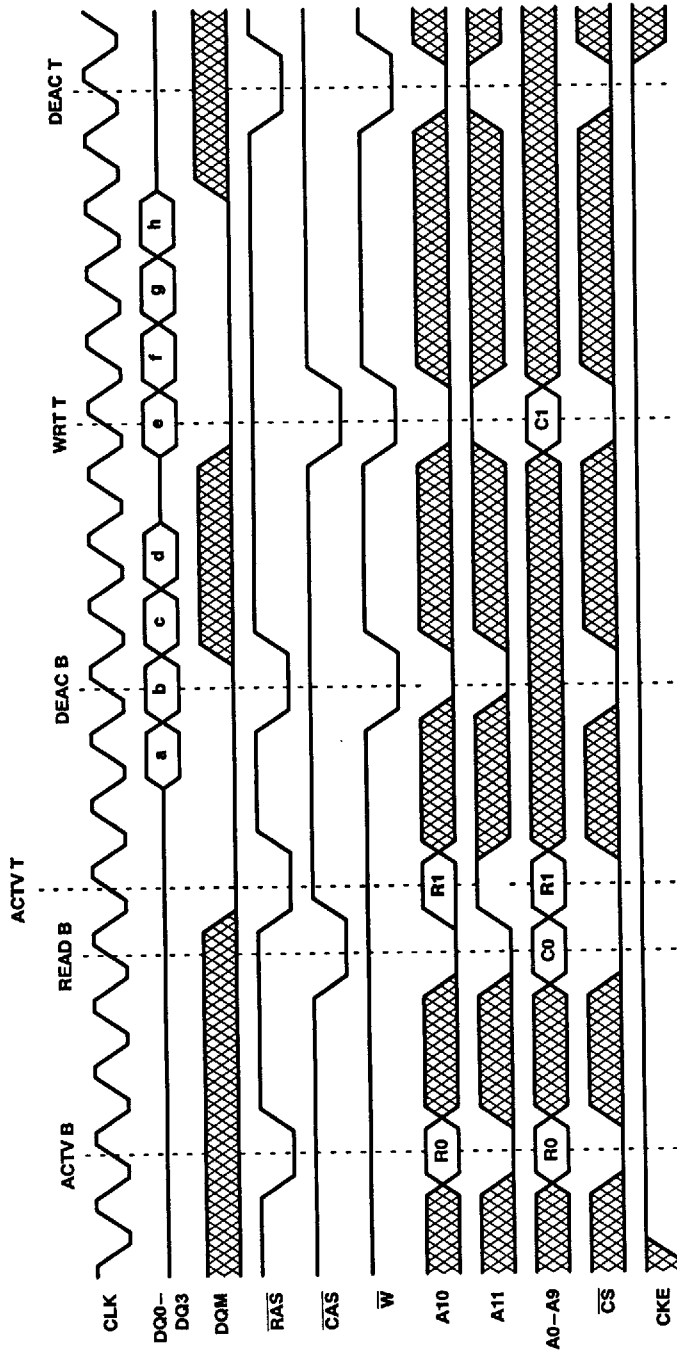
‡ Column-address sequence depends on programmed burst type and C1 (see Table 4).

§ Column-address sequence depends on programmed burst type and C2 (see Table 4).

Figure 28. Two-Bank Column-Interleaving Read Bursts (read latency = 3, burst length = 2)



**PARAMETER MEASUREMENT INFORMATION**

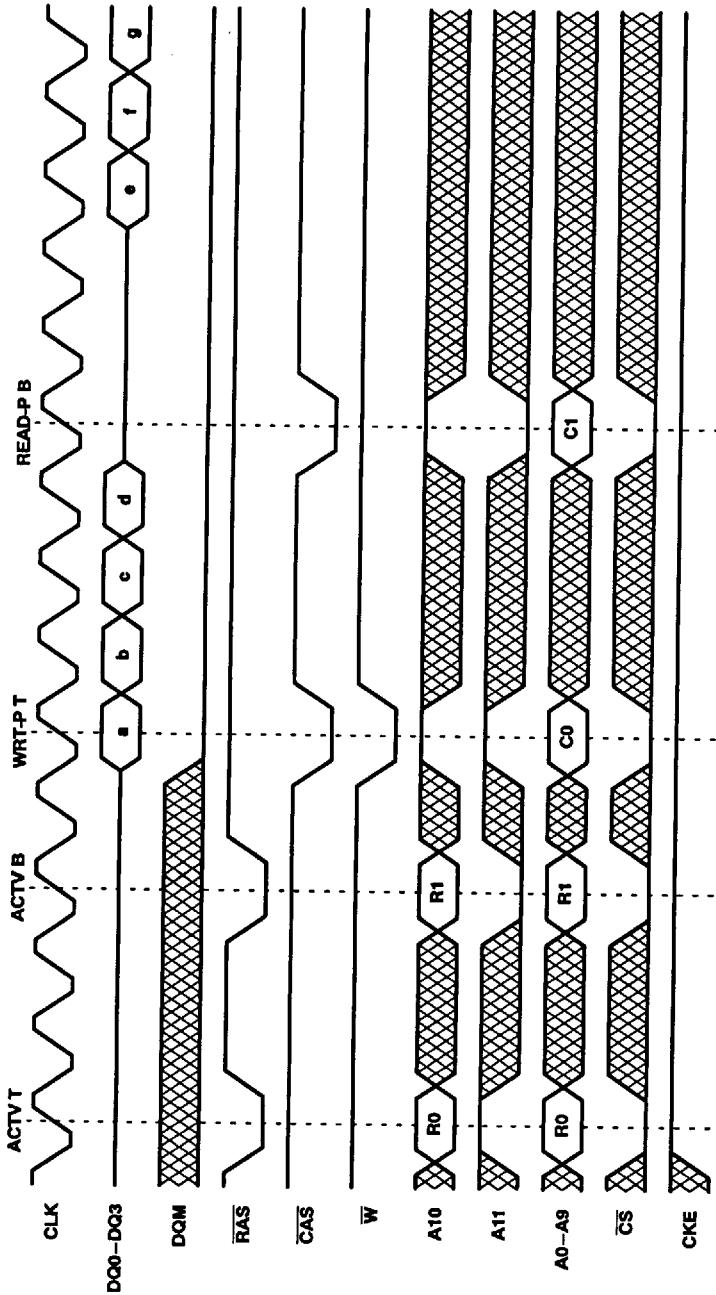


BURST TYPE	BANK (B/T)	ROW ADDR	BURST CYCLE							
Q	B	R0	a	b	c	d	e	f	g	h
D	T	R1	C0†	C0+1	C0+2	C0+3	C1‡	C1+1	C1+2	C1+3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).  
 ‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).  
 NOTE A: This example illustrates a minimum  $t_{PCD}$  and nEP read burst, and a minimum  $t_{PWL}$  write burst for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

**Figure 29. Read-Burst Bank B, Write-Burst Bank T (read latency = 3, burst length = 4)**

PARAMETER MEASUREMENT INFORMATION



BURST TYPE	BANK	ROW	BURST CYCLE							
(D/Q)	(B/T)	ADDR	a	b	c	d	e	f	g	h
D	T	R0	C0†	C0+1	C0+2	C0+3	C1‡	C1+1	C1+2	C1+3
Q	B	R1								

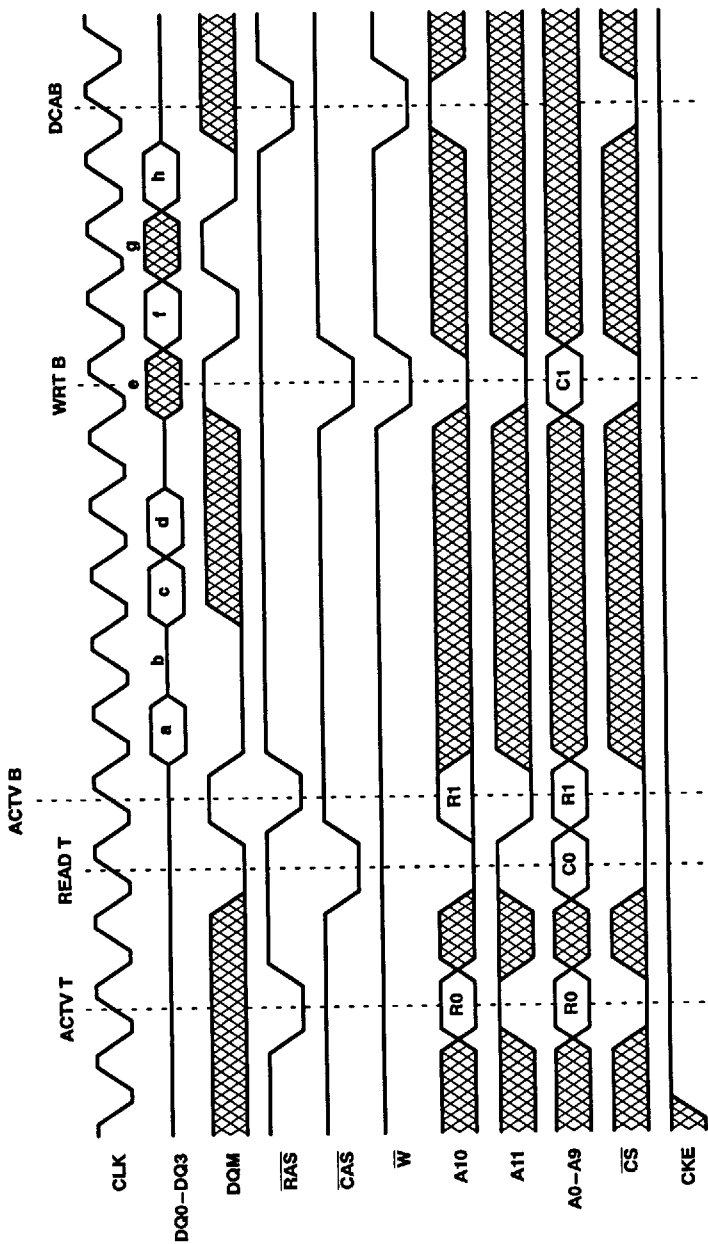
† Column-address sequence depends on programmed burst type and C0 (see Table 5).

‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).

NOTE A: This example illustrates minimum nCWL for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 30. Write-Burst Bank T, Read-Burst Bank B With Automatic Deactivate (read latency = 3, burst length = 4)

PARAMETER MEASUREMENT INFORMATION

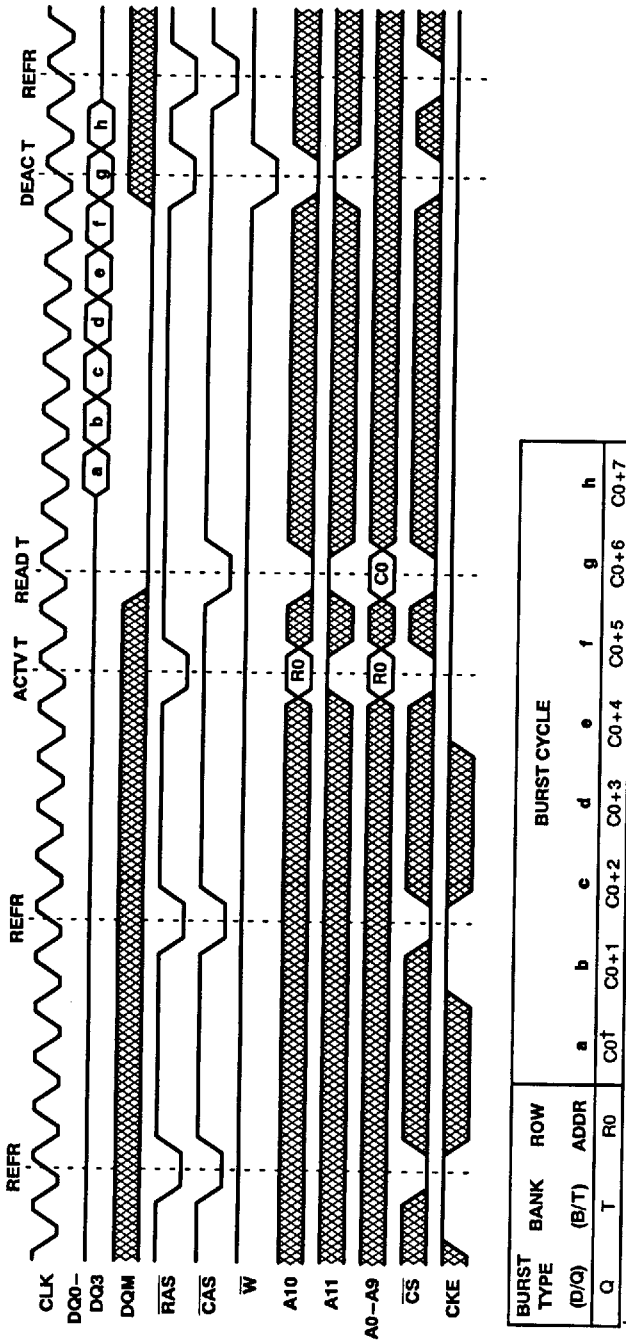


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE								
			a	b	c	d	e	f	g	h	
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0†	C1‡	C1+1	C1+2	C1+3
D	B	R1									

† Column-address sequence depends on programmed burst type and C0 (see Table 5).  
 ‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).  
 NOTE A: This example illustrates a minimum t<sub>PCD</sub> read burst and minimum t<sub>PWL</sub> write burst for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 31. Use Of DQM for Output and Data-In Cycle Masking (read-burst bank T, write-burst bank B, deactivate all banks) (read latency = 2, burst length = 4)

PARAMETER MEASUREMENT INFORMATION



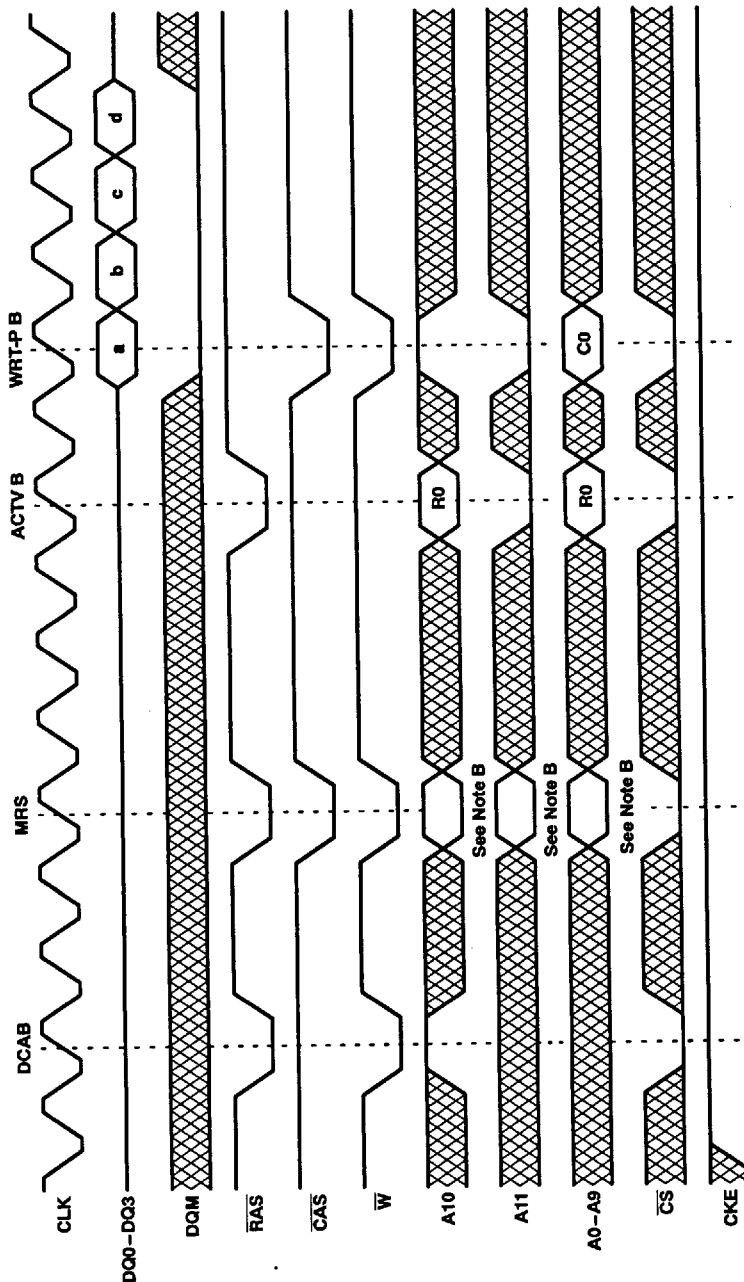
BURST TYPE	BANK	ROW	BURST CYCLE							
(D/O)	(B/T)	ADDR	a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3	C0+4	C0+5	C0+6	C0+7

† Column-address sequence depends on programmed burst type and C0 (see Table 6).

NOTE A: This example illustrates minimum tRC, tRCD, nEP, and tRP for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 32. Refresh Cycles (refreshes followed by read burst followed by refresh) (read latency = 2, burst length = 8)

**PARAMETER MEASUREMENT INFORMATION**

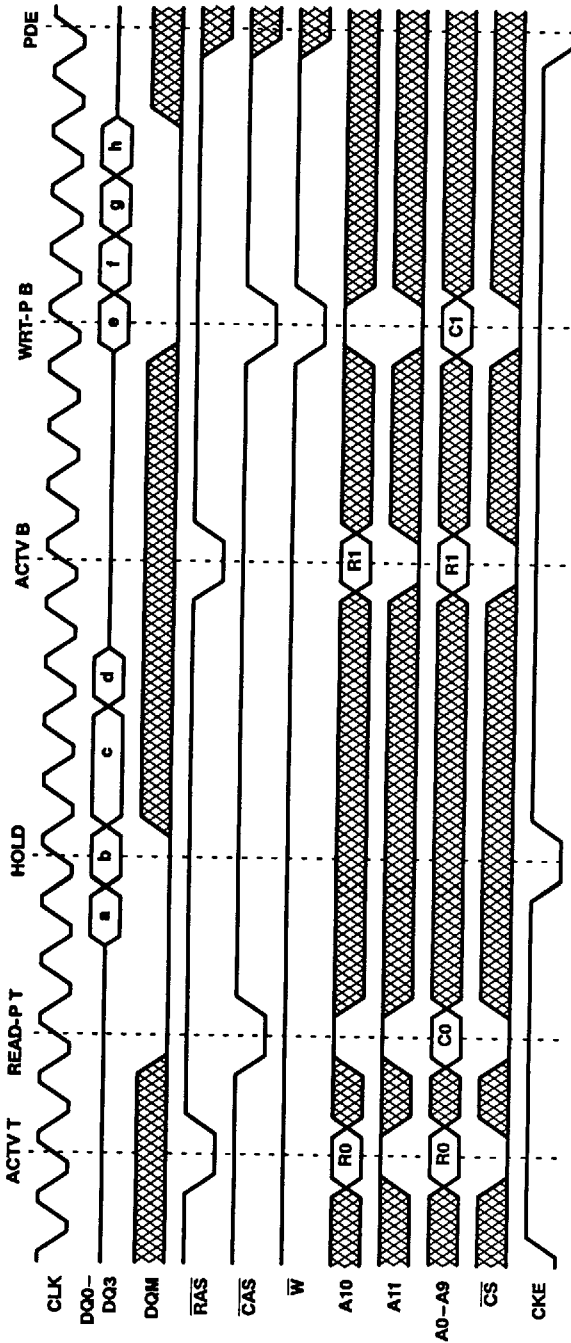


BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE			
D	B	R0	a	b	c	d
			C0†	C0+1	C0+2	C0+3

† Column-address sequence depends on programmed burst type and C0 (see Table 5).  
 NOTES: B. This example illustrates minimum t<sub>PCD</sub> for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.  
 C. Refer to Figure 1

**Figure 33. Mode-Register Programming (deactivate all, mode program, write burst with automatic deactivate) (read latency = 2, burst length = 4)**

PARAMETER MEASUREMENT INFORMATION



BURST TYPE (D/Q)	BANK (B/T)	ROW ADDR	BURST CYCLE							
			a	b	c	d	e	f	g	h
Q	T	R0	C0†	C0+1	C0+2	C0+3	C1‡	C1+1	C1+2	C1+3
D	B	R1								

† Column-address sequence depends on programmed burst type and C0 (see Table 5).

‡ Column-address sequence depends on programmed burst type and C1 (see Table 5).

NOTE A: This example illustrates minimum t<sub>RCD</sub> for the '626402-10 at 100 MHz, the '626402-12 at 80 MHz, and the '626402-15 at 66 MHz.

Figure 34. Use of CKE for Clock Gating (Hold) and Standby Mode (read-burst bank T with hold, write-burst bank B, standby mode) (read latency = 2, burst length = 4)