DESCRIPTION

The 54/74LS221 is a monolithic dual multivibrator which features a negative-transition-triggered input either of which can be used as an inhibit input. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hystersis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2V. A high immunity to Vcc noise of typically 1.5V is also provided by internal latching circuitry.

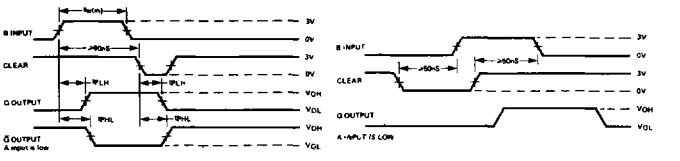
Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulse can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35ns to 49s (54LS221) or 70s (74LS221) by choosing appropriate timing components. With R_{ext} = 2kΩ and C_{ext} = 0, an output pulse of typically 30ns is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of Vcc and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and Vcc ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 70kΩ for the 54LS221, and 2kΩ to 100kΩ for the 74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}$. In 20.7 C_{ext}-R_{ext}. In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4k may be used. Also, the range of jitter-free output pulse widths is extended if Vcc is held to 5V and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. High duty cycles are available if a certain amount pulse width jitter is allowed. The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components.

Pin assignments for this device are identical to those of the 54LS123/74LS123 so that the 54/74LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.

PARAMETER MEASUREMENT INFORMATION



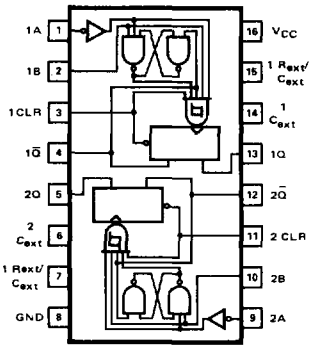
NOTES:

A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω; t_r ≤ 15 ns, t_f ≤ 6 ns.

B. All measurements are made between the 1.3V points of the indicated transitions

PIN CONFIGURATION

B,F,W PACKAGE



positive logic:
Low input to clear reset Q low and Q̄ high regardless of d-c levels at A or B input.

TRUTH TABLE

(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍

Also see description and switching characteristics

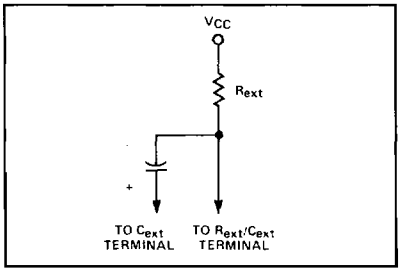
H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high level pulse
⎍ = one low level pulse
X = irrelevant

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B

HYSTERESIS VS. TEMPERATURE — TYPICAL VALUES

PARAMETER	54/74 -55°C	54/74 +25°C	54/74 +125°C	54/74LS -55°C	54/74LS +25°C	54/74LS +125°C	UNIT
V_{T+} Positive going threshold							
A Input		1.4	2				V
B Input		1.55	2				V
V_{T-} Negative going threshold							
A Input	0.8	1.4					V
B Input	0.8	1.35					V
Hysteresis							



TIMING COMPONENT CONNECTIONS

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω C_{ext} = 80pF R_{ext} = 2kΩ			54/74LS C_L=15pF R_L=2kΩ C_{ext} = 80pF R_{ext}=2kΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
$t_{w(out)}$	A,B	Q,$\overline{Q}$	70	110	150	70	110	150	ns
			C_{ext}=0 R_{ext}=2kΩ			C_{ext}=0 R_{ext}=2kΩ			
			20	30	50	15	25	70	
			C_{ext}=100pF R_{ext}=10kΩ			C_{ext}=100pF R_{ext}=10kΩ			
			650	700	750	600	700	750	
			C_{ext}=1μf R_{ext}=10kΩ			C_{ext}=1μf R_{ext}=10kΩ			
			6.5	7	7.5	6.0	7	7.5	ms
$t_{w(in)}$			50			50			ns
$t_{w(clear)}$ Width of clear input pulse			20			40			ns
t_{Setup} (clear)			15			15↑			ns
dv/dt Rate of rise or fall of input pulse									
Schmitt,B			1			1			V/s
Logic Input, A			1			1			V/μs
R_{ext} External timing resistance			(54)			(54)			
			1.4		30	1.4		70	kΩ
			(74)			(74)			
			1.4		40	1.4		100	kΩ
C_{ext} External timing capacitance			0		1000	0		1000	μF
Output duty cycle				67			67		%
			R_{ext}=Max			R_T=Max R_{ext}			
				90			90		%
Propagation delay time									
t_{PLH} Low-to-high	A	Q		45	70		45	70	ns
t_{PHL} High-to-low	A	$\overline{Q}$		50	80		50	80	
t_{PLH} Low-to-high	B	Q		35	55		35	55	
t_{PHL} High-to-low	B	$\overline{Q}$		40	65		40	65	
t_{PLH} Low-to-high	Clear	$\overline{Q}$			40			65	
t_{PHL} High-to-low	Clear	Q			27			55	

Load circuit and typical waveforms are shown at the front of section.

LOGIC