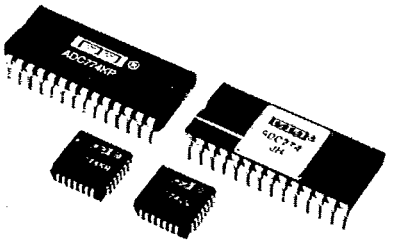
T-51-10-12

BURR-BROWN®



ADC774

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, or 16-BIT MICROPROCESSOR BUS INTERFACE
- ALTERNATE SOURCE FOR HI774 A/D CONVERTER: 8.5µs Conversion Time, 150ns Bus Access Time
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES OVER TEMPERATURE:
  0°C to +75°C: ADC774J, K
  –55°C to +125°C: ADC774SH, TH

DESCRIPTION

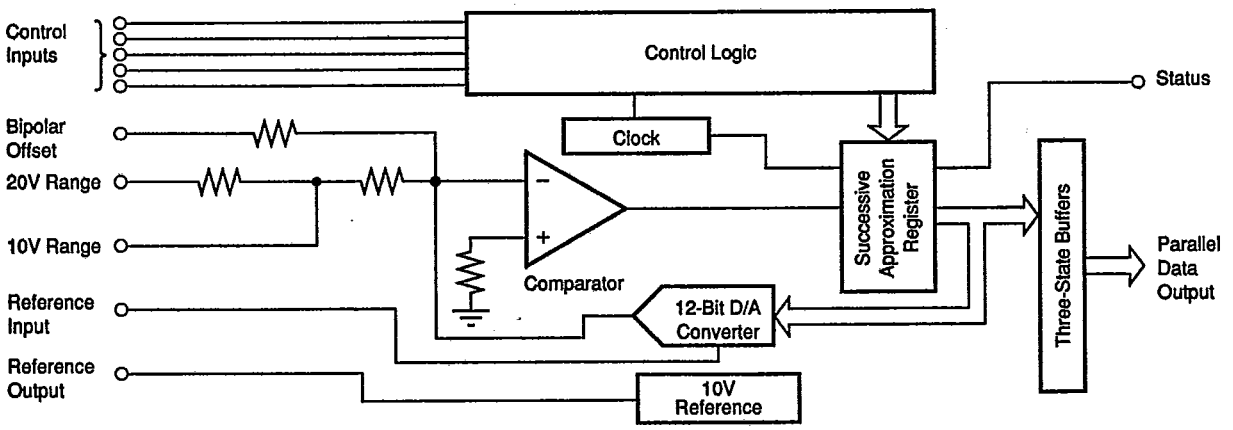
The ADC774 is a 12-bit successive approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 8.5µs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC774, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, plastic leadless chip carrier, or a hermetic side-brazed ceramic DIP.



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Printed in U.S.A. December, 1990

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = –12V or –15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774J, ADC774SH MIN.	ADC774J, ADC774SH TYP	ADC774J, ADC774SH MAX	ADC774K, ADC774TH MIN	ADC774K, ADC774TH TYP	ADC774K, ADC774TH MAX	UNITS
RESOLUTION			12			*	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			*		V
Bipolar		±5, ±10			*		V
Impedance: 0 to +10V, ±5V	4.7	5	5.3	*	*	*	kΩ
±10V, 0V to +20V	9.4	10	10.6	*	*	*	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)							
Over Temperature Range							
Voltages: Logic 1	+2		+5.5	*		*	V
Logic 0	–0.5		+0.8	*		*	V
Current	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
At +25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (Adjustable to Zero)			±2			*	LSB
Bipolar Offset Error (Adjustable to Zero)			±10			±4	LSB
Full-Scale Calibration Error[1]							
(Adjustable to Zero)			±0.25			*	% of FS[2]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			*		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±3/4	LSB
Full-Scale Calibration Error							
Without Initial Adjustment [1] : J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to Zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[3]							
Unipolar Offset: J, K Grades			±10			±5	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} <+16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
–16.5V < V_{EE} <–13.5V or –12.6V < V_{EE} < –11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} <+5.5V			±1/2			*	LSB
CONVERSION TIME [4,5]							
8-Bit Cycle		5	5.3		*	*	µs
12-Bit Cycle		7.5	8.5		*	*	µs
OUTPUTS							
DIGITAL (DB11 – DB0, STATUS)							
(Over Temperature Range)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			*	V
Logic 1 (I_{SOURCE} = 500µA)	+2.4			*			V
Leakage, Data Bits Only, High-Z State	–5	0.1	+5	*	*	*	µA
Capacitance		5			*		pF
INTERNAL REFERENCE VOLRAGE							
Voltage	+9.9	+10	+10.1	*	*	*	V
Source Current Available for External Loads [6]	2.0			*			mA

SPECIFICATIONS (CONT)

ELECTRICAL

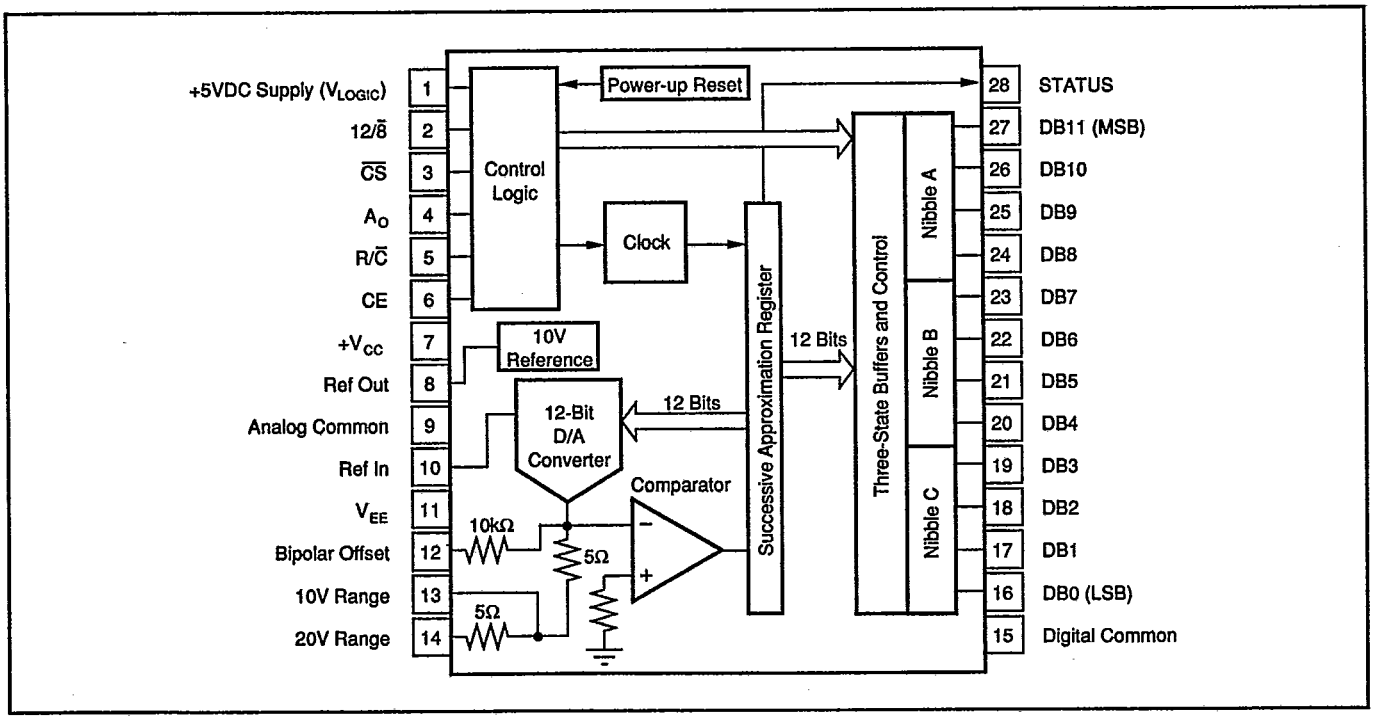
T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

PARAMETER	ADC774J, ADC774SH			ADC774K, ADC774TH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Voltage: V_{CC}	+11.4		+16.5	*		*	V
V_{EE}	−11.4		−16.5	*		*	V
V_{LOGIC}	+4.5		+5.5	*		*	V
Current: I_{CC}		3.5	5		*	*	mA
I_{EE}		15	20		*	*	mA
I_{LOGIC}		9	15		*	*	mA
Power Dissipation (±15V Supplies)		325	450		*	*	mW
TEMPERATURE RANGE (Ambient: T_{MIN}, T_{MAX})							
Specifications: J, K Grades	0		+75	*		*	°C
S, T Grades	−55		+125	*		*	°C
Storage	−65		+150	*		*	°C

*Same specification as ADC774JH, JP, JN, SH.

NOTES: (1) With fixed 50Ω resistor from Ref Out to Ref In. This parameter is also adjustable to zero at +25C. (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range FS means 20V; for a 0V to +10V range, FS means 10V. The term Full Scale for these specification instead of Full-Scale Range is used to be consistent with other vendors' specifications tables. (3) Using internal reference. (4) See "Controlling the ADC774" section for detailed information concerning digital timing. (5) The Harris HI-774 uses a subranging/error correction technique that allows one to begin conversion before a preceding sample-hold or multiplexer has settled to ±1/2LSB. For 12-bit accurate conversions, the input transient to the ADC774 must settle to less than ±1/2LSB before conversion is started. The ADC774 is compatible with HI-774 in all other respects. (6) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0V to +16.5V
V_{EE} to Digital Common ..... 0V to –16.5V
V_{LOGIC} Digital Common ..... 0V to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$)
to Digital Common ..... –0.5V to V_{LOGIC} +0.5V
Analog Inputs (Ref In, Bipolar Offset, $10V_{IN}$)
to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
Ref Out ..... Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature ..... +165°C
Power Dissipation 1000mW
Lead Temperature (soldering,10s) ..... +300°C
Thermal Resistance, θ_{JA} : Ceramic ..... 50°C/W
Plastic ..... 100°C/W

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling prochedures schould be followed.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC774s. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g. ADC774KP-BI). See Ordering Information for pricing.

ORDERING INFORMATION

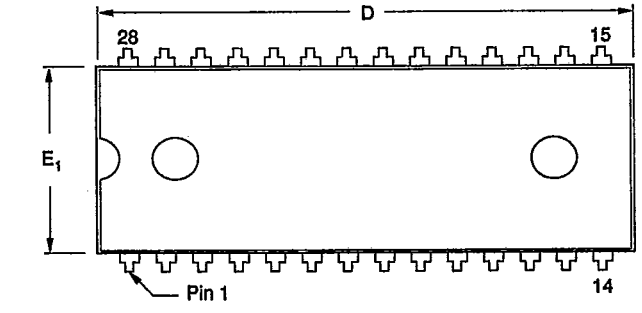
MODEL	PACKAGE	TEMPERATURE RANGE	LINEARITY ERROR MAX (T_{MIN} TO T_{MAX})	USA OEM PRICES 1–24	25–99	100s
ADC774JN	PLCC	0°C to +75°C	±1LSB	$58.00	$45.80	$40.50
ADC774KN	PLCC	0°C to +75°C	±1/2LSB	74.80	59.00	52.30
ADC774JP	Plastic DIP	0°C to +75°C	±1LSB	55.20	43.60	38.60
ADC774KP	Plastic DIP	0°C to +75°C	±1/2LSB	71.20	56.20	49.80
ADC774JH	Ceramic DIP	0°C to +75°C	±1LSB	69.00	54.50	48.30
ADC774KH	Ceramic DIP	0°C to +75°C	±1/2LSB	89.00	70.30	62.30
ADC774SH	Ceramic DIP	–55°C to +125°C	±1LSB	195.00	154.00	136.50
ADC774TH	Ceramic DIP	–55°C to +125°C	±3/4LSB	265.00	209.00	185.50

BURN-IN SCREENING OPTION
See text for details.

MODEL	PACKAGE	TEMPERATURE RANGE	BURN-IN TEMP (160 HOURS)(1)	USA OEM PRICES 1–24	25–99	100s
ADC774JP-BI	Plastic DIP	0°C to +75°C	+85°C	$61.90	$50.10	$44.40
ADC774KP-BI	Plastic DIP	0°C to +75°C	+85°C	79.70	64.60	57.20
ADC774JH-BI	Ceramic DIP	0°C to +75°C	+125°C	79.40	62.70	55.50
ADC774KH-BI	Ceramic DIP	0°C to +75°C	+125°C	102.30	80.80	71.60
ADC774SH-BI	Ceramic DIP	–55°C to +125°C	+125°C	224.20	117.10	157.00
ADC774TH-BI	Ceramic DIP	–55°C to +125°C	+125°C	304.80	240.80	213.30

MECHANICAL

P Package — 28-Pin Plastic DIP

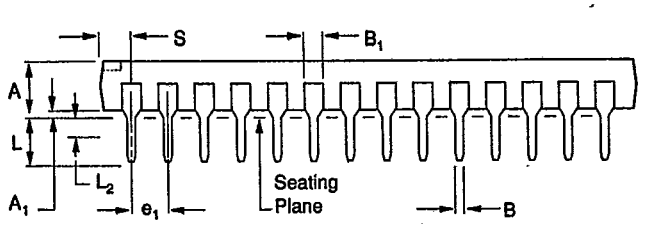


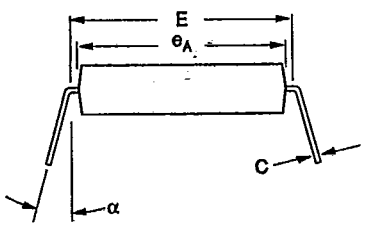
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A(1)	.169	.200	4.29	5.08
A1 (1)	.015	.070	0.38	1.78
B	.015	.020	0.38	0.51
B1	.015	.055	0.38	1.40
C	.008	.012	0.20	0.30
D(1)	1.380	1.455	35.05	36.96
E	.600	.625	15.24	15.88
E1 (1)	.485	.550	12.32	13.97
e1	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
L	.100	.200	2.54	5.08
L2	.000	.030	0.00	0.76
α	0°	15°	0°	15°
Q1	.020	.070	0.51	1.78
S1	.040	.080	1.02	2.03

(1) Not JEDEC Standard

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.





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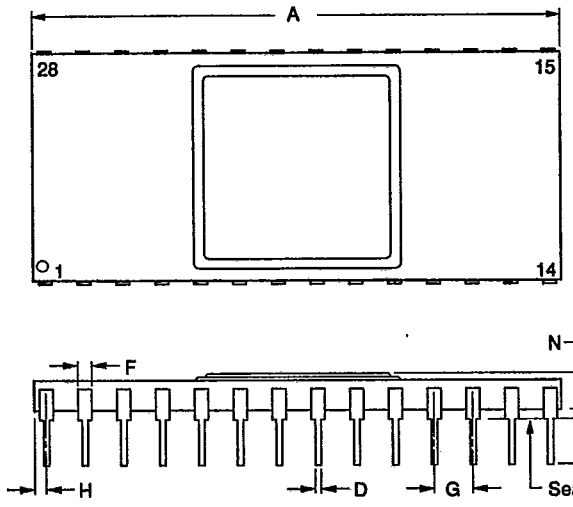
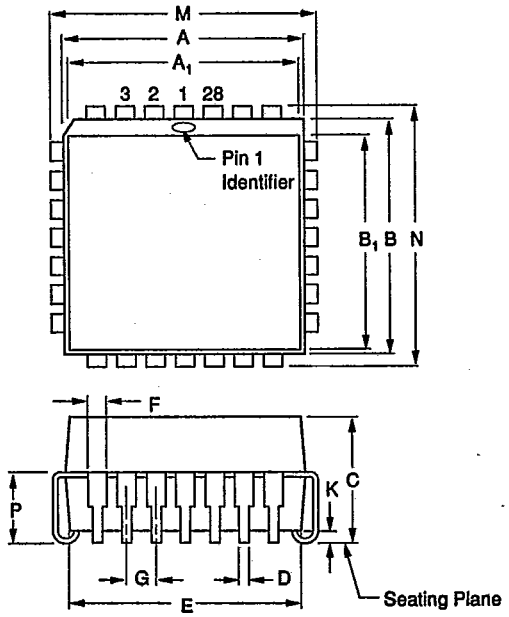
H Package — 28-Pin Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.386	1.414	35.20	35.92
C	.115	.175	2.92	4.45
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

P Package — 28-Pin LCC



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.450	0.460	11.43	11.68
A1	0.450	0.460	11.43	11.68
B	0.450	0.460	11.43	11.68
B1	0.450	0.460	11.43	11.68
C	0.165	0.180	4.19	4.57
D	0.013	0.023	0.33	0.58
E	0.390	0.430	9.91	10.92
F	0.026	0.032	0.66	0.81
G	0.50 BASIC		1.27 BASIC	
K	0.015	0.025	0.38	0.64
M	0.485	0.495	12.32	12.57
N	0.485	0.495	12.32	12.57
P	0.100	0.110	2.54	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

Thus, for a converter connected for biopolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of –10V is 2.44mV below the first code transition (000_H to 001_H at –9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination to appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of –1LSB), a missing code will occur.

ADC774KP, KN, KH and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

UNIPOLAR OFFSET ERROR

An ADC774 connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the acutal transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC774 specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC774 is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

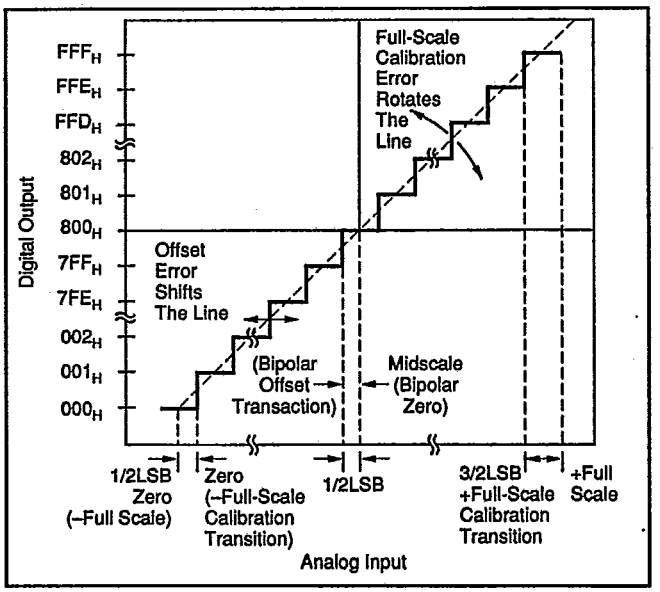


FIGURE 1. ADC774 Transfer Characteristics Terminology.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full-scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC774 assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e., a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined as:	±10V	±5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n =12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+Full-Scale Calibration	+10V – 3/2LSB	+5 – 3/2LSB	+10V – 3/2LSB	+10V – 3/2LSB
$7FF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 – 1/2LSB	0 – 1/2LSB	+5V – 1/2LSB	±10V – 1/2LSB
000_H to 001_H	Zero Calibration (– Full-Scale Calibration)	–10V + 1/2LSB	–5V + 1/2LSB	0 to + 1/2LSB	0 to + 1/2 LSB

TABLE I. Input Voltages, Transition Values, and LSB Values.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/21LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC774, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common. Analog common (pin 9) typically carries +8mA.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referred to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

If the 20V analog input range is used (either bipolar or unipolar), the 10V range input (pin 13) should be shielded with ground plane to reduce noise pickup. If the bipolar offset input (pin 12) is not used to externally trim the unipolar offset as shown in Figure 2, connect it to Analog Common (pin 9).

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC774 as possible. If no trim adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10µF tantalum-type capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

ANALOG SIGNAL SOURCE IMPEDANCE

The signal source supplying the analog input signal to the ADC774 will be driving into a nominal DC input impedance of either 5kΩ or 10kΩ. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast current changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

RANGE CONNECTIONS

The ADC774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V, and ±10V. If a 10V input range is required, the analog input signal should be connected to pin 13 of the converter. A signal requiring a 20V range is connected to pin 14. In either case the other pin of the two is left unconnected. Full-scale and offset adjustments are described below.

To operate the converter with a 10.24V (2.5mV LSB) or 20.48V (5mV LSB) input range, insert a 120Ω 1% metal-film resistor in series with pin 13 for the 10.24V range, or a 240Ω 1% metal-film resistor in series with pin 14 for the 20.48V range. Offset adjustments are still perfomed as described below. A fixed metal-film resistor can be used because the input impedance of the ADC774 is trimmed to typically less than ±2% of the nominal value.

CALIBRATION

OPTIONAL EXTERNAL FULL-SCALE AND OFFSET ADJUSTMENTS

Offset and full-scale errors may be trimmed to zero using external offset and full-scale trim potentiometers connected to the ADC774 as shown in Figures 2 and 3 for unipolar and bipolar operation.

CALIBRATION PROCEDURE— UNIPOLAR RANGES

If adjustment of unipolar offset and full scale is not required, replace R_2 with a 50Ω, 1% metal film resistor and connect pin 12 to pin 9, omitting the adjustment network.

If adjustment is required, connect the converter as shown in Figure 2. Sweep the input through the end-point transition voltage (0V + 1/2LSB; +1.22mV for the 10V range, +2.44mV for the 20V range) that causes the output code to be DB0 ON (high). Adjust potentiometer R_1 until DB0 is alternately toggling ON and OFF with all other bits OFF. Then adjust full scale by applying an input voltage of nominal full-scale value minus 3/2LSB, the value which should cause all bits to be ON. This value is +9.9963V for the 10V range and

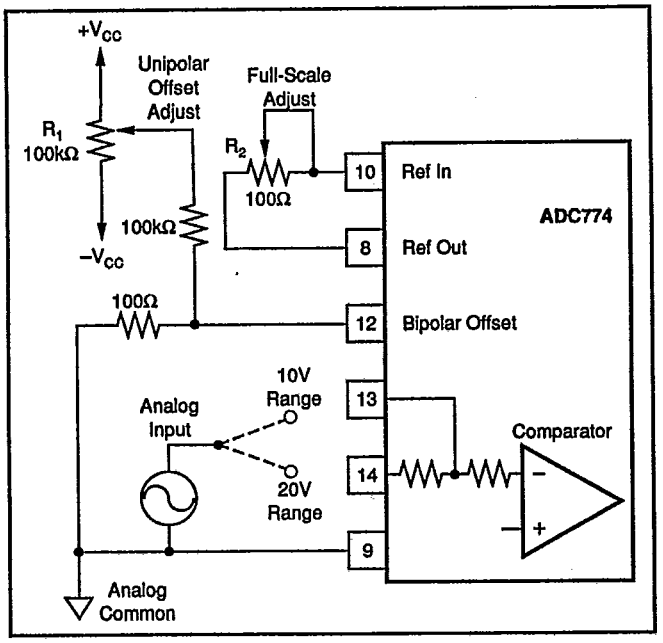


FIGURE 2. Unipolar Configuration.

+19.9927V for the 20V range. Adjust potentiometer R_2 until bits DB1-DB11 are ON and DB0 is toggling ON and OFF.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

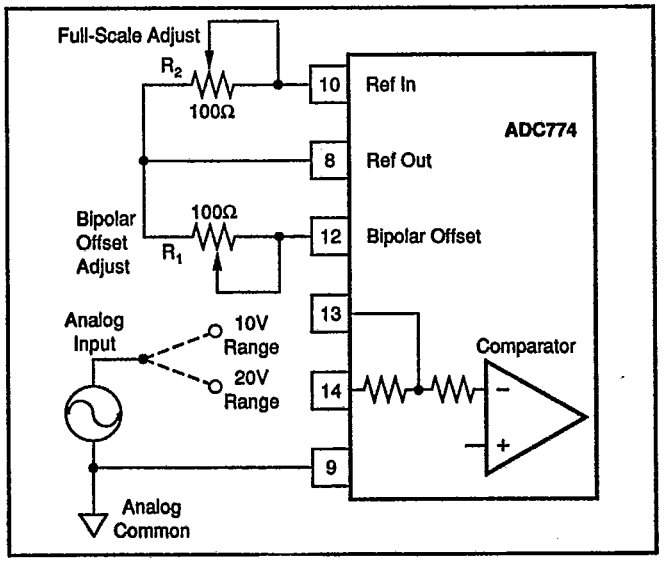


FIGURE 3. Bipolar Configuration.

CONTROLLING THE ADC774

The Burr-Brown ADC774 can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/8, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL/CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

Read footnote 5 to the Electrical Specifications table if using ADC774 to replace the HI-774.

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the output data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Timing specifications for stand-alone operation are listed in Table IV.

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3 LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

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PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. ADC774 Control Line Functions.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE III. Control Input Truth Table.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid		150	375	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing.

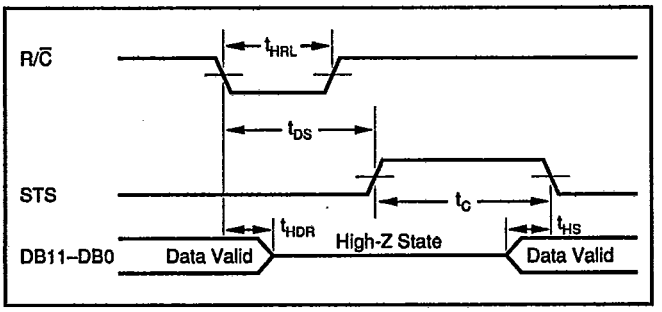

FIGURE 4. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

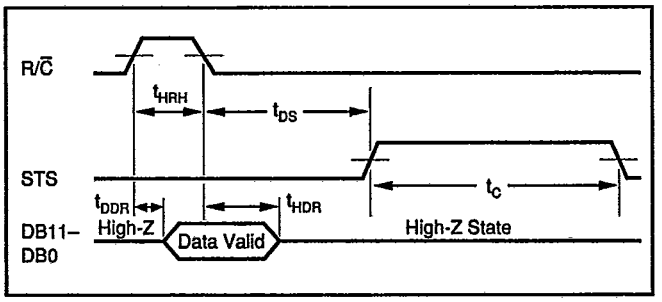

FIGURE 5. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ Is High.

CONVERSION START

The converter is commanded to initiate a conversion by a transition occuring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change state simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three-state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

READING OUTPUT DATA

After conversion is initiated, the output data buffers remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/8 and A_0. See Figure 7 and Table V for timing relationships and specifications.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{DSC}	STS Delay from CE		60	200	ns
t_{HEC}	CE Pulse Width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE Setup time	50	20		ns
t_{HSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time				
	12-bit cycle at 25°C		7.5	8	µs
	0 to +75°C			8.5	µs
	–55°C to +125°C			6	µs
	8-bit cycle at 25°C		5	5.3	µs
	0 to +75°C			5.7	µs
	–55° to +125°C			6	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SAR}	R/$\overline{C}$ to CE setup	0			ns
t_{HSR}	$\overline{CS}$-valid after CE low	0			ns
t_{HRR}	R/C high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid		150	375	ns

TABLE V. Timing Specifications.

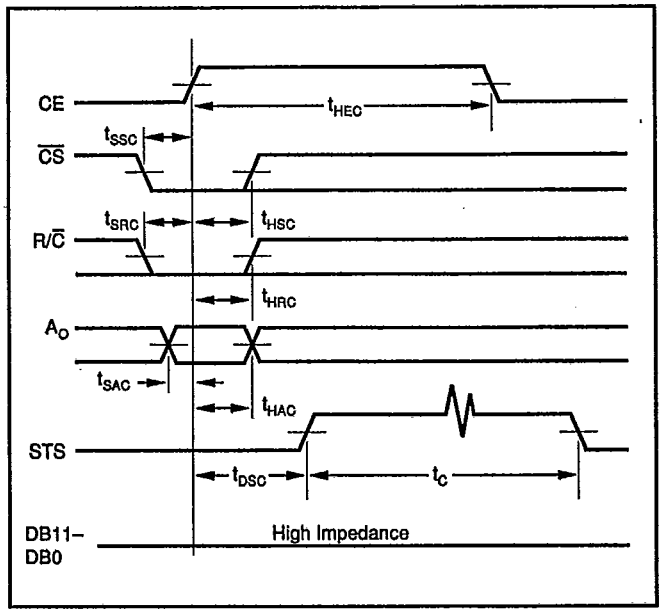

FIGURE 6. Conversion Cycle Timing.

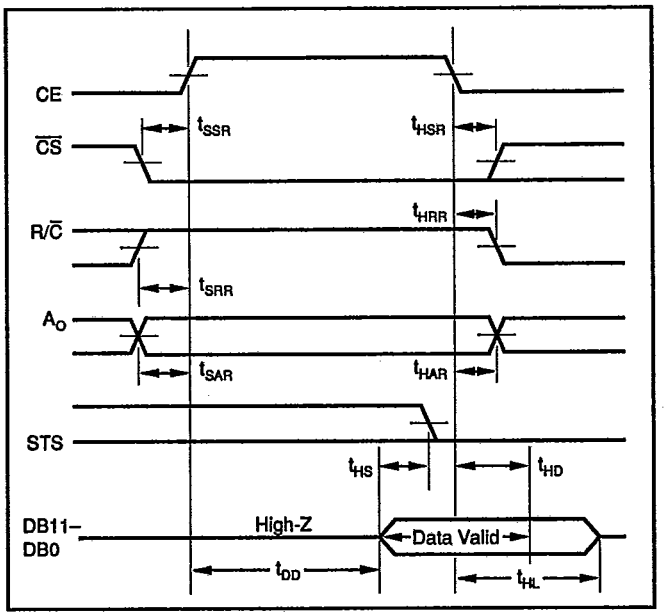

FIGURE 7. Read Cycle Timing.

desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0–DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

When 12/$\overline{8}$ is low, the data is presented in the form of two 8-bit bytes, with selection of the byte of interest accomplished by the state of A_0 during the read cycle. Connection of the ADC774 to an 8-bit bus for transfer of left-justified data is illustrated in Figure 9. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC774 guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as (t_{DD} + t_{HS}) before STATUS goes low. Refer to Figure 7 for these timing relationships.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

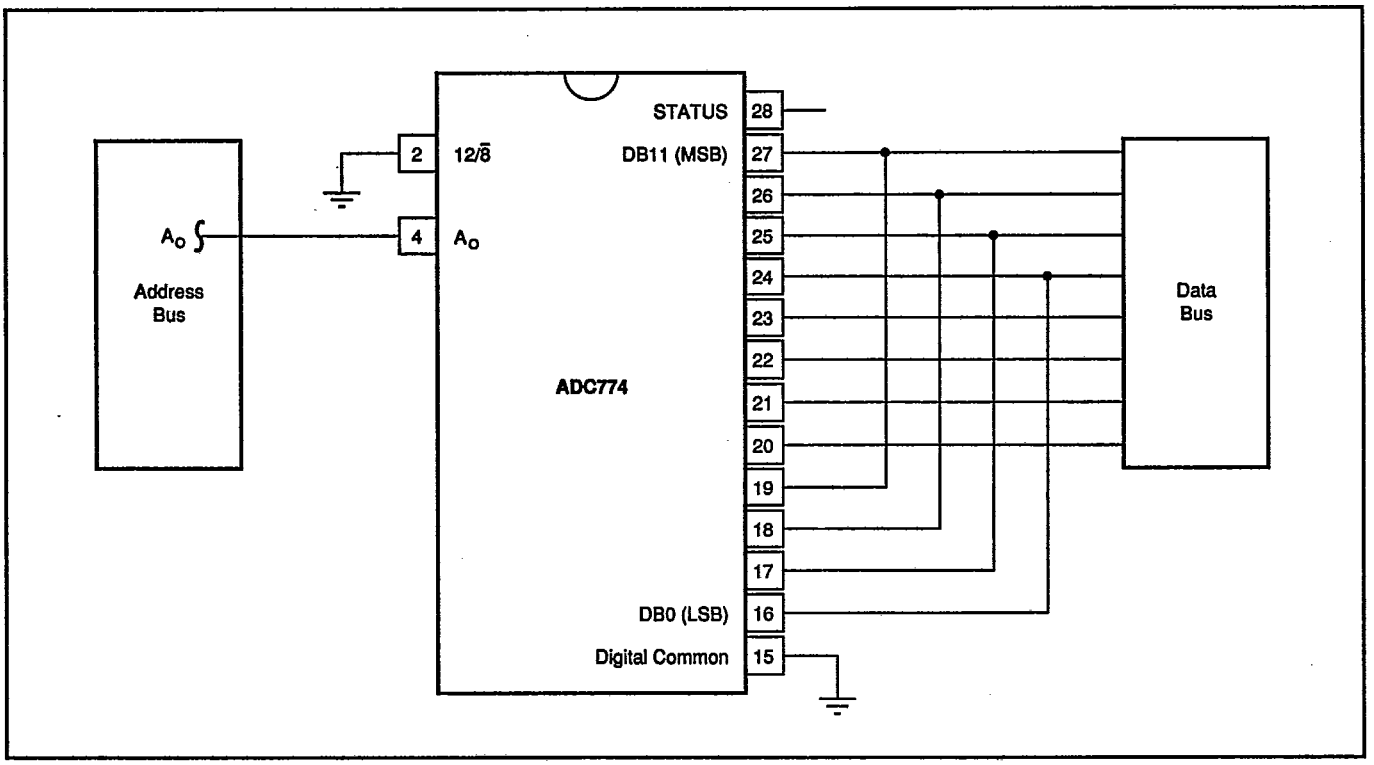

FIGURE 9. Connection to an 8-Bit Bus.