GaAs MMIC CSH 410

Target Data Sheet

- SP4T for GSM Mobile Phones
- GaAs PHEMT technology
- Low insertion loss
- High *IP3*
- No supply voltage needed
- Positive operating voltage: 2.7 to 5 V
- Leadless 16 pin package

ESD: **E**lectro**s**tatic **d**ischarge sensitive device,
observe handling precautions!

Type	**Marking**	**Ordering Code** (tape and reel)	**Package**
CSH 410	on request	on request	P-VQFN-16-2

Maximum Ratings

Parameter	**Symbol**	**Value**		**Unit**
		min.	**max.**	
Control voltage range	V_{CON}	– 5	+ 5.5	V
RF Input Power	P_{IN}	–	6	W
Thermal resistance	R_{th}	–	t.b.d.	K/W
Junction temperature	T_j	–	125	°C
Storage temperature	T_{stg}	– 55	150	°C

Electrical Characteristics

(T_A = 25 °C; V_{Cntrl} = 4.5 V; P_{IN} = 0 dBm; unless otherwise noted)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Insertion Loss TX1-ANT P_{IN} = + 34 dBm	ILTX1				dB
@ 1.0 GHz		–	0.6	0.8	
@ 2.0 GHz		–	0.8	1.0	
Insertion Loss TX1-ANT, RX1-ANT, RX2-ANT	ILxxx				dB
@ 1.0 GHz		–	0.6	0.8	
@ 2.0 GHz		–	0.8	1.0	
Isolation TX1-ANT P_{IN} = + 34 dBm	ISOL				dB
@ 1.0 GHz		25	–	–	
@ 2.0 GHz		21	–	–	
Isolation TX1-ANT, RX1-ANT, RX2-ANT	ISOL				dB
@ 1.0 GHz		25	–	–	
@ 2.0 GHz		21	–	–	
Return Loss[1] TX1-ANT P_{IN} = + 34 dBm	RLTX1				dB
@ 1.0 GHz		20	–	–	
@ 2.0 GHz		18	–	–	
Return Loss[1] TX1-ANT, RX1-ANT, RX2-ANT	RLxxx				dB
@ 1.0 GHz		20	–	–	
@ 2.0 GHz		18	–	–	
Harmonics TX1-ANT P_{IN} = + 34 dBm TX2-ANT P_{IN} = + 32 dBm	P_{Harm}				dBc
@ 1.0 GHz		65	–	–	
@ 2.0 GHz		65	–	–	
Gate leakage	I_L	–	0.1	–	mA
T_{Rise},T_{Fall} (10% RF to 90% RF)	–	–	10	–	ns
T_{ON},T_{OFF} (50% CNTRL - 90%/10% RF)	–	–	20	–	ns

Electrical Characteristics (cont'd)
(T_A = 25 °C; V_{Cntrl} = 4.5 V; P_{IN} = 0 dBm; unless otherwise noted)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input power for 1 dB compression @ 1.0 GHz @ 2.0 GHz	P_1	 – –	 38 –	 – –	dBm
Intermodulation intercept point	$IP3$	–	55	–	dBm

[1] Return Loss specified for Insertion Loss state only.

Control Voltage Levels

Logic Level	Control Ports	min. (VDC)	nom. (VDC)	max. (VDC)
0	V_1, V_2, V_3, V_4	– 0.25	0	+ 0.25
1	V_1, V_2	+ 4.5	+ 4.7	+ 5.5
1	V_3, V_4	+ 2.5	+ 2.7	+ 3.0

Control Voltage Logic

Switch Position	V_1	V_2	V_3	V_4
Tx1 → Ant	1	0	0	0
Tx2 → Ant	0	1	0	0
Rx1 → Ant	0	0	1	0
Rx2 → Ant	0	0	0	1

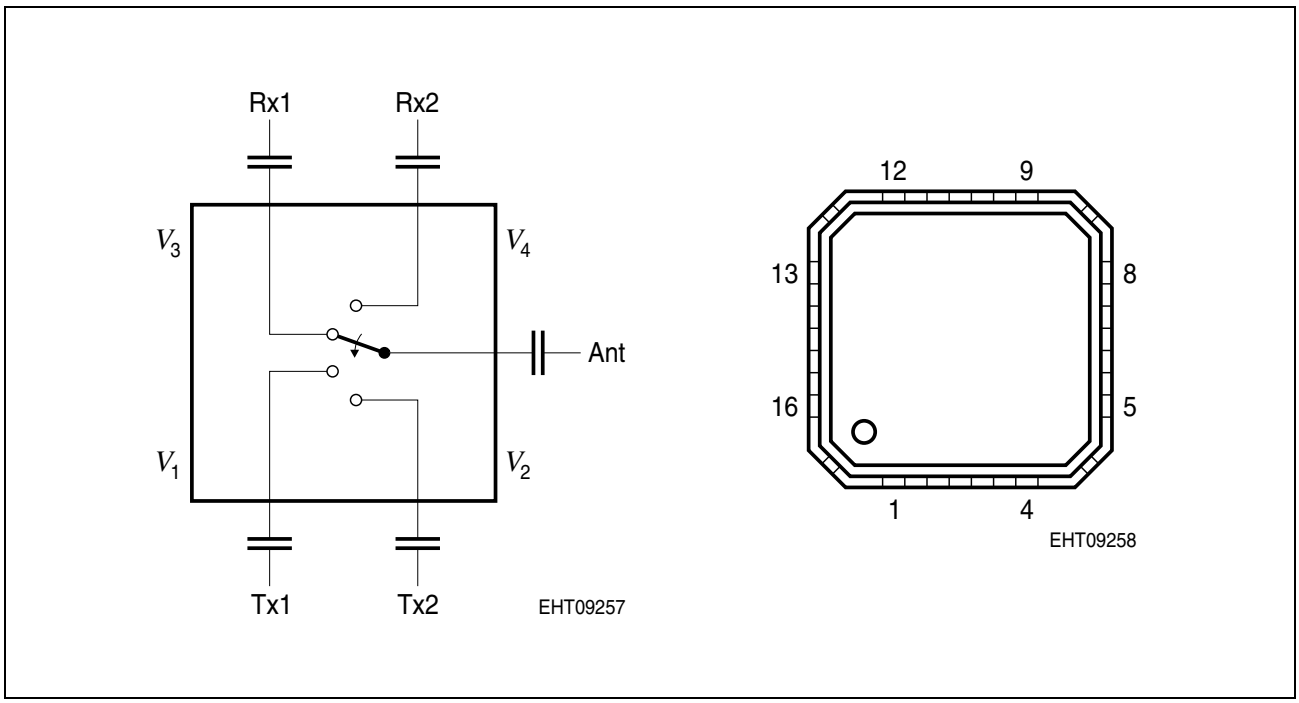

Figure 1 Functional Block Diagram

Pin Definitions and Functions

Pin No.	Function	Pin No.	Function
1	V_1	9	Rx1
2	Tx1	10	GND
3	GND	11	GND
4	Tx2	12	Rx2
5	GND	13	GND
6	V_2	14	V_4
7	V_3	15	GND
8	GND	16	Ant