Microprogram Controller
57110/67110 Data Sheet

Features/Benefits

- Address 512 Word Pages of Memory
- 8 Control Functions
- Microsubroutine Capability
- On-Chip Loop Counter
- 6 Flag Branch Inputs
- 4-Way Branching

Applications

- LSI Controller Circuit for Control of High Speed Disks, Line Printers, CRT Terminals
- Control of Microprogrammed High Performance Mini-computers with 4-Bit Slice Microprocessors

Ordering Information

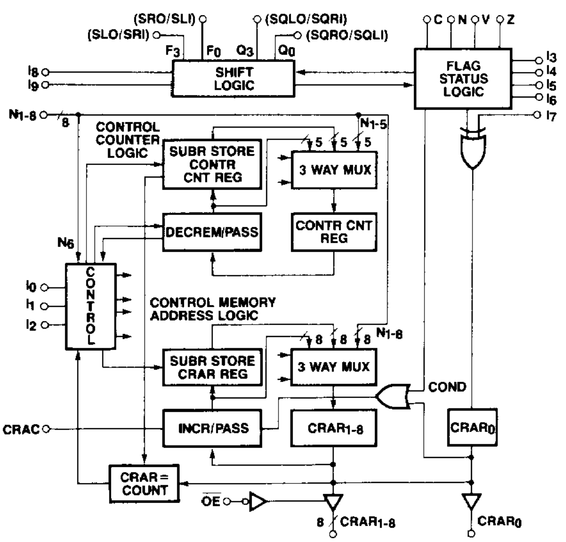
TEMPERATURE RANGE	PACKAGE	ORDER NUMBER
0°C to + 75°C	Ceramic	67110D
−55°C to +125°C	Ceramic	57110D

Description

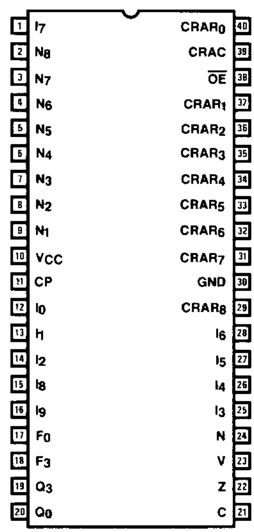
The 57110/67110 Microprogram Controller (MPC) is a member of the 57000/67000 Computer Logic family of high-performance bipolar compatible Schottky TTL components. The device is designed to work in conjunction with 4-Bit Slice Microprocessors and standard ROMs and PROMs for the design of extremely powerful computing systems. The power and flexibility of the MPC also allow it to be used for general purpose control applications. The MPC can directly address up to 512 words of microprogram control memory; larger memories can be accommodated using simple paging techniques.

One of up to six flag signals can be selected from the 5701/6701 4-Bit Slice to provide two-way conditional branching at every step in a microprogram on the value of the flag or its stored value. Four-way conditional branches are possible using an on-chip control counter. The MPC has 8 instructions including continue, conditional and unconditional jumps, conditional and unconditional subroutine jumps to a single level subroutine and subroutine return. Connections are provided to the 5701/6701 for a minimum set of shifting options. The MPC is a synchronous device using a single clock and can operate in systems with less than a 100ns microinstruction period. The device uses a single ±5 V power supply and is packaged in a standard 40 pin DIP.

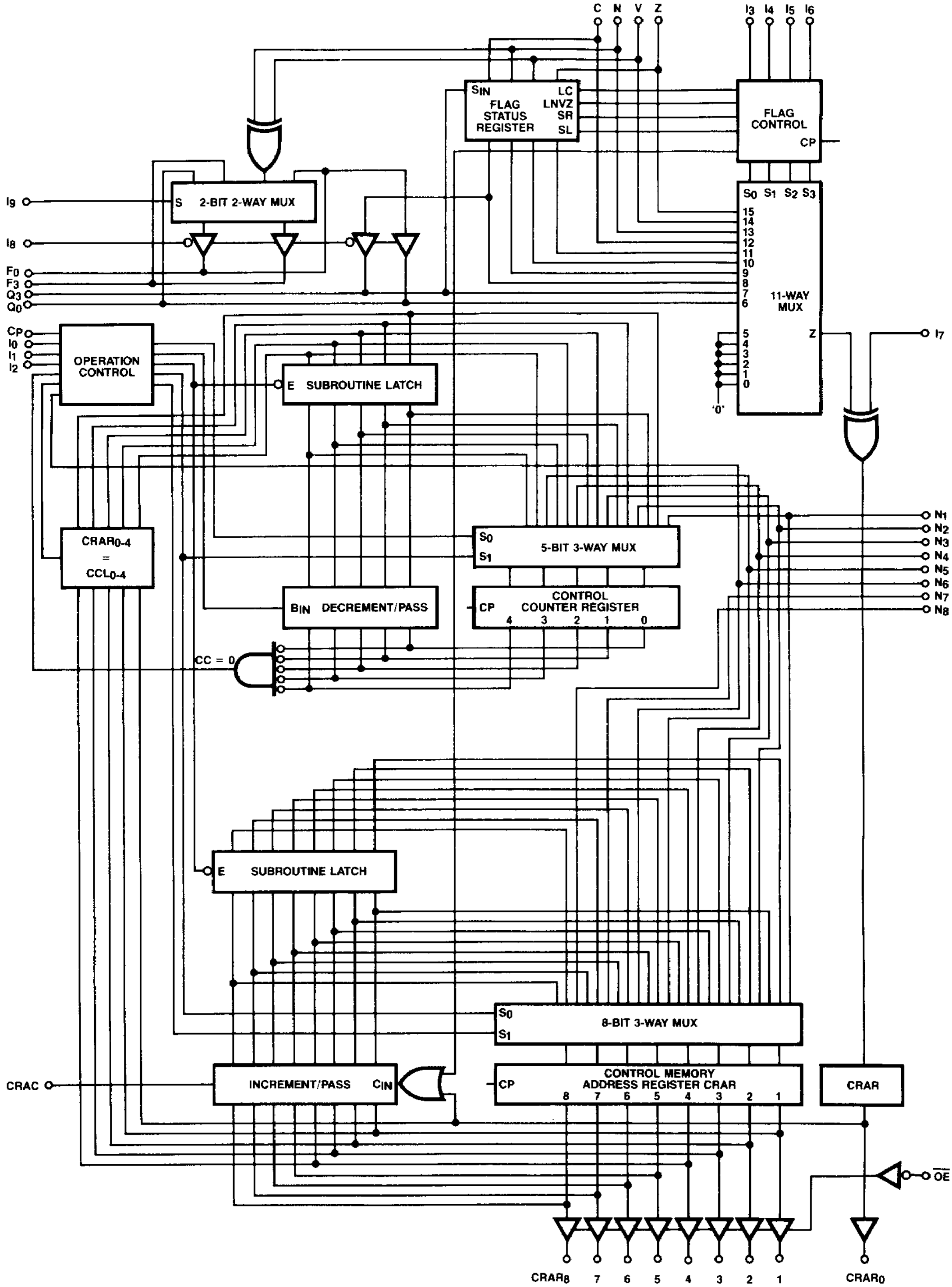
Block Diagram



Pin Configuration



57110/67110 Detailed Block Diagram



Detailed Description

The MPC is a synchronous machine. All changes visible on external pins except for the combinatorial Shift Logic occur on the single clock Low-to-High transition. Internally there are both dual rank registers (flip-flops) and single rank registers (latches). The latches are enabled when the clock is Low and this,together with some inputs defining information destinations, causes timing constraints such that certain input signals must not change while the clock is Low. These timing constraints are shown in the timing diagrams.

The MPC can be divided up into a number of sections. These sections are the Control ROM Address Register ($CRAR_{0-8}$) Logic, the Control Counter (CC) Logic, the Flag Status Logic, the Shifting Control for the 5701/6701 and the MPC Control Logic.

CRAR Logic

The CRAR is split up into two sections, an eight-bit section which can remain unchanged, be incremented, loaded from a subroutine temporary storage register latch and loaded from an 8-bit external field N_{1-8}. The one-bit section is the least significant bit of the Address Word and is directly driven from the output of the Flag Status Logic. The output of the Flag Status Logic therefore defines whether the next address is even or odd depending upon the condition of the selected flag signal. This allows two way branching at every clock period.

The eight-bit section of the register passes through a pass/increment unit and back through a 3-way multiplexer. The output of the pass/increment unit can also be stored in a temporary storage register where it may be returned to the CRAR at the end of a microsubroutine. The pass/increment also provides an end of page signal CRAC indicating that the CRAR is at address 510 or 511. Incrementation occurs in the pass/incrementor when the MPC is at an odd address ($CRAR_0 = 1$) or a Conditional Branch has been selected.

The output of the CRAR passes through buffers to output pins. The eight bit section buffers have three-state outputs so that when the Output Enable ($\overline{OE}$) is High external signals may drive the Control Memory Address lines.

Control Counter Logic

The Control Counter Logic is 5 bits wide with the logic very similar to the CRAR logic. The logic includes a register, pass/decrement unit, temporary subroutine register and a 3-way input multiplexer which can select information from the external field bits N_{1-5}, the temporary storage register, or the pass/decrement unit. The counter logic is used during the two conditional jump instructions. Each time the MPC encounters a conditional jump instruction, the control counter register is tested for zero and decremented. If the register was zero then the MPC instead of performing a jump instruction continues on to the next address pair. The next time the conditional jump instruction occurs the procedure is repeated, but now the value of the register is one less. The control counter register can be loaded from the N_{1-5} inputs on receipt of a Continue Load Control Counter instruction.

Flag Status Logic

The Flag Status Logic consists of a loadable Shift Left/Shift Right register, an eleven-way multiplexer, an exclusive OR gate and a small amount of control logic. The shift register can be loaded with four flags C, N, V, Z, with separate loading selection for C and the group NVZ. The register can be shifted one place Left with N going to C, V to N, etc., and a logic zero being pulled into Z. The C register bit is placed on the bidirectional input/output line Q_0 and would most likely in a system enter the least significant bit of the Q register in the 5701/6701. A Right shift causes C to be loaded from Q_0 this time acting as an input, and what is in C going to N, etc.

The eleven-way multiplexer can be used via the select and control lines I_{3-6} to select one of the following signals: Stored C, N, V, Z, Present C, N, V, Z, logic 0, Q_0 and Q_3. All of these signals can be inverted by having $I_7 = 1$, enabling branching on $\overline{C}$, $\overline{N}$, etc. The output of the Flag Status Logic Ex Or gate is the input to the least significant CRAR register bit. The Flag Status Logic also provides a signal to the pass/increment unit to indicate that a conditional branch is present and the unit should increment.

Shift Control Logic

The Shift Control Logic provides the connections for a minimum set of useful 5701/6701 shifting options. Two control inputs I_8 and I_9 are used to select the desired option. I_8 indicates which bidirectional buffers are actively sending information and I_9 selects various signals to apply to the shift lines of the 5701/6701. Provision is made in the shifting logic to provide correct sign information during right arithmetic shifts by an exclusive $\overline{OR}$ of the N and V signals.

Control Logic

The Control Logic uses the instruction control inputs I_{0-2}, the test zero output of the Control Counter Logic, and the signal which indicates that the Control Counter temporary subroutine storage register contains the same value as the five least significant bits of the CRAR register. These signals are then encoded into the control signals necessary to implement the MPC instructions.

Two flip-flops are included in the control logic. The first remembers that the MPC is in a microsubroutine and when a return is encountered, it is obeyed if the flip-flop is set; if the flip-flop is clear the return is ignored. The second flip-flop indicates that a Preprogrammed Return Subroutine is in progress called by instruction 101, and the MPC should automatically return when equivalence of the CRAR and CC subroutine latch is achieved. Both these flip-flops are automatically cleared during power on if clock is held in the low state and may be reset under microprogram control by loading the Control Counter with $N_6 = 1$.

Table I—MPC Control Options

CONTROL CODE			CONTROL ACTION	ADDRESS FIELD DESTINATION
I_2	I_1	I_0		
0	0	0	Continue to next μinstruction	None
0	0	1	Continue to next μinstruction	Control Counter, Clear SRFF if $N_6 = 1$
0	1	0	Jump to next μinstruction if Control Counter $\neq 0$, Decrement Control Counter	None/CRAR (Cond. Jump)
0	1	1	Subroutine Jump to next μinstruction if Control Counter $\neq 0$, Decrement Control Counter	None/CRAR (Cond. Subr. Jump)
1	0	0*	Return from Subroutine	None
1	0	1**	Jump to next μinstruction Return from Subroutine when Control Counter Subroutine Latch $\equiv CRAR_{0\text{-}4}$	CRAR (Jump Subroutine)
1	1	0	Jump to next μinstruction	CRAR (Jump)
1	1	1	Subroutine Jump to next μinstruction	CRAR (Jump Subroutine)

* The MPC will only return to the calling program if it entered a Subroutine via a Subroutine Jump instruction; otherwise it will continue to the next μinstruction in sequence.

**This operation allows the MPC to branch to a section of code, perform the operations outlined by the code and return after a preprogrammed CROM address has been reached or if a return is encountered.

Table II—Flag Status Control Options

CONTROL CODE				ACTION		
I_6	I_5	I_4	I_3	OPERATION	$CRAR_0$	BRANCH
0	0	0	0	None	I_7	Unconditional*
0	0	0	1	Store C	I_7	Unconditional*
0	0	1	0	Store N, V, Z	I_7	Unconditional**
0	0	1	1	Store C, N, V, Z	I_7	Unconditional*
0	1	0	0	Shift Flag Register into Q_0	I_7	Unconditional*
0	1	0	1	Shift Flag Register out of Q_0	I_7	Unconditional*
0	1	1	0	Instantaneous value of Q_0 to $CRAR_0$	$Q_0 \veebar I_7$	Conditional**
0	1	1	1	Instantaneous value of Q_3 to $CRAR_0$	$Q_3 \veebar I_7$	Conditional**
1	0	0	0	Stored value of C to $CRAR_0$	$SC \veebar I_7$	Conditional**
1	0	0	1	Stored value of N to $CRAR_0$	$SN \veebar I_7$	Conditional**
1	0	1	0	Stored value of V to $CRAR_0$	$SV \veebar I_7$	Conditional**
1	0	1	1	Stored value of Z to $CRAR_0$	$SZ \veebar I_7$	Conditional**
1	1	0	0	Instantaneous value of C to $CRAR_0$	$C \veebar I_7$	Conditional**
1	1	0	1	Instantaneous value of N to $CRAR_0$	$N \veebar I_7$	Conditional*
1	1	1	0	Instantaneous value of V to $CRAR_0$	$V \veebar I_7$	Conditional**
1	1	1	1	Instantaneous value of Z to $CRAR_0$	$Z \veebar I_7$	Conditional**

Code bit I_7 inverts the status of output line so that the condition is dependent upon $\overline{C}$, etc. For the first six entries in the table, if $I_7 = 0$ there is an unconditional branch to X, 0; if $I_7 = 1$, an unconditional branch to X, 1. SC, SN, SV, SZ are Contents of Carry, Sign, Overflow, and Zero Flip Flops.

* Incrementation of $CRAR_{1\text{-}8}$ occurs if $CRAR_0 = 1$.

**Incrementation of $CRAR_{1\text{-}8}$ always occurs.

Table III—Shift Control Options

CONTROL CODE			BIDIRECTIONAL SHIFT LINES ACTING AS OUTPUTS			
I_9	I_8	SHIFTING OPERATION	F_3 (SLO/SRI)	F_0 (SRO/SLI)	Q_3 (SQLO/SQRI)	Q_0 (SQRO/SQLI)
0	0	Arithmetic Shift Left	—	Q_3	—	Flag (SC)
0	1	Arithmetic Shift Right	$N \veebar V$	—	F_0	—
1	0	Rotate Shift Left	—	F_3	—	Flag (SC)
1	1	Rotate Shift Right	F_0	—	F_0	—

— High Impedance State

SC Contents of Carry Flip Flop

Table IV—Next Address Table

ADDRESSES—*In Pairs* *Even A, 0 etc.*
Odd A, 1 etc.

INCREMENT—*If Present Address Odd or Conditional*

INSTRUCTION	FLAG STATUS	PRESENT ADDRESS	NEXT ADDRESS	COMMENTS
Continue	Unc. '0'	A, 0	A, 0	Locked Loop
	Unc. '1'	A, 0	A, 1	Next Consecutive Address
	Unc. '0'	A, 1	A + 1, 0	Next Consecutive Address
	Unc. '1'	A, 1	A + 1, 1	Skip Over A + 1, 0
	Cond.	A, 0	A + 1, Cond.	Skip Over A, 1
	Cond.	A, 1	A + 1, Cond.	Next Address Pair
Jump	Unc. '0'	A, X	N, 0	Jump to N, 0
	Unc. '1'	A, X	N, 1	Jump to N, 1
	Cond.	A, X	N, Cond.	Jump to N, Cond.
Return	Unc. '0'	A, X	R, 0 or R + 1, 0	Return Address is incremented if $CRAR_0$ = 1 or Conditional Branch Subroutine Entry is made
	Unc. '1'	A, X	R, 1 or R + 1, 1	
	Cond.	A, X	R, Cond. or R + 1, Cond.	

X = 0, or 1

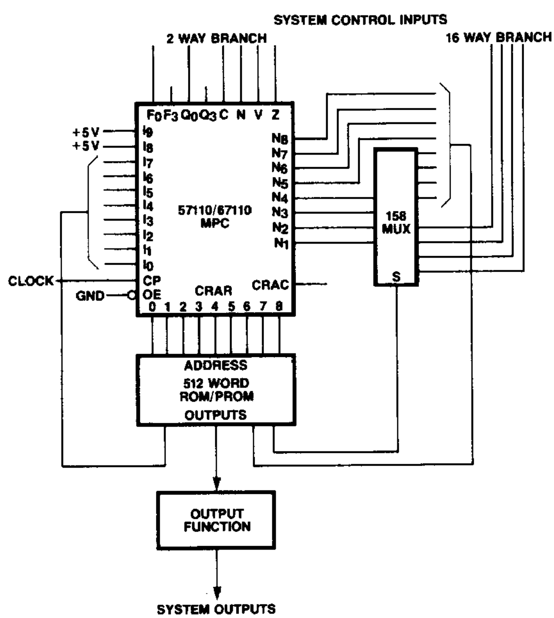
Applications

The 57110/67110 Microprogram controller is a general purpose LSI control element which can be used efficiently in all types of Microprogrammed systems. The device is a powerful microprogrammed sequencer with the additional features of Flag Status multiplexer and storage, an on-chip loop counter with its subroutine register and some shifting connection logic for use with popular Bit-Slice Microprocessors.

The familiar application of such a powerful controller is in the control of microprogrammed high-performance computers. However, the economics of LSI and flexibility of the microprogrammed concept have now made the Microprogram Controller an important and essential concept in all types of high performance digital control. The 57110/67110 is therefore suitable for the central control of disk, tape, CRT and line printers where high data rates and flexibility are necessary.

All of these systems, although they differ in detail, follow the same concept. Inputs from the system to be controlled are sent to the Controller and are examined either through the Flag Status Logic and/or through a Multiplexer connected to the address lines N_{1-8}. The Flag Status inputs allow a two-way branch depending upon the value of the chosen Flag Status input, while the use of a multiplexer at the N inputs allows a 2M way branch on M input variables. The MPC addresses the control memory, some outputs of which are fed back to control the MPC at the next time period, while other outputs of the control memory can form the system outputs either directly or more efficiently via some MSI networks.

Typical Control System Connection



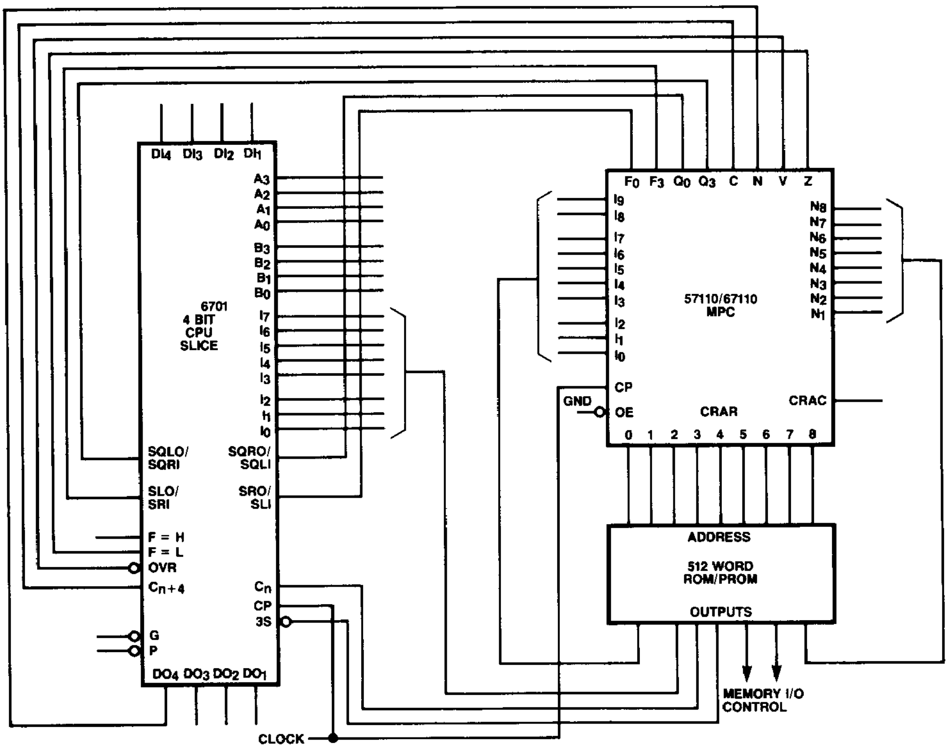
57110/67110 with 4-Bit Slice

The 57110/67110 Microprogram Controller is the ideal LSI element for control of systems which incorporate popular 4-Bit Slice Microprocessors. The 57110/67110 has Flag Status logic which can directly connect to the Flags such as Carry, Sign, Overflow and Zero from the 4-Bit Slice, and allow 2 way branching in the microprogram on the value of one of these Flags. In addition these Flags can be stored for later examination. The extremities of the Q extension register can also be examined by the Flag Status Logic to assist in Multiply and Shifting operations.

The 57110/67110 also has the connections to provide a minimum set of shifting functions which include both double and single length arithmetic shifts and logical end-around shifts.

The Microprogram Controller addresses the control memory which provides the feedback necessary for determining the next operation and control memory address, and also the micro-control signals for the instruction fields of the 4-Bit Slice. The clocks of both the Microprogram Controller and 4-Bit Slice are driven in parallel to make a single clock synchronous system.

57110/67110
6701
INTERCONNECTIONS



Electrical Characteristics Over Operating Temperature Range (unless otherwise noted)

67110: V_{CC} = 5V ±5%, T_A = 0°C to +75°C; 57110: V_{CC} = 5V ±10%, T_A = −55°C to +125°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input HIGH Level Voltage		2.0			V
V_{IL}	Input LOW Level Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA, T_A = 25°C		−1.0	−1.5	V
V_{OH}	Output HIGH level Voltage	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = −2.0mA	2.4	3.0		V
V_{OL}	Output LOW level Voltage	V_{CC} = Min, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 8mA		0.30	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_{IN} = 5.5V			1.0	mA
I_{IH}	Input HIGH Level Current I_{0-9}, $\overline{OE}$, CP	V_{CC} = Max, V_{IN} = 2.4V			25	μA
	N_{1-8}, C,N,V,Z				50	μA
	Q_0, Q_3, F_0, F_3	Used as input			100	μA
I_{IL}	Input LOW Level Current I_{0-9}, $\overline{OE}$, CP	V_{CC} = Max, V_{IN} = 0.5V			250	μA
	N_{1-8}, C, N, V, Z				1.0	mA
	Q_0, Q_3, F_0, F_3	Used as input			0.5	mA
I_{OZ}	Output Off State (high impedance) Current $CRAC_{1-8}$	V_{CC} = Max, V_{OUT} = 0.5V			−50	μA
		V_{CC} = Max, V_{OUT} = 2.4V			50	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0V	20		90	mA
I_{CC}	Supply Current	V_{CC} = Max		159	254	mA

Switching Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	57110 MIN	57110 TYP	57110 MAX	67110 MIN	67110 TYP	67110 MAX
	Delay from $\overline{OE}$ to:	C_L = 15pF, See Timing Diagrams						
t_{HZ}, t_{LZ}	$CRAR_{1-8}$ High Impedance State		5	12	25	5	12	20
t_{ZL}, t_{ZH}	$CRAR_{1-8}$ Active State		5	10	25	5	10	20
	Delay from I_8 to:							
t_{HZ}, t_{LZ}	F_0,F_3,Q_0,Q_3 High Impedance State		5	15	34	5	15	28
t_{ZL}, t_{HZ}	F_0,F_3,$Q_0$$Q_3$ Active State		5	18	40	5	18	32
t_{PHL}, t_{PLH}	Delay from I_9 to F_0, F_3	C_L = 30pF, S_1, S_2 Closed, See Timing Diagrams	5	14	32	5	14	27
t_{PHL}, t_{PLH}	Delay from N, V to F_3		5	15	32	5	15	27
t_{PHL}, t_{PLH}	Delay from F_0 to F_3		4	10	20	4	10	18
t_{PHL}, t_{PLH}	Delay from F_3 to F_0		4	10	20	4	10	18
t_{PHL}, t_{PLH}	Delay from Q_0 to F_0		4	10	20	4	10	18
t_{PHL}, t_{PLH}	Delay from F_0 to Q_3		4	10	20	4	10	18
	Delay from Clock Low to High Transition to:							
t_{PHL}, t_{PLH}	Q_0		15	35	60	15	35	55
t_{PHL}, t_{PLH}	$CRAR_{0-8}$		6	17	40	6	17	35
t_{PHL}, t_{PLH}	CRARC		10	23	48	10	23	42
	Set-Up Time Before the High to Low Transition of Clock:							
t_{SI}	I_0, I_1, I_2, I_3, I_4, I_5, I_6		5	−5		5	−5	
	Set-Up Time Before the Low to High Transition of Clock:							
t_{SD}	I_7		16	6		16	6	
t_{SD}	C, N, V, Z, Q_0, Q_3		28	11		20	11	
t_{SD}	N_{1-8}		30	15		24	15	
	Hold Time After the Low to High Transition of Clock:							
t_{HI}	I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7		18	6		15	6	
t_{HD}	C, N, V, Z, Q_0, Q_3		25	13		22	13	
t_{HD}	N_{1-8}		12	5		12	5	
t_{CPL}	Minimum Clock Low Pulse Width			18	40		18	30
t_{CPH}	Minimum Clock High Pulse Width			45	80		45	70

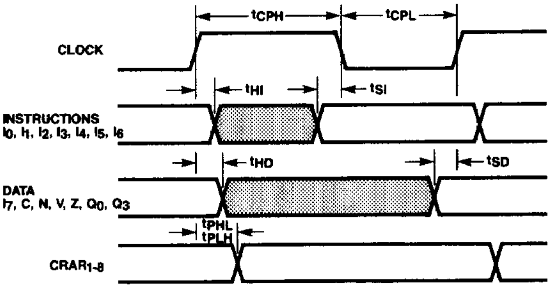
Typical values are at V_{CC} = 5.0V and T_A = 25°C.
In order to guarantee that control logic flip flops are reset during power on, the Clock Pulse must be held LOW (0.5V) until V_{CC} is at V_{CC} min.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Current	100mA
Ambient Temperature	−55°C to +125°C
Storage Temperature	−65°C to +125°C

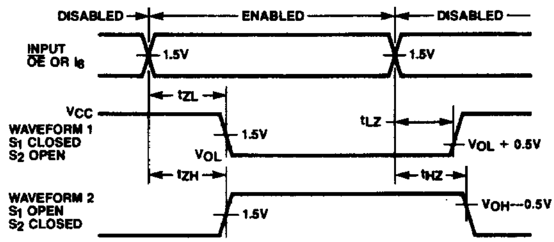
Stresses above and extended time at Absolute Maximum Ratings may cause permanent damage or affect device reliability. Functional operation at these limits is neither guaranteed nor implied.

Timing Diagrams



Notes:
Shaded areas denote DON'T CARE conditions.
All delays, set-up and hold times measured at 1.5V level.

Three State Delays



Notes:
Waveform 1 requires internal conditions such that the output is LOW except when disabled.
Waveform 2 requires internal conditions such that the output is HIGH except when disabled.

Standard Test Loads