

# 1GB Registered DDR SDRAM DIMM

## EBD10RD4ADFA (128M words × 72 bits, 1 Rank)

### Description

The EBD10RD4ADFA is 128M words × 72 bits, 1 rank Double Data Rate (DDR) SDRAM registered module, mounting 18 pieces of 512M bits DDR SDRAM sealed in TSOP package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 2-bit prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each TSOP on the module board.

### Features

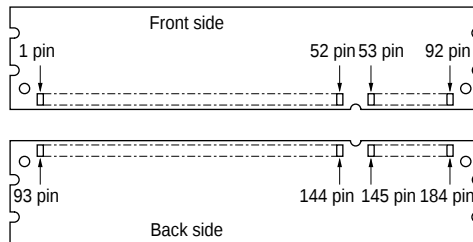
- 184-pin socket type dual in line memory module (DIMM)
  - PCB height: 30.48mm
  - Lead pitch: 1.27mm
- 2.5V power supply
- Data rate: 333Mbps/266Mbps (max.)
- 2.5 V (SSTL\_2 compatible) I/O
- Double Data Rate architecture; two data transfers per clock cycle
- Bi-directional, data strobe (DQS) is transmitted /received with data, to be used in capturing data at the receiver
- Data inputs and outputs are synchronized with DQS
- 4 internal banks for concurrent operation (Component)
- DQS is edge aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data referenced to both edges of DQS
- Auto precharge option for each burst access
- Programmable burst length: 2, 4, 8
- Programmable /CAS latency (CL): 2, 2.5
- Refresh cycles: (8192 refresh cycles /64ms)
  - 7.8μs maximum average periodic refresh interval
- 2 variations of refresh
  - Auto refresh
  - Self refresh
- 1 piece of PLL clock driver, 2 pieces of register driver and 1 piece of serial EEPROM (2k bits) for Presence Detect (SPD) on PCB.

## Ordering Information

| Part number     | Data rate<br>Mbps (max.) | Component<br>JEDEC speed bin* <sup>1</sup><br>(CL-tRCD-tRP) | Package      | Contact<br>pad | Mounted devices          |
|-----------------|--------------------------|-------------------------------------------------------------|--------------|----------------|--------------------------|
| EBD10RD4ADFA-6B | 333                      | DDR333B (2.5-3-3)                                           | 184-pin DIMM | Gold           | EDD5104ADTA-6B           |
| EBD10RD4ADFA-7A | 266                      | DDR266A (2-3-3)                                             |              |                | EDD5104ADTA-6B, -7A      |
| EBD10RD4ADFA-7B | 266                      | DDR266B (2.5-3-3)                                           |              |                | EDD5104ADTA-6B, -7A, -7B |

Note: 1. Module /CAS latency = component CL + 1

## Pin Configurations



| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name  | Pin No. | Pin name  |
|---------|----------|---------|----------|---------|-----------|---------|-----------|
| 1       | VREF     | 47      | DQS8     | 93      | VSS       | 139     | VSS       |
| 2       | DQ0      | 48      | A0       | 94      | DQ4       | 140     | DM8/DQS17 |
| 3       | VSS      | 49      | CB2      | 95      | DQ5       | 141     | A10       |
| 4       | DQ1      | 50      | VSS      | 96      | VDD       | 142     | CB6       |
| 5       | DQS0     | 51      | CB3      | 97      | DM0/DQS9  | 143     | VDD       |
| 6       | DQ2      | 52      | BA1      | 98      | DQ6       | 144     | CB7       |
| 7       | VDD      | 53      | DQ32     | 99      | DQ7       | 145     | VSS       |
| 8       | DQ3      | 54      | VDD      | 100     | VSS       | 146     | DQ36      |
| 9       | NC       | 55      | DQ33     | 101     | NC        | 147     | DQ37      |
| 10      | /RESET   | 56      | DQS4     | 102     | NC        | 148     | VDD       |
| 11      | VSS      | 57      | DQ34     | 103     | NC        | 149     | DM4/DQS13 |
| 12      | DQ8      | 58      | VSS      | 104     | VDD       | 150     | DQ38      |
| 13      | DQ9      | 59      | BA0      | 105     | DQ12      | 151     | DQ39      |
| 14      | DQS1     | 60      | DQ35     | 106     | DQ13      | 152     | VSS       |
| 15      | VDD      | 61      | DQ40     | 107     | DM1/DQS10 | 153     | DQ44      |
| 16      | NC       | 62      | VDD      | 108     | VDD       | 154     | /RAS      |
| 17      | NC       | 63      | /WE      | 109     | DQ14      | 155     | DQ45      |
| 18      | VSS      | 64      | DQ41     | 110     | DQ15      | 156     | VDD       |
| 19      | DQ10     | 65      | /CAS     | 111     | NC        | 157     | /CS0      |
| 20      | DQ11     | 66      | VSS      | 112     | VDD       | 158     | NC        |
| 21      | CKE0     | 67      | DQS5     | 113     | NC        | 159     | DM5/DQS14 |
| 22      | VDD      | 68      | DQ42     | 114     | DQ20      | 160     | VSS       |
| 23      | DQ16     | 69      | DQ43     | 115     | A12       | 161     | DQ46      |
| 24      | DQ17     | 70      | VDD      | 116     | VSS       | 162     | DQ47      |
| 25      | DQS2     | 71      | NC       | 117     | DQ21      | 163     | NC        |
| 26      | VSS      | 72      | DQ48     | 118     | A11       | 164     | VDD       |
| 27      | A9       | 73      | DQ49     | 119     | DM2/DQS11 | 165     | DQ52      |

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name  | Pin No. | Pin name  |
|---------|----------|---------|----------|---------|-----------|---------|-----------|
| 28      | DQ18     | 74      | VSS      | 120     | VDD       | 166     | DQ53      |
| 29      | A7       | 75      | NC       | 121     | DQ22      | 167     | NC        |
| 30      | VDD      | 76      | NC       | 122     | A8        | 168     | VDD       |
| 31      | DQ19     | 77      | VDD      | 123     | DQ23      | 169     | DM6/DQS15 |
| 32      | A5       | 78      | DQS6     | 124     | VSS       | 170     | DQ54      |
| 33      | DQ24     | 79      | DQ50     | 125     | A6        | 171     | DQ55      |
| 34      | VSS      | 80      | DQ51     | 126     | DQ28      | 172     | VDD       |
| 35      | DQ25     | 81      | VSS      | 127     | DQ29      | 173     | NC        |
| 36      | DQS3     | 82      | VDDID    | 128     | VDD       | 174     | DQ60      |
| 37      | A4       | 83      | DQ56     | 129     | DM3/DQS12 | 175     | DQ61      |
| 38      | VDD      | 84      | DQ57     | 130     | A3        | 176     | VSS       |
| 39      | DQ26     | 85      | VDD      | 131     | DQ30      | 177     | DM7/DQS16 |
| 40      | DQ27     | 86      | DQS7     | 132     | VSS       | 178     | DQ62      |
| 41      | A2       | 87      | DQ58     | 133     | DQ31      | 179     | DQ63      |
| 42      | VSS      | 88      | DQ59     | 134     | CB4       | 180     | VDD       |
| 43      | A1       | 89      | VSS      | 135     | CB5       | 181     | SA0       |
| 44      | CB0      | 90      | NC       | 136     | VDD       | 182     | SA1       |
| 45      | CB1      | 91      | SDA      | 137     | CK0       | 183     | SA2       |
| 46      | VDD      | 92      | SCL      | 138     | /CK0      | 184     | VDDSPD    |

**Pin Description**

| Pin name                 | Function                               |
|--------------------------|----------------------------------------|
| A0 to A12                | Address input                          |
|                          | Row address      A0 to A12             |
|                          | Column address    A0 to A9, A11, A12   |
| BA0, BA1                 | Bank select address                    |
| DQ0 to DQ63              | Data input/output                      |
| CB0 to CB7               | Check bit (Data input/output)          |
| /RAS                     | Row address strobe command             |
| /CAS                     | Column address strobe command          |
| /WE                      | Write enable                           |
| /CS0                     | Chip select                            |
| CKE0                     | Clock enable                           |
| CK0                      | Clock input                            |
| /CK0                     | Differential clock input               |
| DQS0 to DQS8             | Input and output data strobe           |
| DM0 to DM8/DQS9 to DQS17 | Input and output data strobe           |
| SCL                      | Clock input for serial PD              |
| SDA                      | Data input/output for serial PD        |
| SA0 to SA2               | Serial address input                   |
| VDD                      | Power for internal circuit             |
| VDDSPD                   | Power for serial EEPROM                |
| VREF                     | Input reference voltage                |
| VSS                      | Ground                                 |
| VDDID                    | VDD identification flag                |
| /RESET                   | Reset pin (forces register inputs low) |
| NC                       | No connection                          |

**Serial PD Matrix<sup>\*1</sup>**

| Byte No. | Function described                                                            | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex value | Comments                    |
|----------|-------------------------------------------------------------------------------|------|------|------|------|------|------|------|------|-----------|-----------------------------|
| 0        | Number of bytes utilized by module manufacturer                               | 1    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 80H       | 128                         |
| 1        | Total number of bytes in serial PD device                                     | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 0    | 08H       | 256 byte                    |
| 2        | Memory type                                                                   | 0    | 0    | 0    | 0    | 0    | 1    | 1    | 1    | 07H       | SDRAM DDR                   |
| 3        | Number of row address                                                         | 0    | 0    | 0    | 0    | 1    | 1    | 0    | 1    | 0DH       | 13                          |
| 4        | Number of column address                                                      | 0    | 0    | 0    | 0    | 1    | 1    | 0    | 0    | 0CH       | 12                          |
| 5        | Number of DIMM ranks                                                          | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 01H       | 1                           |
| 6        | Module data width                                                             | 0    | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 48H       | 72 bits                     |
| 7        | Module data width continuation                                                | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 00H       | 0 (+)                       |
| 8        | Voltage interface level of this assembly                                      | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 04H       | SSTL 2.5V                   |
| 9        | DDR SDRAM cycle time, CL = X<br>-6B                                           | 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    | 60H       | CL = 2.5 <sup>*3</sup>      |
|          | -7A, -7B                                                                      | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 75H       |                             |
| 10       | SDRAM access from clock (tAC)<br>-6B                                          | 0    | 1    | 1    | 1    | 0    | 0    | 0    | 0    | 70H       | 0.70ns <sup>*3</sup>        |
|          | -7A, -7B                                                                      | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 75H       | 0.75ns <sup>*3</sup>        |
| 11       | DIMM configuration type                                                       | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 02H       | ECC                         |
| 12       | Refresh rate/type                                                             | 1    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 82H       | 7.8 $\mu$ s<br>Self refresh |
| 13       | Primary SDRAM width                                                           | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 04H       | $\times 4$                  |
| 14       | Error checking SDRAM width                                                    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 04H       | $\times 4$                  |
| 15       | SDRAM device attributes:<br>Minimum clock delay back-to-back<br>column access | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 01H       | 1 CLK                       |
| 16       | SDRAM device attributes:<br>Burst length supported                            | 0    | 0    | 0    | 0    | 1    | 1    | 1    | 0    | 0EH       | 2, 4, 8                     |
| 17       | SDRAM device attributes: Number of<br>banks on SDRAM device                   | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 0    | 04H       | 4                           |
| 18       | SDRAM device attributes:<br>/CAS latency                                      | 0    | 0    | 0    | 0    | 1    | 1    | 0    | 0    | 0CH       | 2/2.5                       |
| 19       | SDRAM device attributes:<br>/CS latency                                       | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 01H       | 0                           |
| 20       | SDRAM device attributes:<br>/WE latency                                       | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 0    | 02H       | 1                           |
| 21       | SDRAM module attributes                                                       | 0    | 0    | 1    | 0    | 0    | 1    | 1    | 0    | 26H       | Registered                  |
| 22       | SDRAM device attributes: General                                              | 1    | 1    | 0    | 0    | 0    | 0    | 0    | 0    | C0H       | $\pm 0.2V$                  |
| 23       | Minimum clock cycle time at CLX - 0.5<br>-6B, -7A                             | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 75H       | CL = 2 <sup>*3</sup>        |
|          | -7B                                                                           | 1    | 0    | 1    | 0    | 0    | 0    | 0    | 0    | A0H       |                             |
| 24       | Maximum data access time (tAC) from<br>clock at CLX - 0.5<br>-6B              | 0    | 1    | 1    | 1    | 0    | 0    | 0    | 0    | 70H       | 0.70ns <sup>*3</sup>        |
|          | -7A, -7B                                                                      | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 75H       | 0.75ns <sup>*3</sup>        |
| 25       | Minimum clock cycle time at CLX - 1                                           | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 00H       |                             |
| 26       | Maximum data access time (tAC) from<br>clock at CLX - 1                       | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 00H       |                             |
| 27       | Minimum row precharge time (tRP)<br>-6B                                       | 0    | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 48H       | 18ns                        |
|          | -7A, -7B                                                                      | 0    | 1    | 0    | 1    | 0    | 0    | 0    | 0    | 50H       | 20ns                        |

| Byte No. | Function described                                                  | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex value | Comments             |
|----------|---------------------------------------------------------------------|------|------|------|------|------|------|------|------|-----------|----------------------|
| 28       | Minimum row active to row active delay (tRRD)<br>-6B                | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 0    | 30H       | 12ns                 |
|          | -7A, -7B                                                            | 0    | 0    | 1    | 1    | 1    | 1    | 0    | 0    | 3CH       | 15ns                 |
| 29       | Minimum /RAS to /CAS delay (tRCD)<br>-6B                            | 0    | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 48H       | 18ns                 |
|          | -7A, -7B                                                            | 0    | 1    | 0    | 1    | 0    | 0    | 0    | 0    | 50H       | 20ns                 |
| 30       | Minimum active to precharge time (tRAS)<br>-6B                      | 0    | 0    | 1    | 0    | 1    | 0    | 1    | 0    | 2AH       | 42ns                 |
|          | -7A, -7B                                                            | 0    | 0    | 1    | 0    | 1    | 1    | 0    | 1    | 2DH       | 45ns                 |
| 31       | Module rank density                                                 | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 1    | 01H       | 1 rank<br>1GB        |
| 32       | Address and command setup time before clock (tIS)<br>-6B            | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 75H       | 0.75ns <sup>*3</sup> |
|          | -7A, -7B                                                            | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 90H       | 0.9ns <sup>*3</sup>  |
| 33       | Address and command hold time after clock (tIH)<br>-6B              | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 75H       | 0.75ns <sup>*3</sup> |
|          | -7A, -7B                                                            | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 90H       | 0.9ns <sup>*3</sup>  |
| 34       | Data input setup time before clock (tDS)<br>-6B                     | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 1    | 45H       | 0.45ns <sup>*3</sup> |
|          | -7A, -7B                                                            | 0    | 1    | 0    | 1    | 0    | 0    | 0    | 0    | 50H       | 0.5ns <sup>*3</sup>  |
| 35       | Data input hold time after clock (tDH)<br>-6B                       | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 1    | 45H       | 0.45ns <sup>*3</sup> |
|          | -7A, -7B                                                            | 0    | 1    | 0    | 1    | 0    | 0    | 0    | 0    | 50H       | 0.5ns <sup>*3</sup>  |
| 36 to 40 | Superset information                                                | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 00H       | Future use           |
| 41       | Active command period (tRC)<br>-6B                                  | 0    | 0    | 1    | 1    | 1    | 1    | 0    | 0    | 3CH       | 60ns <sup>*3</sup>   |
|          | -7A, -7B                                                            | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 1    | 41H       | 65ns <sup>*3</sup>   |
| 42       | Auto refresh to active/<br>Auto refresh command cycle (tRFC)<br>-6B | 0    | 1    | 0    | 0    | 1    | 0    | 0    | 0    | 48H       | 72ns <sup>*3</sup>   |
|          | -7A, -7B                                                            | 0    | 1    | 0    | 0    | 1    | 0    | 1    | 1    | 4BH       | 75ns <sup>*3</sup>   |
| 43       | SDRAM tCK cycle max. (tCK max.)                                     | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 0    | 30H       | 12ns <sup>*3</sup>   |
| 44       | Dout to DQS skew<br>-6B                                             | 0    | 0    | 1    | 0    | 1    | 1    | 0    | 1    | 2DH       | 450ps <sup>*3</sup>  |
|          | -7A, -7B                                                            | 0    | 0    | 1    | 1    | 0    | 0    | 1    | 0    | 32H       | 500ps <sup>*3</sup>  |
| 45       | Data hold skew (tQHS)<br>-6B                                        | 0    | 1    | 0    | 1    | 0    | 1    | 0    | 1    | 55H       | 550ps <sup>*3</sup>  |
|          | -7A, -7B                                                            | 0    | 1    | 1    | 1    | 0    | 1    | 0    | 1    | 75H       | 750ps <sup>*3</sup>  |
| 46 to 61 | Superset information                                                | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 00H       | Future use           |
| 62       | SPD revision                                                        | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 00H       | Initial              |
| 63       | Checksum for bytes 0 to 62<br>-6B                                   | 1    | 1    | 0    | 1    | 0    | 0    | 1    | 1    | D3H       | 211                  |
|          | -7A                                                                 | 1    | 0    | 0    | 0    | 1    | 0    | 1    | 0    | 8AH       | 138                  |
|          | -7B                                                                 | 1    | 0    | 1    | 1    | 0    | 1    | 0    | 1    | B5H       | 181                  |
| 64       | Manufacturer's JEDEC ID code                                        | 0    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 7FH       |                      |
| 65       | Manufacturer's JEDEC ID code                                        | 0    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 7FH       |                      |
| 66       | Manufacturer's JEDEC ID code                                        | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 0    | FEH       | Elpida Memory        |

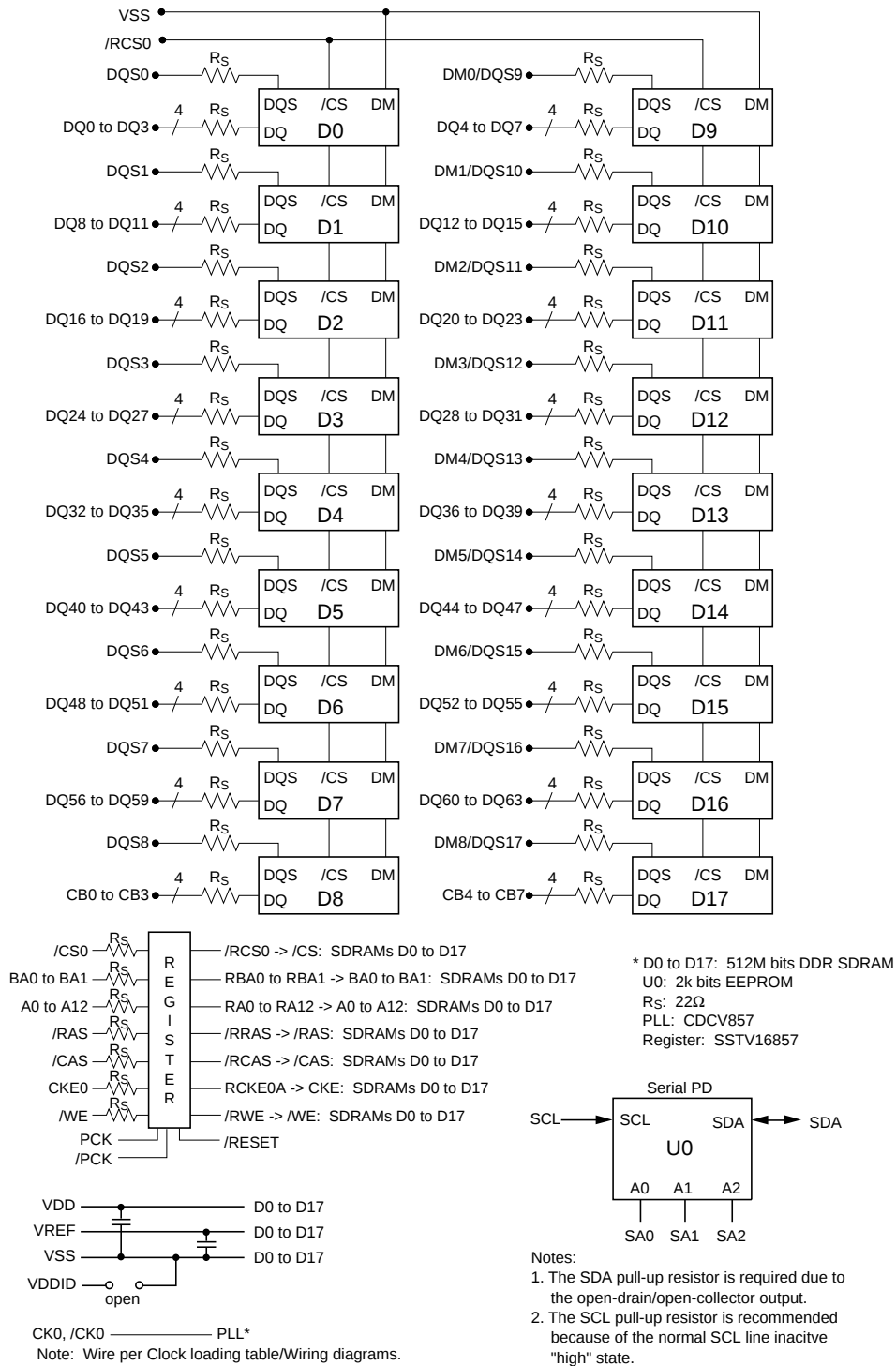
| Byte No.  | Function described           | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Hex value | Comments          |
|-----------|------------------------------|------|------|------|------|------|------|------|------|-----------|-------------------|
| 67 to 71  | Manufacturer's JEDEC ID code | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 00H       |                   |
| 72        | Manufacturing location       | ×    | ×    | ×    | ×    | ×    | ×    | ×    | ×    | ×         | (ASCII-8bit code) |
| 73        | Module part number           | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 1    | 45H       | E                 |
| 74        | Module part number           | 0    | 1    | 0    | 0    | 0    | 0    | 1    | 0    | 42H       | B                 |
| 75        | Module part number           | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 0    | 44H       | D                 |
| 76        | Module part number           | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 1    | 31H       | 1                 |
| 77        | Module part number           | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 0    | 30H       | 0                 |
| 78        | Module part number           | 0    | 1    | 0    | 1    | 0    | 0    | 1    | 0    | 52H       | R                 |
| 79        | Module part number           | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 0    | 44H       | D                 |
| 80        | Module part number           | 0    | 0    | 1    | 1    | 0    | 1    | 0    | 0    | 34H       | 4                 |
| 81        | Module part number           | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 1    | 41H       | A                 |
| 82        | Module part number           | 0    | 1    | 0    | 0    | 0    | 1    | 0    | 0    | 44H       | D                 |
| 83        | Module part number           | 0    | 1    | 0    | 0    | 0    | 1    | 1    | 0    | 46H       | F                 |
| 84        | Module part number           | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 1    | 41H       | A                 |
| 85        | Module part number           | 0    | 0    | 1    | 0    | 1    | 1    | 0    | 1    | 2DH       | —                 |
| 86        | Module part number<br>-6B    | 0    | 0    | 1    | 1    | 0    | 1    | 1    | 0    | 36H       | 6                 |
|           | -7A, -7B                     | 0    | 0    | 1    | 1    | 0    | 1    | 1    | 1    | 37H       | 7                 |
| 87        | Module part number<br>-7A    | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 1    | 41H       | A                 |
|           | -6B, -7B                     | 0    | 1    | 0    | 0    | 0    | 0    | 1    | 0    | 42H       | B                 |
| 88 to 90  | Module part number           | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 20H       | (Space)           |
| 91        | Revision code                | 0    | 0    | 1    | 1    | 0    | 0    | 0    | 0    | 30H       | Initial           |
| 92        | Revision code                | 0    | 0    | 1    | 0    | 0    | 0    | 0    | 0    | 20H       | (Space)           |
| 93        | Manufacturing date           | ×    | ×    | ×    | ×    | ×    | ×    | ×    | ×    | ×         | Year code (HEX)   |
| 94        | Manufacturing date           | ×    | ×    | ×    | ×    | ×    | ×    | ×    | ×    | ×         | Week code (HEX)   |
| 95 to 98  | Module serial number         | *2   |      |      |      |      |      |      |      |           |                   |
| 99 to 127 | Manufacturer specific data   |      |      |      |      |      |      |      |      |           |                   |

Notes: 1. All serial PD data are not protected. 0: Serial data, "driven Low", 1: Serial data, "driven High".

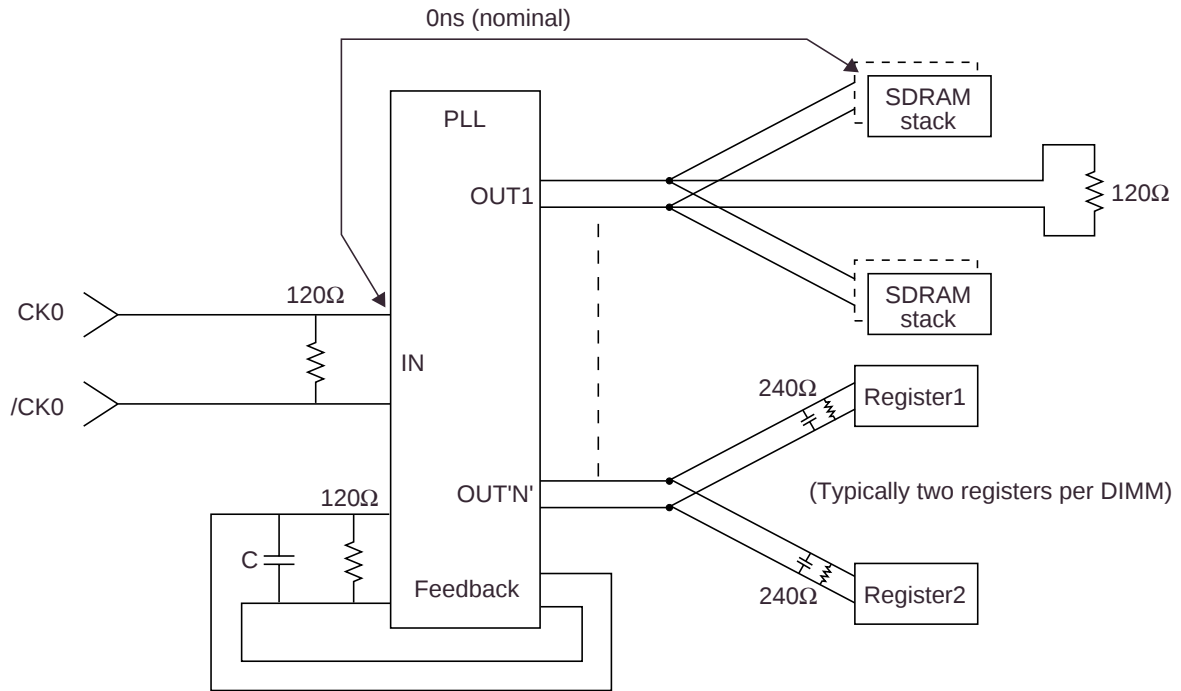
2. Bytes 95 through 98 are assembly serial number.

3. These specifications are defined based on component specification, not module.

## Block Diagram



## Differential Clock Net Wiring (CK0, /CK0)



- Notes:
1. The clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0 ns (nominal).
  2. Input, output and feedback clock lines are terminated from line to line as shown, and not from line to ground.
  3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
  4. Termination resistors for feedback path clocks are located after the pins of the PLL.

## Electrical Specifications

- All voltages are referenced to VSS (GND).

### Absolute Maximum Ratings

| Parameter                          | Symbol | Value        | Unit | Note |
|------------------------------------|--------|--------------|------|------|
| Voltage on any pin relative to VSS | VT     | −1.0 to +3.6 | V    |      |
| Supply voltage relative to VSS     | VDD    | −1.0 to +3.6 | V    |      |
| Short circuit output current       | IOS    | 50           | mA   |      |
| Power dissipation                  | PD     | 18           | W    |      |
| Operating ambient temperature      | TA     | 0 to +70     | °C   | 1    |
| Storage temperature                | Tstg   | −55 to +125  | °C   |      |

Note:1. DDR SDRAM component specification

### Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### DC Operating Conditions (TA = 0 to +70°C) (DDR SDRAM Component Specification)

| Parameter                                                 | Symbol   | Min                      | Typ                | Max                      | Unit | Notes |
|-----------------------------------------------------------|----------|--------------------------|--------------------|--------------------------|------|-------|
| Supply voltage                                            | VDD,VDDQ | 2.3                      | 2.5                | 2.7                      | V    | 1     |
|                                                           | VSS      | 0                        | 0                  | 0                        | V    |       |
| Input reference voltage                                   | VREF     | $0.49 \times VDDQ$       | $0.50 \times VDDQ$ | $0.51 \times VDDQ$       | V    |       |
| Termination voltage                                       | VTT      | $VREF - 0.04$            | VREF               | $VREF + 0.04$            | V    |       |
| Input high voltage                                        | VIH (DC) | $VREF + 0.15$            | —                  | $VDDQ + 0.3$             | V    | 2     |
| Input low voltage                                         | VIL (DC) | −0.3                     | —                  | $VREF - 0.15$            | V    | 3     |
| Input voltage level, CK and /CK inputs                    | VIN (DC) | −0.3                     | —                  | $VDDQ + 0.3$             | V    | 4     |
| Input differential cross point voltage, CK and /CK inputs | VIX (DC) | $0.5 \times VDDQ - 0.2V$ | $0.5 \times VDDQ$  | $0.5 \times VDDQ + 0.2V$ | V    |       |
| Input differential voltage, CK and /CK inputs             | VID (DC) | 0.36                     | —                  | $VDDQ + 0.6$             | V    | 5, 6  |

Notes: 1. VDDQ must be lower than or equal to VDD.

2. VIH is allowed to exceed VDD up to 3.6V for the period shorter than or equal to 5ns.

3. VIL is allowed to outreach below VSS down to −1.0V for the period shorter than or equal to 5ns.

4. VIN (DC) specifies the allowable DC execution of each differential input.

5. VID (DC) specifies the input differential voltage required for switching.

6. VIH (CK) min assumed over  $VREF + 0.18V$ , VIL (CK) max assumed under  $VREF - 0.18V$  if measurement.

**DC Characteristics 1 (TA = 0 to +70°C, VDD = 2.5V ± 0.2V, VSS = 0V)**

| Parameter                                 | Symbol | Grade           | max.         | Unit | Test condition                                      | Notes      |
|-------------------------------------------|--------|-----------------|--------------|------|-----------------------------------------------------|------------|
| Operating current (ACTV-PRE)              | IDD0   | -6B<br>-7A, -7B | 3165<br>2830 | mA   | CKE ≥ VIH,<br>tRC = tRC (min.)                      | 1, 2, 9    |
| Operating current (ACTV-READ-PRE)         | IDD1   | -6B<br>-7A, -7B | 3885<br>3460 | mA   | CKE ≥ VIH, BL = 4,<br>CL = 3.5,<br>tRC = tRC (min.) | 1, 2, 5    |
| Idle power down standby current           | IDD2P  | -6B<br>-7A, -7B | 520<br>454   | mA   | CKE ≤ VIL                                           | 4          |
| Floating idle standby current             | IDD2F  | -6B<br>-7A, -7B | 1005<br>850  | mA   | CKE ≥ VIH, /CS ≥ VIH,<br>DQ, DQS, DM = VREF         | 4, 5       |
| Quiet idle standby current                | IDD2Q  | -6B<br>-7A, -7B | 825<br>760   | mA   | CKE ≥ VIH, /CS ≥ VIH,<br>DQ, DQS, DM = VREF         | 4, 10      |
| Active power down standby current         | IDD3P  | -6B<br>-7A, -7B | 825<br>760   | mA   | CKE ≤ VIL                                           | 3          |
| Active standby current                    | IDD3N  | -6B<br>-7A, -7B | 1635<br>1390 | mA   | CKE ≥ VIH, /CS ≥ VIH<br>tRAS = tRAS (max.)          | 3, 5, 6    |
| Operating current (Burst read operation)  | IDD4R  | -6B<br>-7A, -7B | 4605<br>4000 | mA   | CKE ≥ VIH, BL = 2,<br>CL = 3.5                      | 1, 2, 5, 6 |
| Operating current (Burst write operation) | IDD4W  | -6B<br>-7A, -7B | 4605<br>4000 | mA   | CKE ≥ VIH, BL = 2,<br>CL = 3.5                      | 1, 2, 5, 6 |
| Auto refresh current                      | IDD5   | -6B<br>-7A, -7B | 6225<br>5800 | mA   | tRFC = tRFC (min.),<br>Input ≤ VIL or ≥ VIH         |            |
| Self refresh current                      | IDD6   | -6B<br>-7A, -7B | 538<br>472   | mA   | Input ≥ VDD - 0.2 V<br>Input ≤ 0.2 V                |            |
| Operating current (4 banks interleaving)  | IDD7A  | -6B<br>-7A, -7B | 9285<br>7780 | mA   | BL = 4                                              | 1, 5, 6, 7 |

Notes. 1. These IDD data are measured under condition that DQ pins are not connected.

2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one cycle.
6. DQ, DM, DQS transition twice per one cycle.
7. 4 banks active. Only one bank is running at tRC = tRC (min.)
8. The IDD data on this table are measured with regard to tCK = tCK (min.) in general.
9. Command/Address transition once every two clock cycles.
10. Command/Address stable at ≥ VIH or ≤ VIL.

**DC Characteristics 2 (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS = 0V)****(DDR SDRAM Component Specification)**

| Parameter              | Symbol | min.  | max. | Unit | Test condition    | Notes |
|------------------------|--------|-------|------|------|-------------------|-------|
| Input leakage current  | ILI    | -2    | 2    | μA   | VDD ≥ VIN ≥ VSS   |       |
| Output leakage current | ILO    | -5    | 5    | μA   | VDDQ ≥ VOUT ≥ VSS |       |
| Output high current    | IOH    | -15.2 | —    | mA   | VOUT = 1.95V      |       |
| Output low current     | IOL    | 15.2  | —    | mA   | VOUT = 0.35V      |       |

**Pin Capacitance (TA = +25°C, VDD = 2.5V ± 0.2V)**

| Parameter                             | Symbol | Pins                               | max. | Unit | Notes   |
|---------------------------------------|--------|------------------------------------|------|------|---------|
| Input capacitance                     | CI1    | Address, /RAS, /CAS, /WE, /CS, CKE | 12   | pF   | 1, 3    |
| Input capacitance                     | CI2    | CK, /CK                            | 20   | pF   | 1, 3    |
| Data and DQS input/output capacitance | CO     | DQ, DQS, CB                        | 15   | pF   | 1, 2, 3 |

Notes: 1. These parameters are measured on conditions: f = 100MHz, VOUT = VDDQ/2, ΔVOUT = 0.2V.

2. Dout circuits are disabled.

3. This parameter is sampled and not 100% tested.

**AC Characteristics (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS = 0V)****(DDR SDRAM Component Specification)**

| Parameter                                      | Symbol | -6B            |      | -7A            |      | -7B            |      | Unit | Notes |
|------------------------------------------------|--------|----------------|------|----------------|------|----------------|------|------|-------|
|                                                |        | min.           | max  | min.           | max  | min.           | max  |      |       |
| Clock cycle time (CL = 2)                      | tCK    | 7.5            | 12   | 7.5            | 12   | 10             | 12   | ns   | 10    |
| (CL = 2.5)                                     | tCK    | 6              | 12   | 7.5            | 12   | 7.5            | 12   | ns   |       |
| CK high-level width                            | tCH    | 0.45           | 0.55 | 0.45           | 0.55 | 0.45           | 0.55 | tCK  |       |
| CK low-level width                             | tCL    | 0.45           | 0.55 | 0.45           | 0.55 | 0.45           | 0.55 | tCK  |       |
| CK half period                                 | tHP    | min (tCH, tCL) | —    | min (tCH, tCL) | —    | min (tCH, tCL) | —    | tCK  |       |
| DQ output access time from CK, /CK             | tAC    | −0.7           | 0.7  | −0.75          | 0.75 | −0.75          | 0.75 | ns   | 2, 11 |
| DQS output access time from CK, /CK            | tDQSCK | −0.6           | 0.6  | −0.75          | 0.75 | −0.75          | 0.75 | ns   | 2, 11 |
| DQS to DQ skew                                 | tDQSQ  | —              | 0.45 | —              | 0.5  | —              | 0.5  | ns   | 3     |
| DQ/DQS output hold time from DQS               | tQH    | tHP − tQHS     | —    | tHP − tQHS     | —    | tHP − tQHS     | —    | ns   |       |
| Data hold skew factor                          | tQHS   | —              | 0.55 | —              | 0.75 | —              | 0.75 | ns   |       |
| Data-out high-impedance time from CK, /CK      | tHZ    | −0.7           | 0.7  | −0.75          | 0.75 | −0.75          | 0.75 | ns   | 5, 11 |
| Data-out low-impedance time from CK, /CK       | tLZ    | −0.7           | 0.7  | −0.75          | 0.75 | −0.75          | 0.75 | ns   | 6, 11 |
| Read preamble                                  | tRPRE  | 0.9            | 1.1  | 0.9            | 1.1  | 0.9            | 1.1  | tCK  |       |
| Read postamble                                 | tRPST  | 0.4            | 0.6  | 0.4            | 0.6  | 0.4            | 0.6  | tCK  |       |
| DQ and DM input setup time                     | tDS    | 0.45           | —    | 0.5            | —    | 0.5            | —    | ns   | 8     |
| DQ and DM input hold time                      | tDH    | 0.45           | —    | 0.5            | —    | 0.5            | —    | ns   | 8     |
| DQ and DM input pulse width                    | tDIPW  | 1.75           | —    | 1.75           | —    | 1.75           | —    | ns   | 7     |
| Write preamble setup time                      | tWPRES | 0              | —    | 0              | —    | 0              | —    | ns   |       |
| Write preamble                                 | tWPRE  | 0.25           | —    | 0.25           | —    | 0.25           | —    | tCK  |       |
| Write postamble                                | tWPST  | 0.4            | 0.6  | 0.4            | 0.6  | 0.4            | 0.6  | tCK  | 9     |
| Write command to first DQS latching transition | tDQSS  | 0.75           | 1.25 | 0.75           | 1.25 | 0.75           | 1.25 | tCK  |       |
| DQS falling edge to CK setup time              | tDSS   | 0.2            | —    | 0.2            | —    | 0.2            | —    | tCK  |       |
| DQS falling edge hold time from CK             | tDSH   | 0.2            | —    | 0.2            | —    | 0.2            | —    | tCK  |       |
| DQS input high pulse width                     | tDQSH  | 0.35           | —    | 0.35           | —    | 0.35           | —    | tCK  |       |
| DQS input low pulse width                      | tDQSL  | 0.35           | —    | 0.35           | —    | 0.35           | —    | tCK  |       |
| Address and control input setup time           | tIS    | 0.75           | —    | 0.9            | —    | 0.9            | —    | ns   | 8     |

| Parameter                                          | Symbol | -6B                 |        | -7A                 |        | -7B                 |        | Unit | Notes |
|----------------------------------------------------|--------|---------------------|--------|---------------------|--------|---------------------|--------|------|-------|
|                                                    |        | min.                | max    | min.                | max    | min.                | max    |      |       |
| Address and control input hold time                | tIH    | 0.75                | —      | 0.9                 | —      | 0.9                 | —      | ns   | 8     |
| Address and control input pulse width              | tIPW   | 2.2                 | —      | 2.2                 | —      | 2.2                 | —      | ns   | 7     |
| Mode register set command cycle time               | tMRD   | 2                   | —      | 2                   | —      | 2                   | —      | tCK  |       |
| Active to Precharge command period                 | tRAS   | 42                  | 120000 | 45                  | 120000 | 45                  | 120000 | ns   |       |
| Active to Active/Auto refresh command period       | tRC    | 60                  | —      | 65                  | —      | 65                  | —      | ns   |       |
| Auto refresh to Active/Auto refresh command period | tRFC   | 72                  | —      | 75                  | —      | 75                  | —      | ns   |       |
| Active to Read/Write delay                         | tRCD   | 18                  | —      | 20                  | —      | 20                  | —      | ns   |       |
| Precharge to active command period                 | tRP    | 18                  | —      | 20                  | —      | 20                  | —      | ns   |       |
| Active to auto precharge delay                     | tRAP   | tRCD min.           | —      | tRCD min.           | —      | tRCD min.           | —      | ns   |       |
| Active to active command period                    | tRRD   | 12                  | —      | 15                  | —      | 15                  | —      | ns   |       |
| Write recovery time                                | tWR    | 15                  | —      | 15                  | —      | 15                  | —      | ns   |       |
| Auto precharge write recovery and precharge time   | tDAL   | (tWR/tCK)+(tRP/tCK) | —      | (tWR/tCK)+(tRP/tCK) | —      | (tWR/tCK)+(tRP/tCK) | —      | tCK  | 13    |
| Internal write to Read command delay               | tWTR   | 1                   | —      | 1                   | —      | 1                   | —      | tCK  |       |
| Average periodic refresh interval                  | tREF   | —                   | 7.8    | —                   | 7.8    | —                   | 7.8    | μs   |       |

Notes: 1. All the AC parameters listed in this data sheet is component specifications. For AC testing conditions, refer to the corresponding component data sheet.

2. This parameter defines the signal transition delay from the cross point of CK and /CK. The signal transition is defined to occur when the signal level crossing VTT.
3. The timing reference level is VTT.
4. Output valid window is defined to be the period between two successive transition of data out or DQS (read) signals. The signal transition is defined to occur when the signal level crossing VTT.
5. tHZ is defined as DOUT transition delay from Low-Z to High-Z at the end of read burst operation. The timing reference is cross point of CK and /CK. This parameter is not referred to a specific DOUT voltage level, but specify when the device output stops driving.
6. tLZ is defined as DOUT transition delay from High-Z to Low-Z at the beginning of read operation. This parameter is not referred to a specific DOUT voltage level, but specify when the device output begins driving.
7. Input valid windows is defined to be the period between two successive transition of data input or DQS (write) signals. The signal transition is defined to occur when the signal level crossing VREF.
8. The timing reference level is VREF.
9. The transition from Low-Z to High-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
10. tCK (max.) is determined by the lock range of the DLL. Beyond this lock range, the DLL operation is not assured.
11. tCK = tCK (min.) when these parameters are measured. Otherwise, absolute minimum values of these values are 10% of tCK.
12. VDD is assumed to be 2.5V ± 0.2V. VDD power supply variation per cycle expected to be less than 0.4V/400 cycle.
13. tDAL = (tWR/tCK)+(tRP/tCK)

For each of the terms above, if not already an integer, round to the next highest integer.

Example: For -7A Speed at CL = 2.5, tCK = 7.5ns, tWR = 15ns and tRP = 20ns,

$$tDAL = (15\text{ns}/7.5\text{ns}) + (20\text{ns}/7.5\text{ns}) = (2) + (3)$$

$$tDAL = 5 \text{ clocks}$$

## Timing Parameter Measured in Clock Cycle for Registered DIMM

|                                                                   |        | Number of clock cycle |      |          |      |      |
|-------------------------------------------------------------------|--------|-----------------------|------|----------|------|------|
| tCK                                                               |        | 6ns                   |      | 7.5ns    |      |      |
| Parameter                                                         | Symbol | min.                  | max. | min.     | max. | Unit |
| Write to pre-charge command delay (same bank)                     | tWPD   | 4 + BL/2              | —    | 3 + BL/2 | —    | tCK  |
| Read to pre-charge command delay (same bank)                      | tRPD   | BL/2                  | —    | BL/2     | —    | tCK  |
| Write to read command delay (to input all data)                   | tWRD   | 2 + BL/2              | —    | 2 + BL/2 | —    | tCK  |
| Burst stop command to write command delay (CL = 3)                | tBSTW  | —                     | —    | 2        | —    | tCK  |
| (CL = 3.5)                                                        | tBSTW  | 3                     | —    | 3        | —    | tCK  |
| Burst stop command to DQ High-Z (CL = 3)                          | tBSTZ  | —                     | —    | 3        | 3    | tCK  |
| (CL = 3.5)                                                        | tBSTZ  | 3.5                   | 3.5  | 3.5      | 3.5  | tCK  |
| Read command to write command delay (to output all data) (CL = 3) | tRWD   | —                     | —    | 2 + BL/2 | —    | tCK  |
| (CL = 3.5)                                                        | tRWD   | 3 + BL/2              | —    | 3 + BL/2 | —    | tCK  |
| Pre-charge command to High-Z (CL = 3)                             | tHZP   | —                     | —    | 3        | 3    | tCK  |
| (CL = 3.5)                                                        | tHZP   | 3.5                   | 3.5  | 3.5      | 3.5  | tCK  |
| Write command to data in latency                                  | tWCD   | 2                     | —    | 2        | 2    | tCK  |
| Write recovery                                                    | tWR    | 2                     | —    | 1        | —    | tCK  |
| Register set command to active or register set command            | tMRD   | 2                     | —    | 2        | —    | tCK  |
| Self refresh exit to non-read command                             | tSNR   | 12                    | —    | 10       | —    | tCK  |
| Self refresh exit to read command                                 | tSRD   | 200                   | —    | 200      | —    | tCK  |
| Power down entry                                                  | tPDEN  | 1                     | 1    | 1        | 1    | tCK  |
| Power down exit to command input                                  | tPDEX  | 1                     | —    | 1        | —    | tCK  |

## Pin Functions

### CK, /CK (input pin)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CK and the /CK.

### /CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

### /RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

### A0 to A12 (input pins)

Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY9, AY11, AY12) is loaded via the A0 to the A9, the A11 and the A12 at the cross point of the CK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

### A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = high when a precharge command is issued, all banks are precharged. If A10 = low when a precharge command is issued, only the bank that is selected by BA1, BA0 is precharged. If A10 = high when read or write command, auto-precharge function is enabled. While A10 = low, auto-precharge function is disabled.

### BA0, BA1 (input pin)

BA0, BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Bank Select Signal Table)

#### [Bank Select Signal Table]

|        | BA0 | BA1 |
|--------|-----|-----|
| Bank 0 | L   | L   |
| Bank 1 | H   | L   |
| Bank 2 | L   | H   |
| Bank 3 | H   | H   |

Remark: H: VIH. L: VIL.

### CKE (input pin)

CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven low and exited when it resumes to high.

The CKE level must be kept for 1 CK cycle at least, that is, if CKE changes at the cross point of the CK rising edge and the VREF level with proper setup time tIS, at the next CK rising edge CKE level must be kept with proper hold time tIH.

### DQ, CB (input and output pins)

Data are input to and output from these pins.

### DQS (input and output pin)

DQS provide the read data strobes (as output) and the write data strobes (as input).

**VDD (power supply pins)**

2.5V is applied. (VDD is for the internal circuit.)

**VDDSPD (power supply pin)**

2.5V is applied (For serial EEPROM).

**VSS (power supply pin)**

Ground is connected.

**/RESET (input pin)**

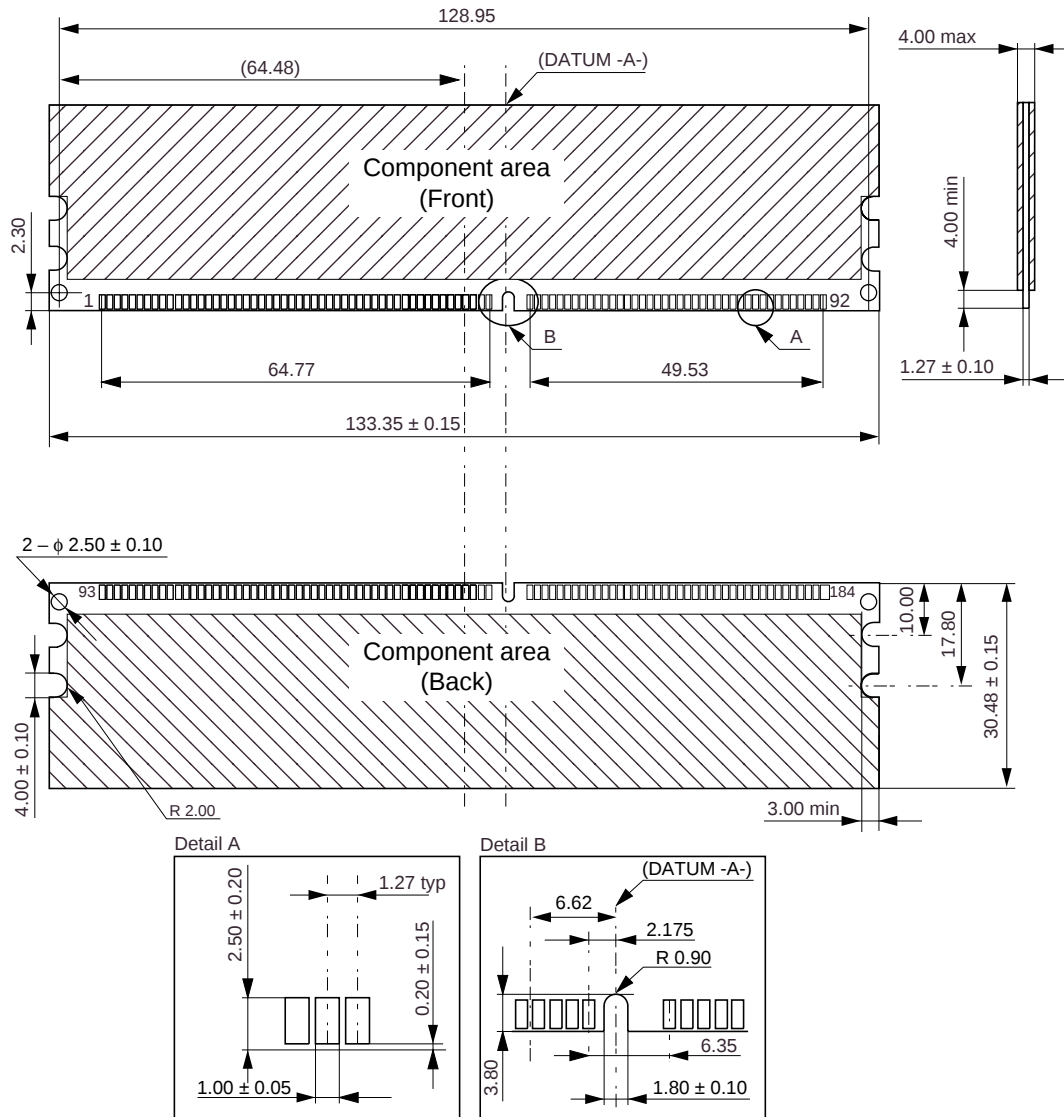
LVC MOS reset input. When /RESET is low, all registers are reset and all outputs are low.

**Detailed Operation Part and Timing Waveforms**

Refer to the EDD5104ADTA, EDD5108ADTA, EDD5116ADTA datasheet (E0384E). DM pins of component device fixed to VSS level on the module board. DIMM /CAS latency = component CL + 1 for registered type.

## Physical Outline

Unit: mm



ECA-TS2-0050-01

**CAUTION FOR HANDLING MEMORY MODULES**

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.

Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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**[Product usage]**

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This product is not designed to be resistant to electromagnetic waves or radiation. This product must be used in a non-condensing environment.

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If these products/technology are sold, leased, or transferred to a third party, or a third party is granted license to use these products, that third party must be made aware that they are responsible for compliance with the relevant laws and regulations.

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