MITSUBISHI LSIs

M5M4V16405CJ,TP-5,-6,-7, -5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMs with Hyper Page mode fuction, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16405CXX-5,-5S	50	13	25	13	90	330
M5M4V16405CXX-6,-6S	60	15	30	15	110	270
M5M4V16405CXX-7,-7S	70	20	35	20	130	225

XX=J,TP

- Standard 26pin SOJ, 26pin TSOP
- Single 3.3V±0.3V supply
- Low stand-by power dissipation
  - 1.80mW (Max) ------------------------- CMOS Input level
  - 0.72mW (Max) * ---------------------- CMOS Input level
- Low operating power dissipation
  - M5M4V16405Cxx-5,-5S -------------------- 400mW (Max)
  - M5M4V16405Cxx-6,-6S -------------------- 325mW (Max)
  - M5M4V16405Cxx-7,-7S -------------------- 270mW (Max)
- Self refresh capability *
  - Self refresh current ------------------------ 200 μA(Max)
- Hyper page mode (1024-column random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
  Early-write mode, $\overline{OE}$ and $\overline{W}$ to control output buffer impedance
- All inputs, outputs TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A_0 ~A_{11})

  *:Applicable to self refresh version (M5M4V16405CJ,TP-5S,-6S, -7S:option) only

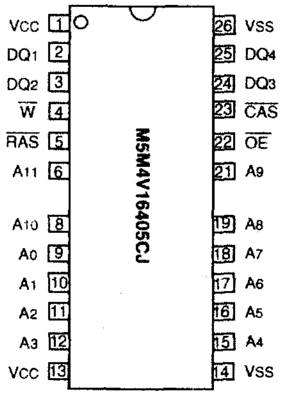
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

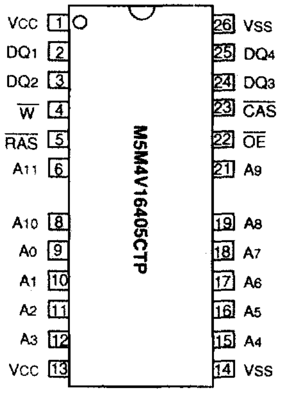
PIN DESCRIPTION

Pin name	Function
A_0~A_{11}	Address inputs
DQ_1~DQ_4	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

M5M4V16405CJ,TP-5,-5S : Under development

FUNCTION

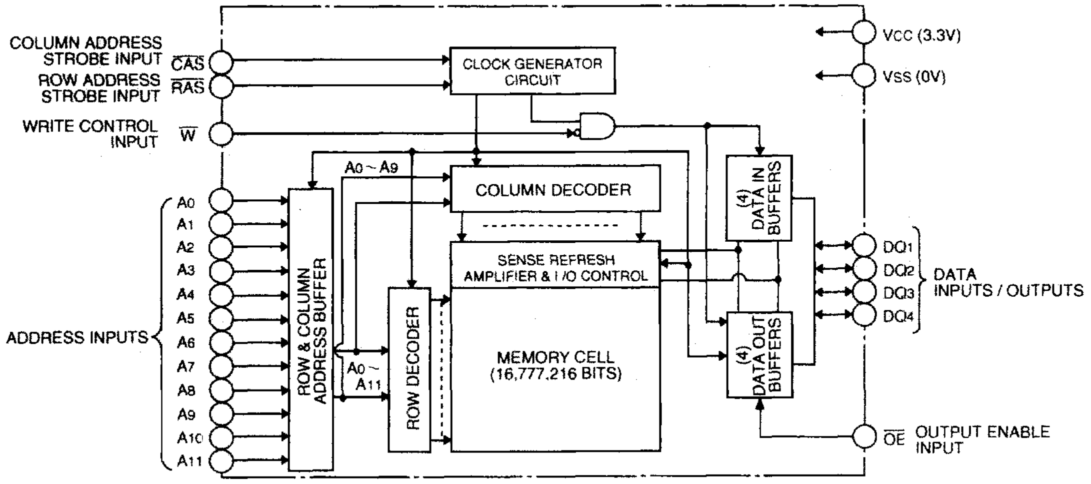
In addition to Hyper Page Mode, normal read, write and read-modify-write operations the M5M4V16405CJ,TP provides a number of other functions, e.g., $\overline{\text{RAS}}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{\text{RAS}}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	NAC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



M5M4V16405CJ,TP-5,-5S : Under development

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	-0.5~4.6	V
V_I	Input voltage		-0.5~4.6	V
V_O	Output voltage		-0.5~4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		-65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.0	3.3	3.6	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		V_{CC}+0.3	V
V_{IL}	Low-level input voltage, all inputs	-0.3**		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

** : V_{IL}(min.) is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to V_{SS}.)

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-2.0mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦V_{OUT}≦ 3.6V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦+3.6V, Other inputs pins=0V	-10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3,4,5)	M5M4V16405C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			110	mA
		M5M4V16405C-6,-6S				90	
		M5M4V16405C-7,-7S				75	
I_{CC2}	Supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧V_{CC} -0.2V, output open			0.5	
I_{CC3} (AV)	Average supply current from V_{CC}, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M4V16405C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			110	mA
		M5M4V16405C-6,-6S				90	
		M5M4V16405C-7,-7S				75	
$I_{CC4(AV)}$	Average supply current from V_{CC}, Hyper Page Mode (Note 3,4,5)	M5M4V16405C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{HPC}=min. output open			140	mA
		M5M4V16405C-6,-6S				115	
		M5M4V16405C-7,-7S				90	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M4V16405C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			110	mA
		M5M4V16405C-6,-6S				90	
		M5M4V16405C-7,-7S				75	

Note 2 : Current flowing into an IC is positive, out is negative.

3 : I_{CC1} (AV), I_{CC3} (AV) , I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4 : I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

5 : Under condition of column address being changed once or less while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}

CAPACITANCE (Ta=0~70℃, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I (A)}$	Input capacitance, address inputs	V_I=V_{SS} f=1MHz V_I=25mVrms			5	pF
$C_{I (CLK)}$	Input capacitance, clock inputs				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				8	pF

M5M4V16405CJ,TP-5,-5S : Under development

SWITCHING CHARACTERISTICS (Ta=0～70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{\text{CAS}}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{\text{RAS}}$	(Note 7,9)		50		60		70	ns
t_{AA}	Column address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{\text{CAS}}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{\text{OE}}$	(Note 7)		13		15		20	ns
t_{OHC}	Output hold time from $\overline{\text{CAS}}$ high	(Note 13)	5		5		5		ns
t_{OHR}	Output hold time from $\overline{\text{RAS}}$ high	(Note 13)	5		5		5		ns
t_{CLZ}	Output low impedance time from $\overline{\text{CAS}}$ low	(Note 7)	5		5		5		ns
t_{OEZ}	Output disable time after $\overline{\text{OE}}$ high	(Note 12)		13		15		20	ns
t_{WEZ}	Output disable time after $\overline{\text{WE}}$ high	(Note 12)		13		15		20	ns
t_{OFF}	Output disable time after $\overline{\text{CAS}}$ high	(Note 12,13)		13		15		20	ns
t_{REZ}	Output disable time after $\overline{\text{RAS}}$ high	(Note 12,13)		13		15		20	ns
t_{DOH}	Output hold time from $\overline{\text{CAS}}$ low		5		5		5		ns

Note 6 : An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization $\overline{\text{RAS}}$ cycles. The initialization cycles should be done either by $\overline{\text{RAS}}$-only refresh cycles or by $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles only.
Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$/$\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 64ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.
After the initialization cycles, $\overline{\text{RAS}}$ should be kept either higher than $V_{IH(min)}$ or lower than $V_{IL(max)}$ except $\overline{\text{RAS}}$ transition time.

7 : Measured with a load circuit equivalent to 100pF.
The reference levels for measuring of output signals are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8 : Assumes that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$ and $t_{CP} \geqq t_{CP(max)}$.

9 : Assumes that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leqq t_{CP(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq | \pm 10\mu A |$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0～70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter		Limits						Unit
			M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			64		64		64	ms
t_{RP}	$\overline{\text{RAS}}$ high pulse width		30		40		50		ns
t_{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low	(Note 16)	18	37	20	45	20	50	ns
t_{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low		5		5		5		ns
t_{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low		0		0		0		ns
t_{CPN}	$\overline{\text{CAS}}$ high pulse width		8		10		13		ns
t_{RAD}	Column address delay time from $\overline{\text{RAS}}$ low	(Note 17)	13	25	15	30	15	35	ns
t_{ASR}	Row address setup time before $\overline{\text{RAS}}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{\text{CAS}}$ low	(Note 18)	0	10	0	13	0	13	ns
t_{RAH}	Row address hold time after $\overline{\text{RAS}}$ low		8		10		10		ns
t_{CAH}	Column address hold time after $\overline{\text{CAS}}$ low		8		10		10		ns
t_{DZC}	Delay time, data to $\overline{\text{CAS}}$ low	(Note 19)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{\text{OE}}$ low	(Note 19)	0		0		0		ns
t_{RDD}	Delay time, $\overline{\text{RAS}}$ high to data	(Note 20)	13		15		20		ns
t_{CDD}	Delay time, $\overline{\text{CAS}}$ high to data	(Note 20)	13		15		20		ns
t_{ODD}	Delay time, $\overline{\text{OE}}$ high to data	(Note 20)	13		15		20		ns
t_T	Transition time	(Note 21)	1	50	1	50	1	50	ns

Note 14 : The timing requirements are assumed t_T=2ns.

15 : $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16 : $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.

17 : $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

18 : $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19 : Either t_{DZC} or t_{DZO} must be satisfied.

20 : Either t_{RDD} or t_{CDD} or t_{ODD} must be satisfied.

21 : t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

M5M4V16405CJ,TP-5,-5S : Under development

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		ns
t_{RAS}	$\overline{\text{RAS}}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{\text{CAS}}$ low pulse width	8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	40		48		55		ns
t_{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	13		15		20		ns
t_{RCS}	Read Setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{\text{CAS}}$ high (Note 22)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{\text{RAS}}$ high (Note 22)	0		0		0		ns
t_{RAL}	Column address to $\overline{\text{RAS}}$ hold time	25		30		35		ns
t_{CAL}	Column address to $\overline{\text{CAS}}$ hold time	13		18		23		ns
t_{ORH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low	13		15		20		ns
t_{OCH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low	13		15		20		ns

Note 22 : Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90		110		130		ns
t_{RAS}	$\overline{\text{RAS}}$ low pulse width	50	10000	60	10000	70	10000	ns
t_{CAS}	$\overline{\text{CAS}}$ low pulse width	8	10000	10	10000	13	10000	ns
t_{CSH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	40		48		55		ns
t_{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	13		15		20		ns
t_{WCS}	Write setup time before $\overline{\text{CAS}}$ low (Note 24)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{\text{CAS}}$ low	8		10		13		ns
t_{CWL}	$\overline{\text{CAS}}$ hold time after $\overline{\text{W}}$ low	8		10		13		ns
t_{RWL}	$\overline{\text{RAS}}$ hold time after $\overline{\text{W}}$ low	8		10		13		ns
t_{WP}	Write pulse width	8		10		13		ns
t_{DS}	Data setup time before $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note 23)	109		133		161		ns
t_{RAS}	$\overline{\text{RAS}}$ low pulse width	75	10000	89	10000	107	10000	ns
t_{CAS}	$\overline{\text{CAS}}$ low pulse width	38	10000	44	10000	57	10000	ns
t_{CSH}	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	70		82		99		ns
t_{RSH}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	38		44		57		ns
t_{RCS}	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (Note 24)	28		32		42		ns
t_{RWD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low (Note 24)	65		77		92		ns
t_{AWD}	Delay time, address to $\overline{\text{W}}$ low (Note 24)	40		47		57		ns
t_{OEH}	$\overline{\text{OE}}$ hold time after $\overline{\text{W}}$ low	13		15		20		ns

Note 23 : t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24 : t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes back to V_{IH}) is indeterminate.

M5M4V16405CJ,TP-5,-5S : Under development

Hyper page Mode Cycle
(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time (Note 26)	20		25		30		ns
t_{HPRWC}	Hyper Page Mode read write/read modify write cycle time	57		66		79		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read or write cycle (Note 27)	65	100000	77	100000	92	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 28)	8	13	10	16	13	16	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 24)	43		50		60		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until $\overline{CAS}$ access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	13		15		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	25		30		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	28		33		38		ns

Note 25 : All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.
26 : $t_{HPC(min)}$ is specified in the case of read-only and early write-only in Hyper Page Mode.
27 : $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.
28 : $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	17		17		22		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 29 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Hidden Refresh Cycle (Note 30)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{RSR}	Read setup time before $\overline{RAS}$ low	5		5		5		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Note 30 : Read, early write, delayed write, read write or read-modify-write cycle is applicable to hidden refresh cycle. In all cases t_{RSR} and t_{RHR} should be satisfied.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC8} (AV)	Average supply current from Vcc Slow-Refresh cycle (Note 6)	M5M4V16405C (S)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycling or $\overline{\text{RAS}}$ cycling & $\overline{\text{CAS}} \leqq 0.2\text{V}$ $\overline{\text{OE}}$ & $\overline{\text{WE}} \leqq 0.2\text{V}$ or $\overline{\text{OE}}$ & $\overline{\text{WE}} \geqq \text{Vcc}-0.2\text{V}$ $A_0 \sim A_{11} \leqq 0.2\text{V}$ or $A_0 \sim A_{11} \geqq \text{Vcc}-0.2\text{V}$ t_{REF}=128ms (4096cycles) output=OPEN $t_{RAS}=t_{RAS}\text{min.} \sim 1\mu\text{s}$			500	μA
I_{CC9} (AV)*	Average supply current from Vcc Self-Refresh cycle (Note 6)	M5M4V16405C (S)	$\overline{\text{RAS}}=\overline{\text{CAS}} \leqq 0.2\text{V}$ output = OPEN			200	μA

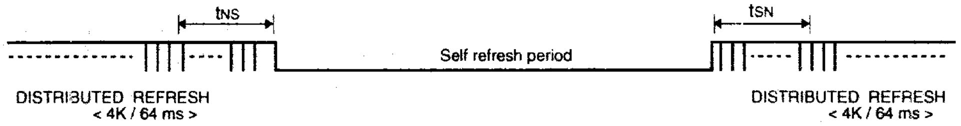
TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.3V±0.3V, Vss=0V, unless otherwise noted, see notes 14, 15)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5S		M5M4V16405C-6S		M5M4V16405C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{\text{RAS}}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{\text{RAS}}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{\text{RAS}}$ hold time	- 50		- 50		- 50		ns
t_{RSR}	Read setup time before $\overline{\text{RAS}}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{\text{RAS}}$ low	10		10		15		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

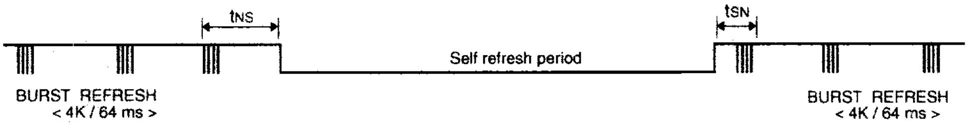
(1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 64\text{ms}$ and $t_{SN} \leqq 64\text{ms}$.



(2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS}+t_{SN} \leqq 64\text{ms}$.

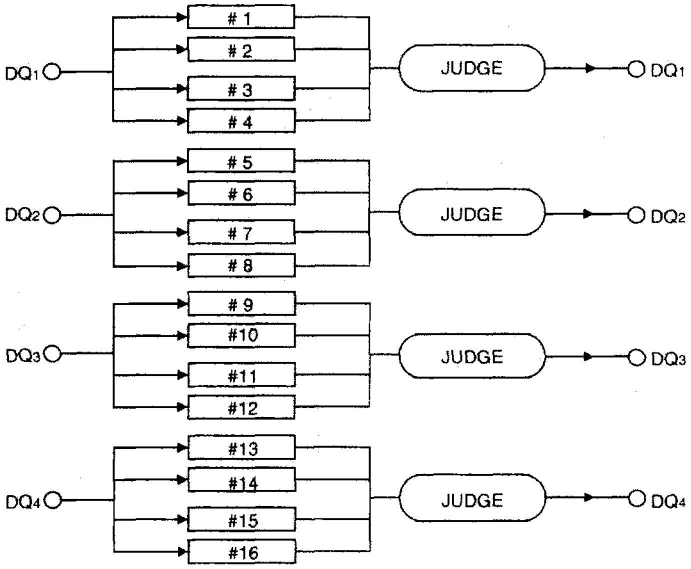


M5M4V16405CJ,TP-5,-5S : Under development

TEST Mode SET Cycle (Note 31)

Symbol	Parameter	Limits						Unit
		M5M4V16405C-5,-5S		M5M4V16405C-6,-6S		M5M4V16405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	$\overline{W}$ hold time after $\overline{RAS}$ low	10		10		15		ns

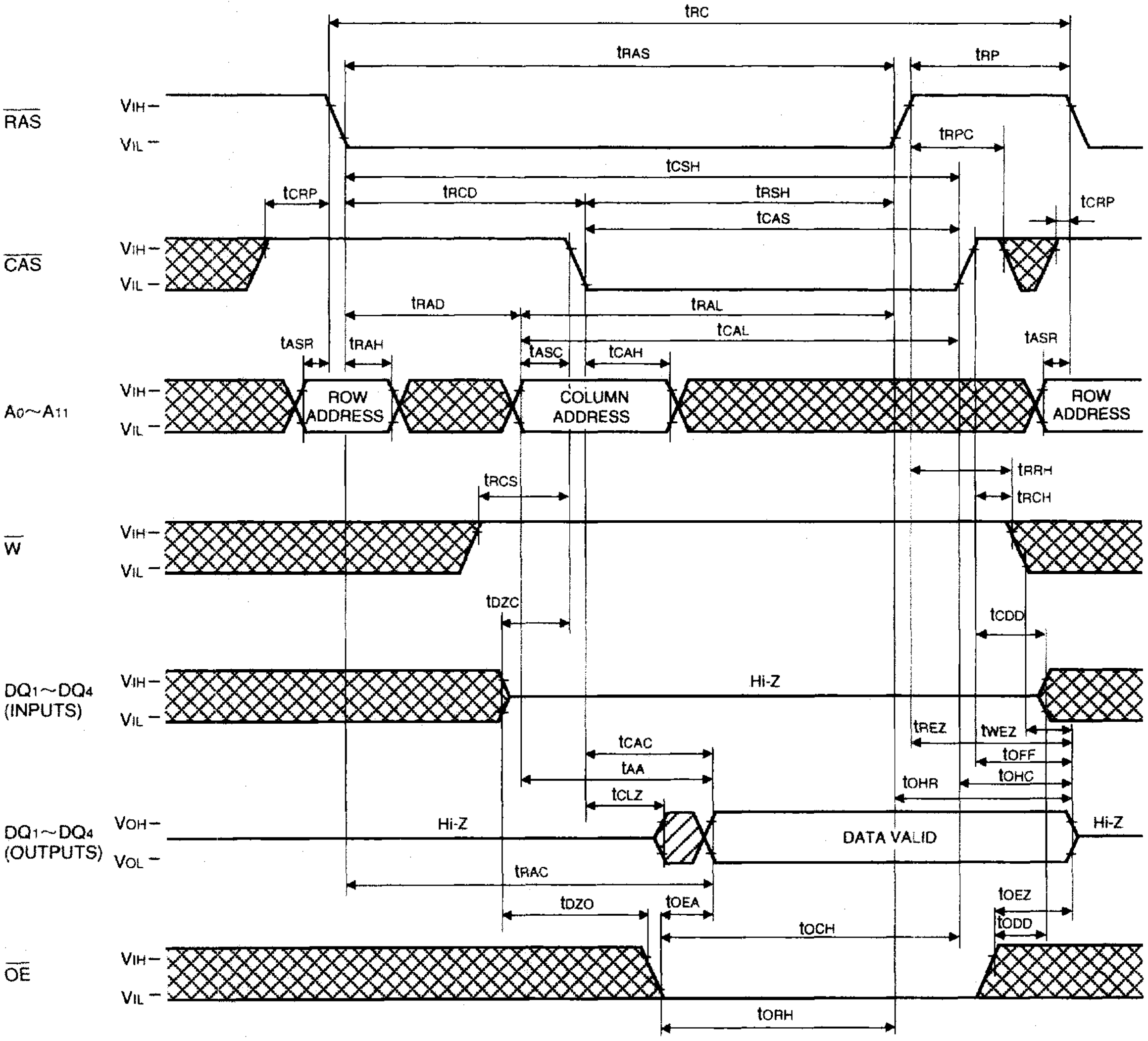
Note 31 : The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA_0 and CA_1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, only WCBR cycle can be used to perform refresh.



M5M4V16405CJ,TP-5,-5S : Under development

Timing Diagrams (Note 32)

Read Cycle

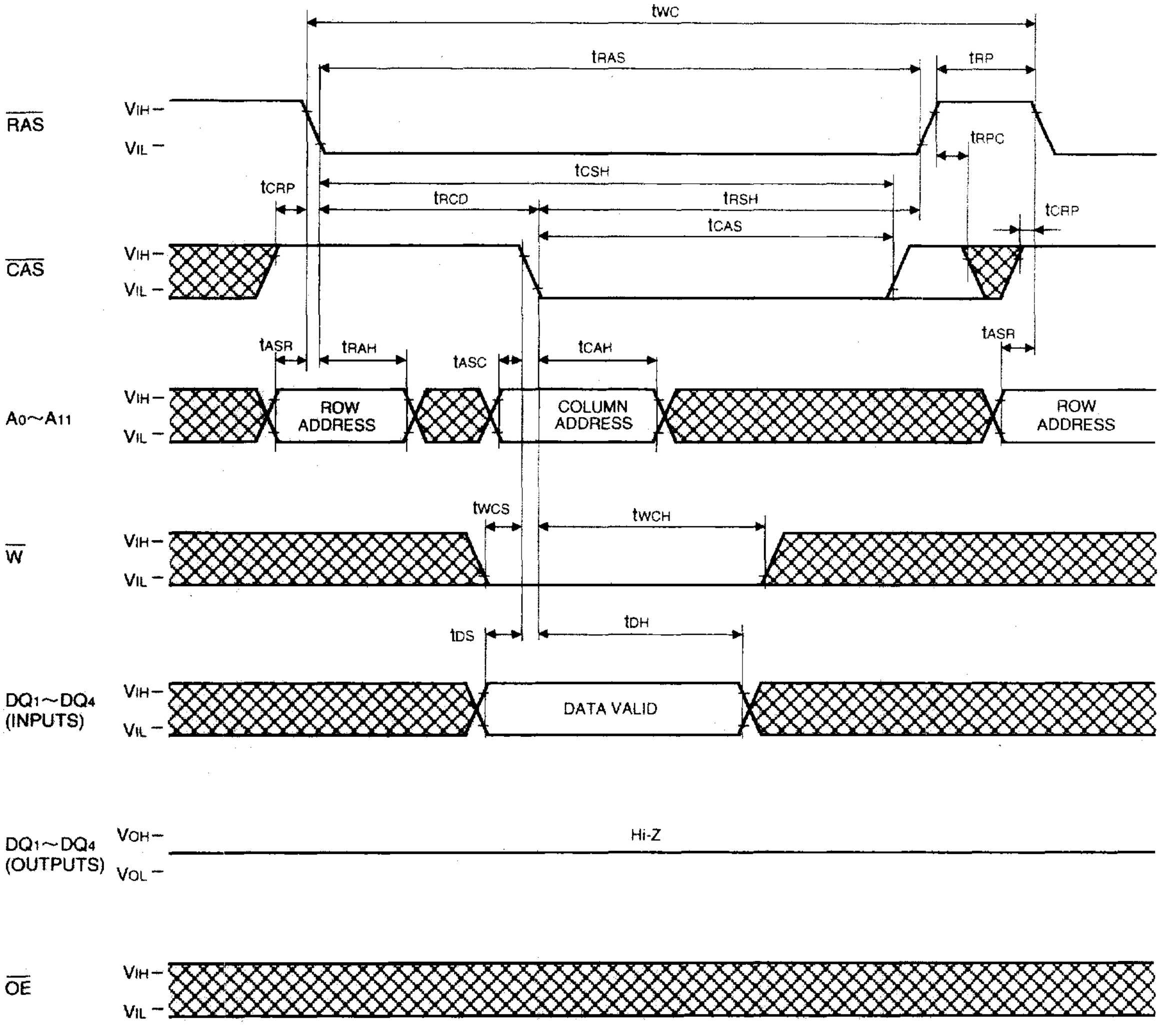


Note 32 ▩ Indicates the don't care input.
VIH(min)≦VIN≦VIH(max) or VIL(min)≦VIN≦VIL(max)

▨ Indicates the invalid output.

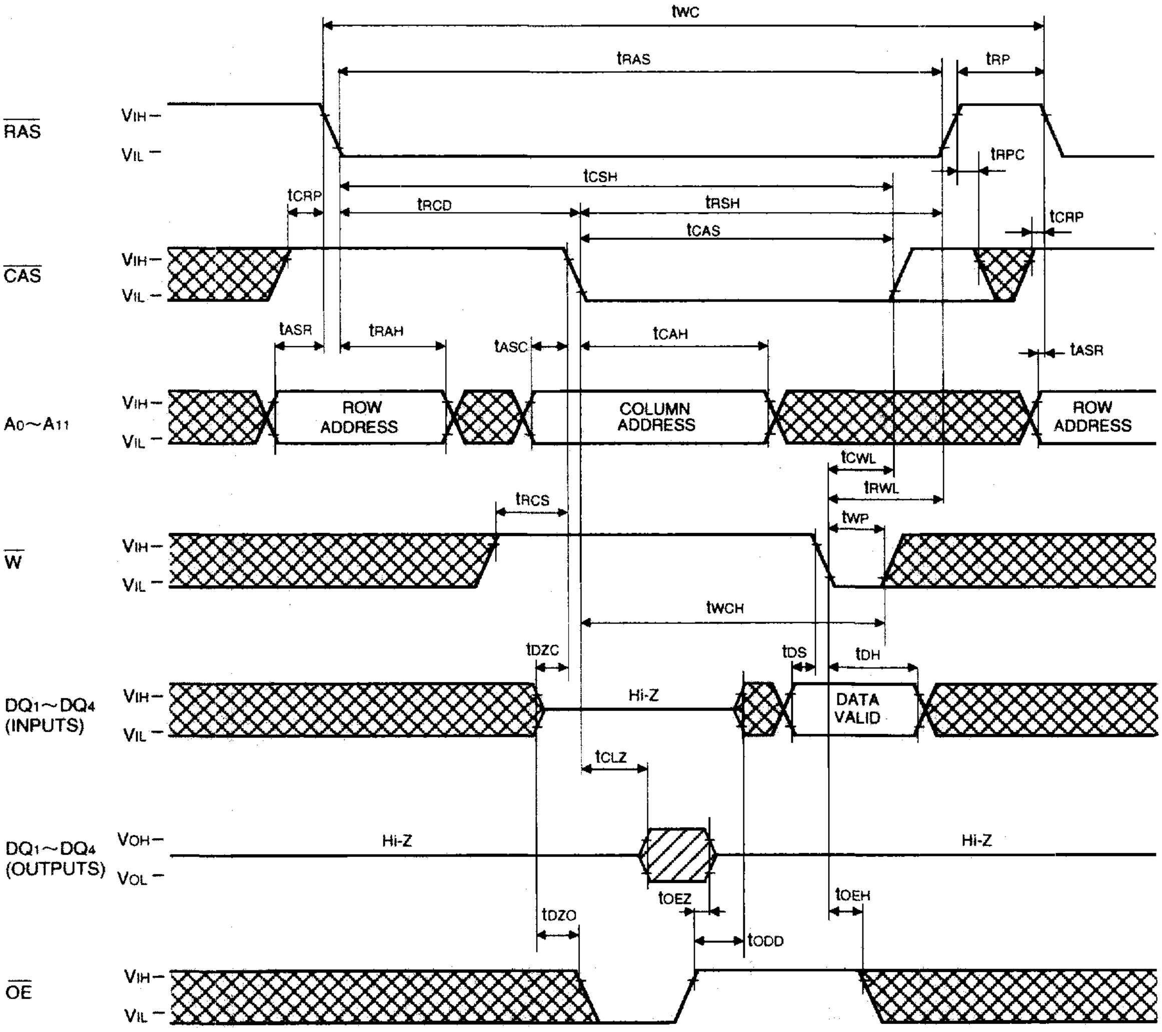
M5M4V16405CJ,TP-5,-5S : Under development

Early Write Cycle

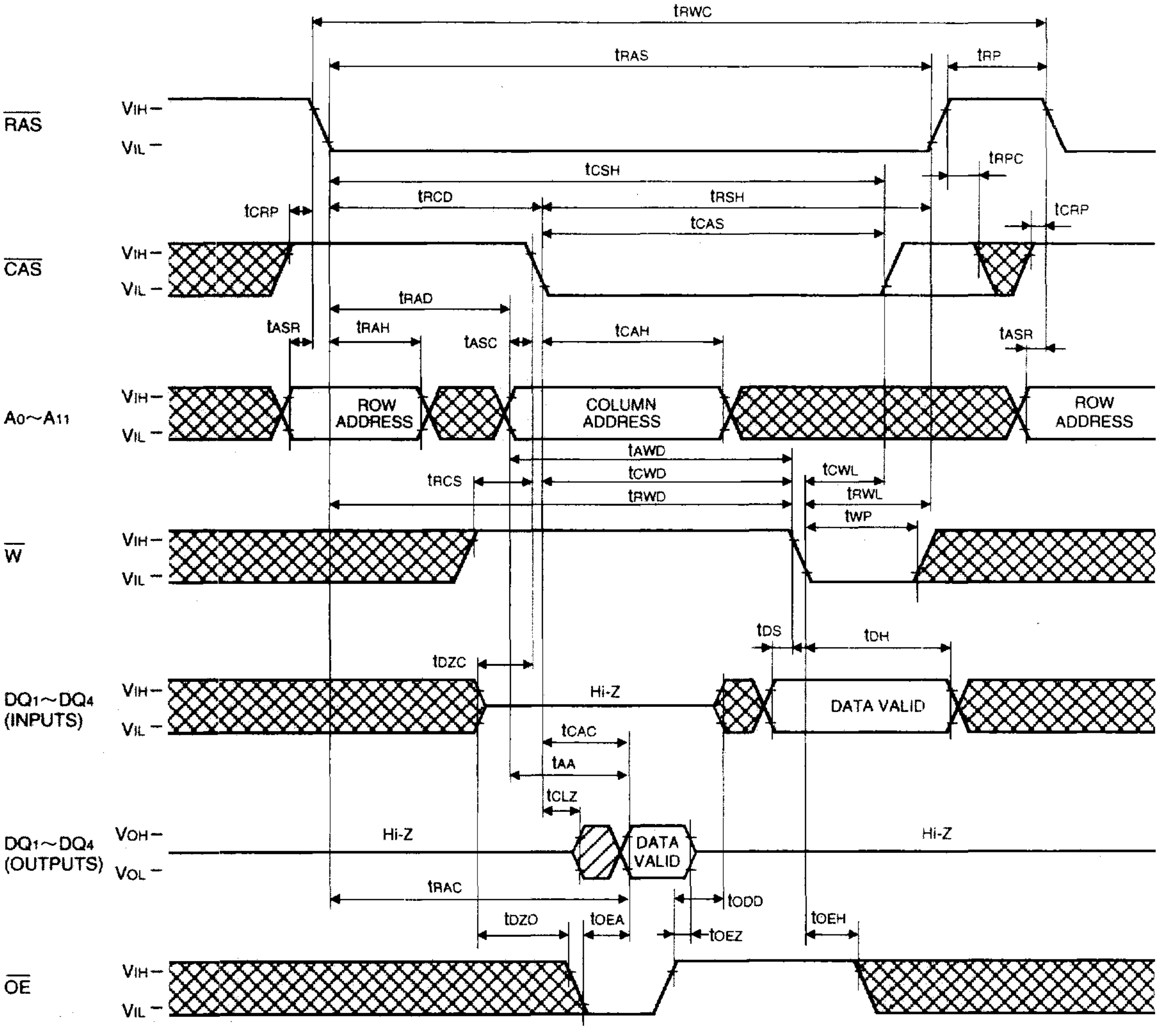


M5M4V16405CJ,TP-5,-5S : Under development

Delayed Write Cycle

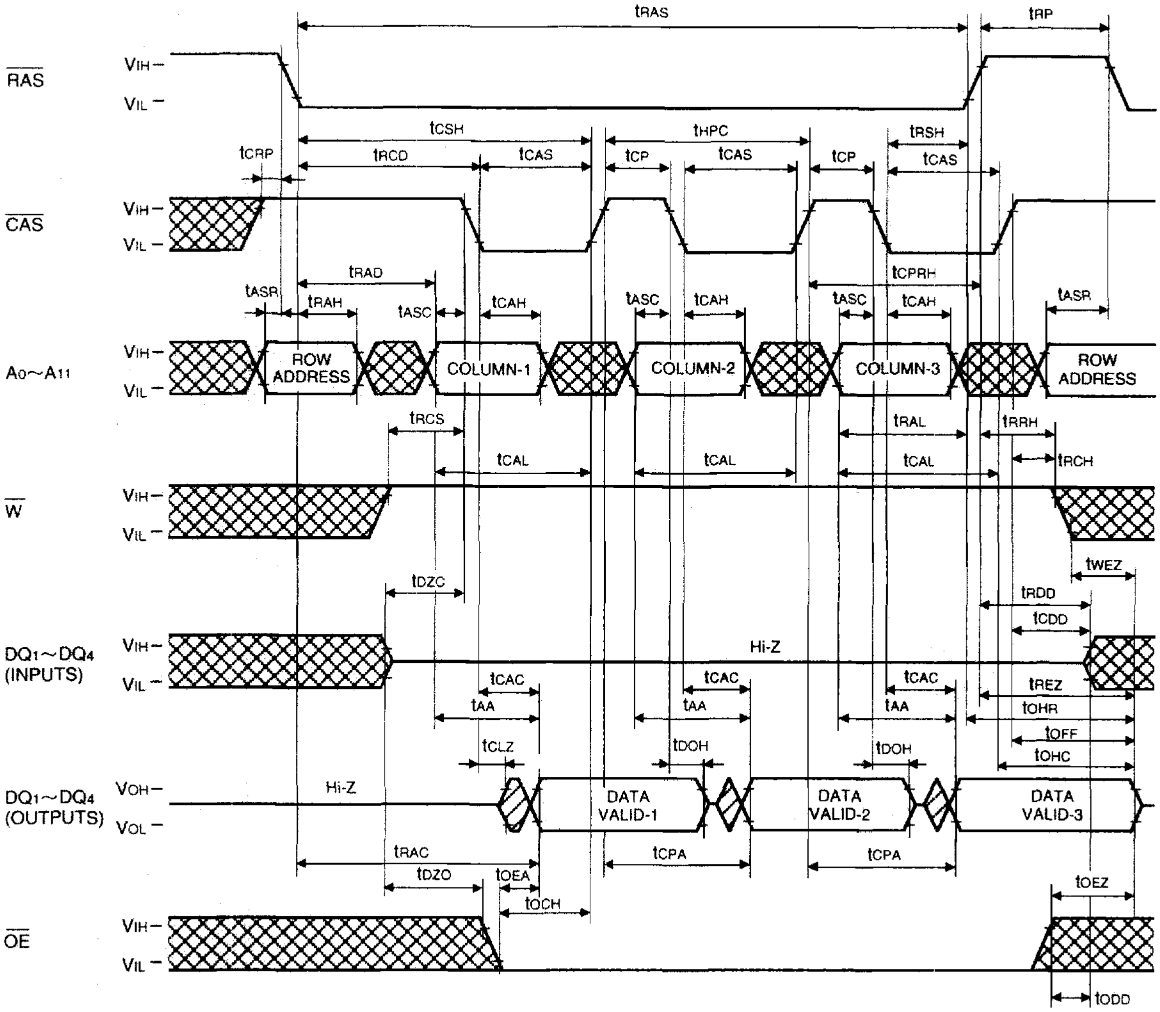


Read-Write, Read-Modify-Write Cycle



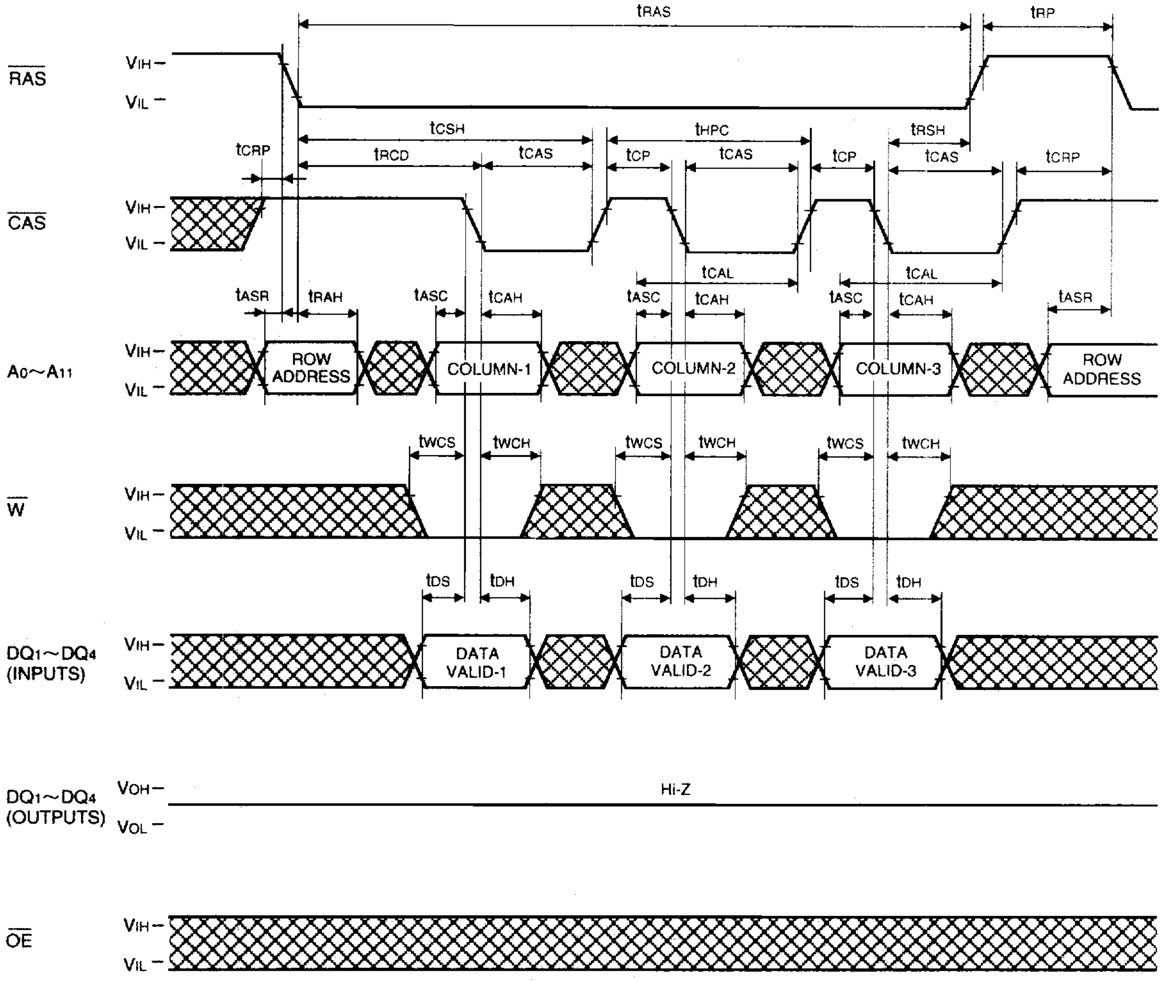
M5M4V16405CJ,TP-5,-5S : Under development

Hyper Page Mode Read Cycle



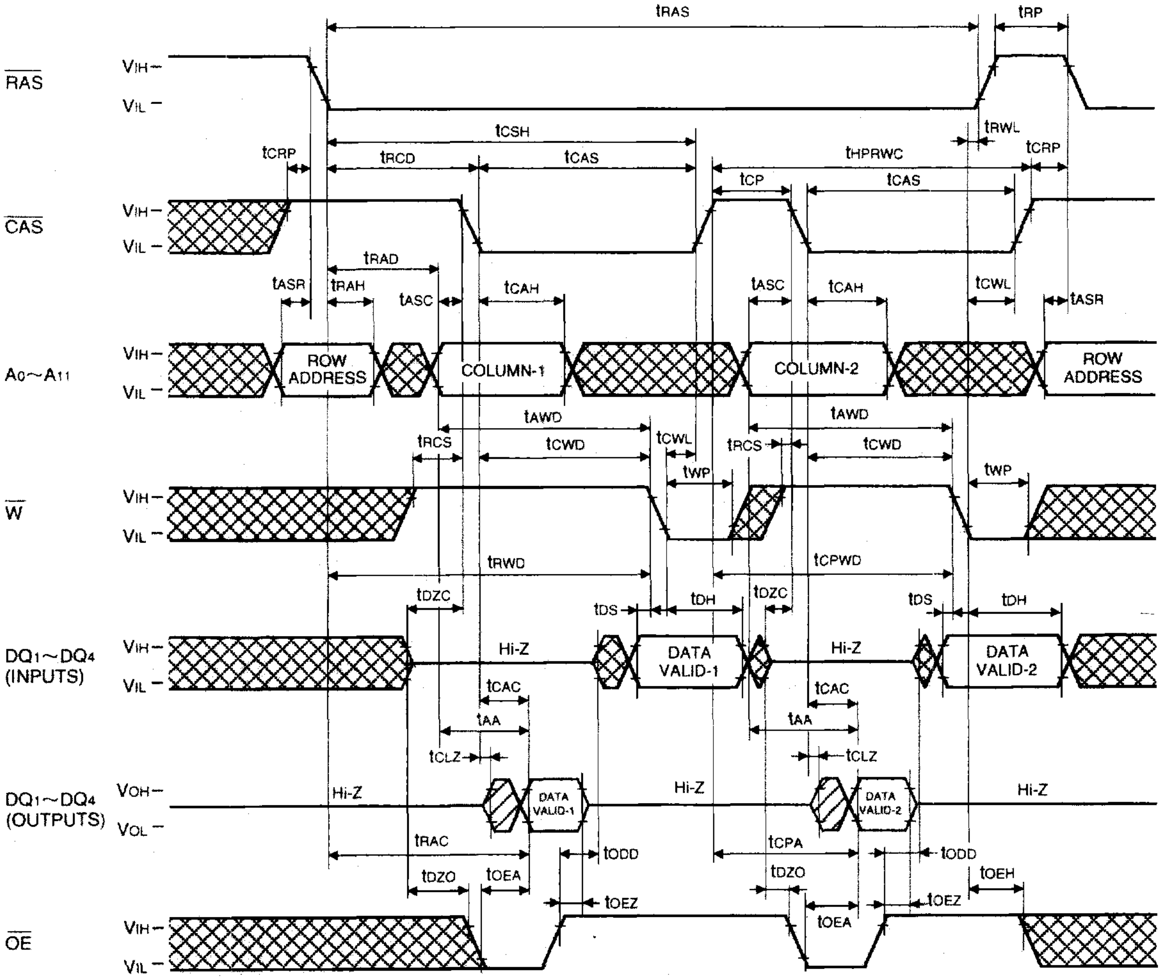
M5M4V16405CJ,TP-5,-5S : Under development

Hyper Page Mode Early Write Cycle



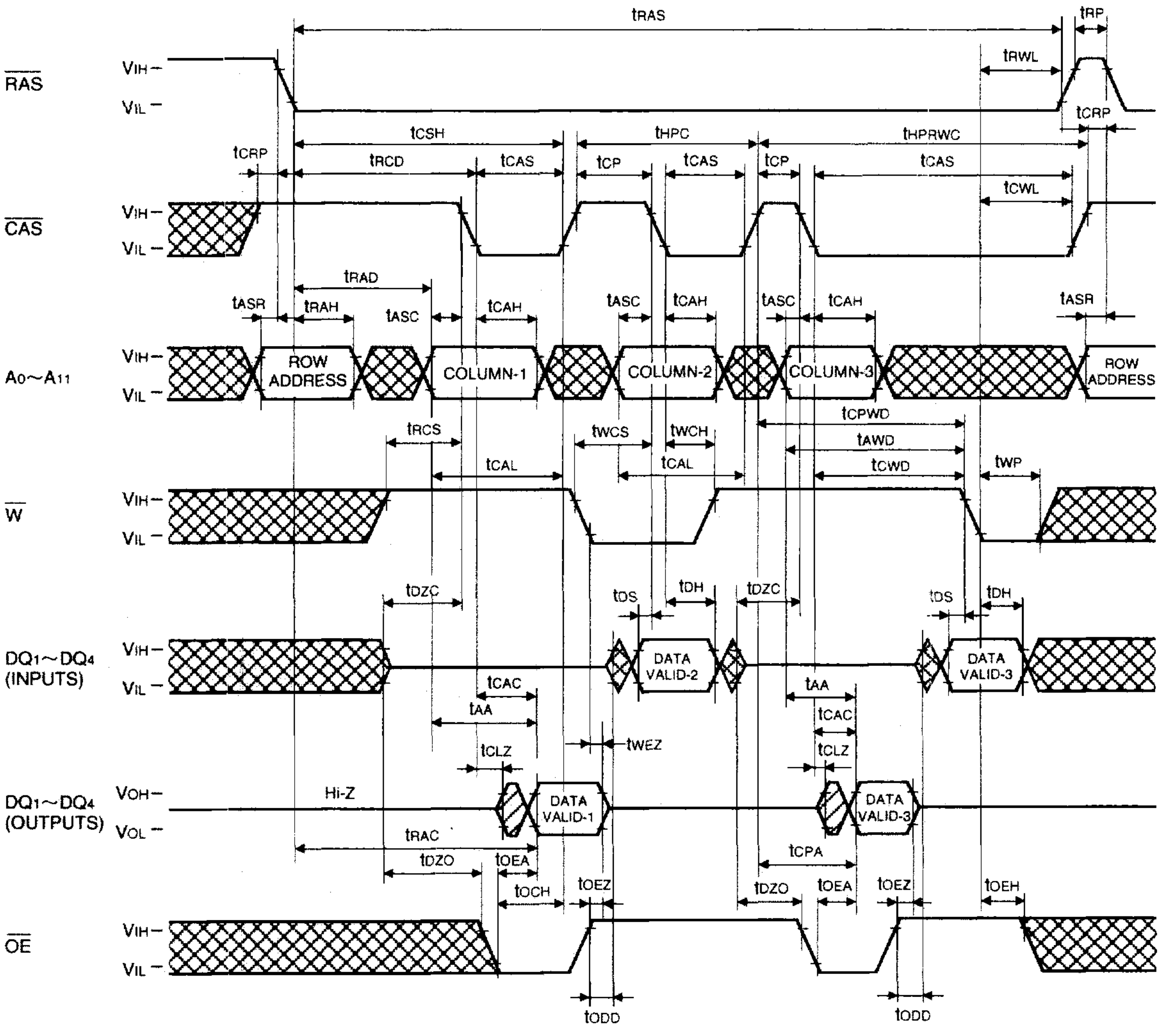
M5M4V16405CJ,TP-5,-5S : Under development

Hyper Page Mode Read-Write, Read-Modify-Write Cycle



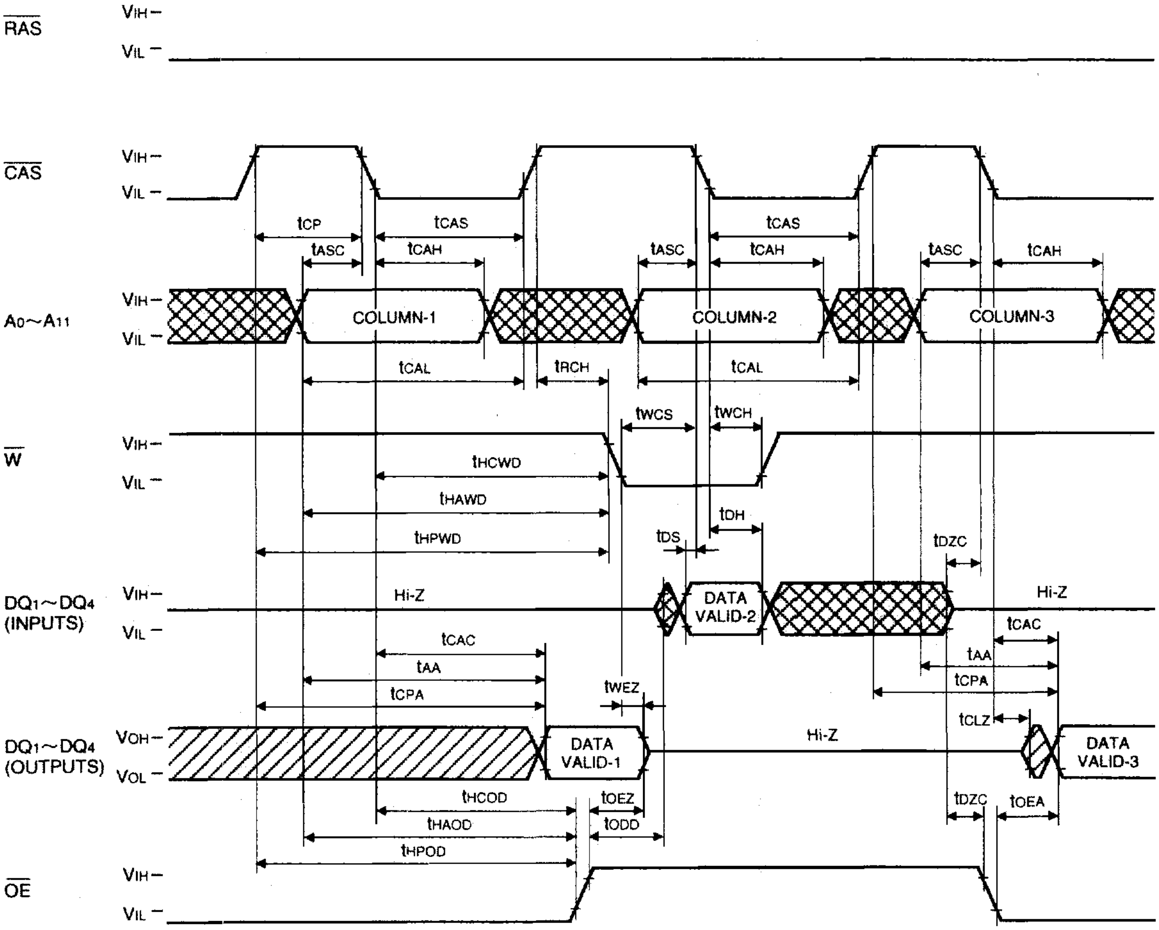
M5M4V16405CJ,TP-5,-5S : Under development

Hyper Page Mode Mix Cycle (1)



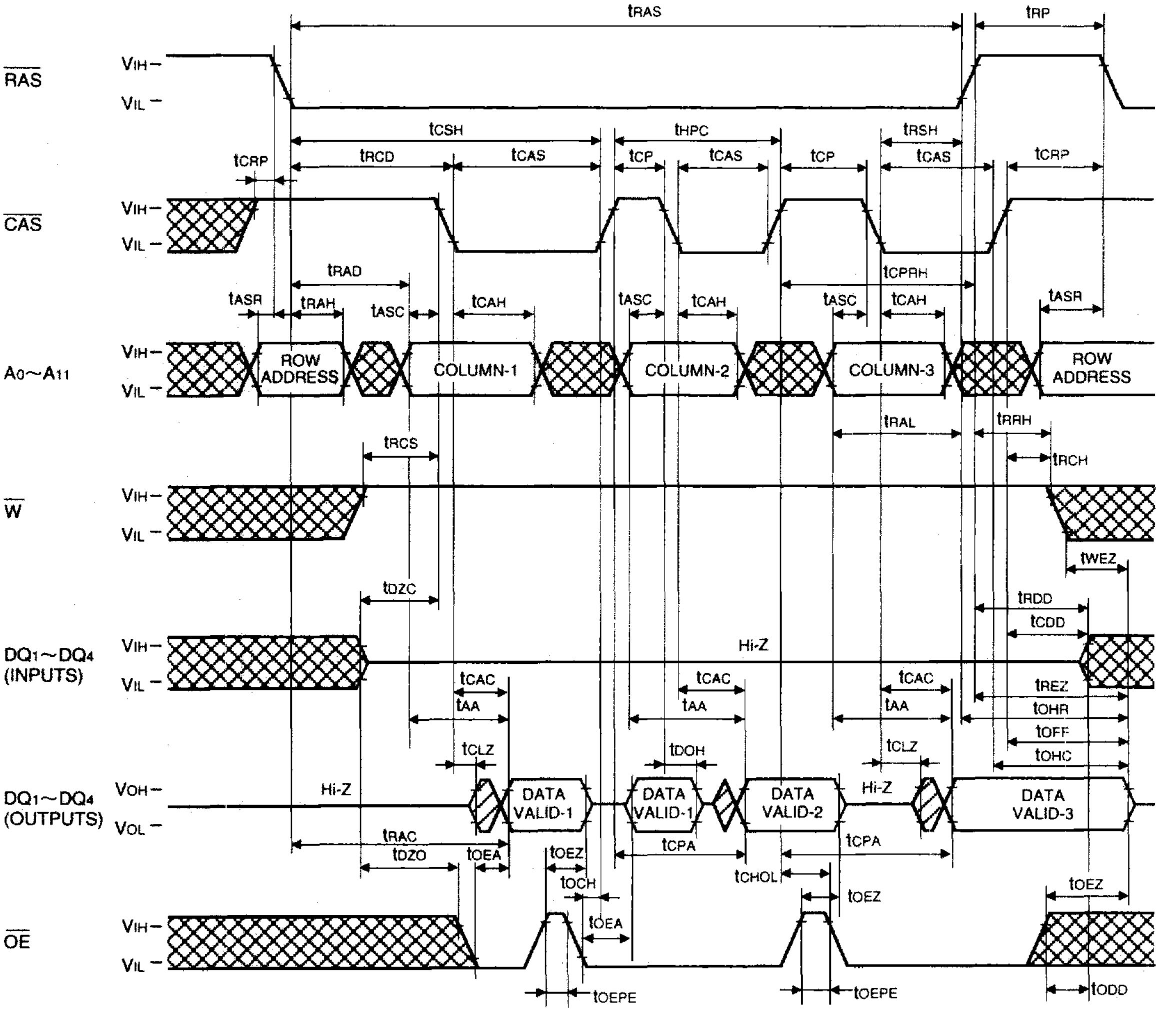
M5M4V16405CJ,TP-5,-5S : Under development

Hyper Page Mode Mix Cycle (2)

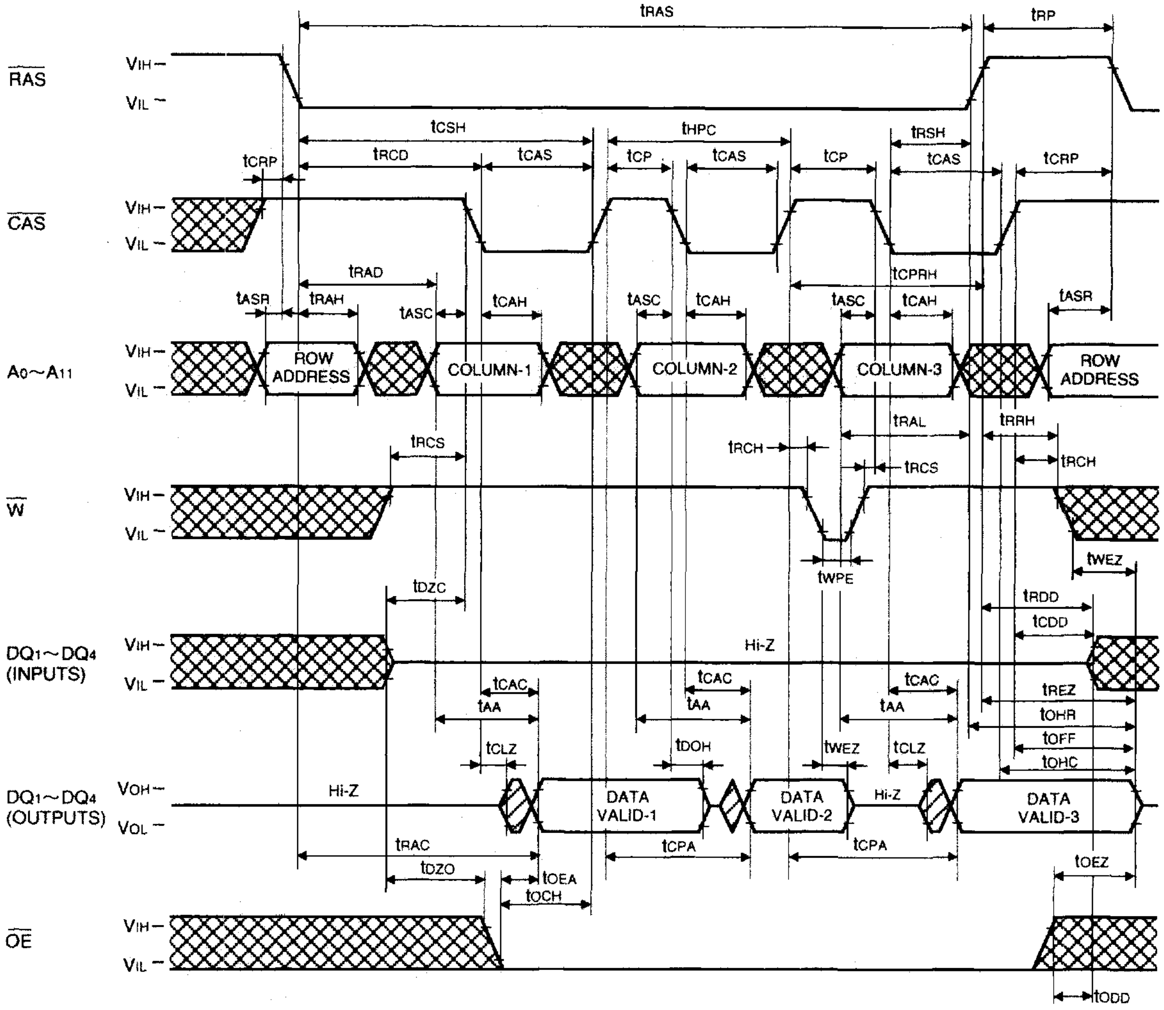


M5M4V16405CJ,TP-5,-5S : Under development

Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)

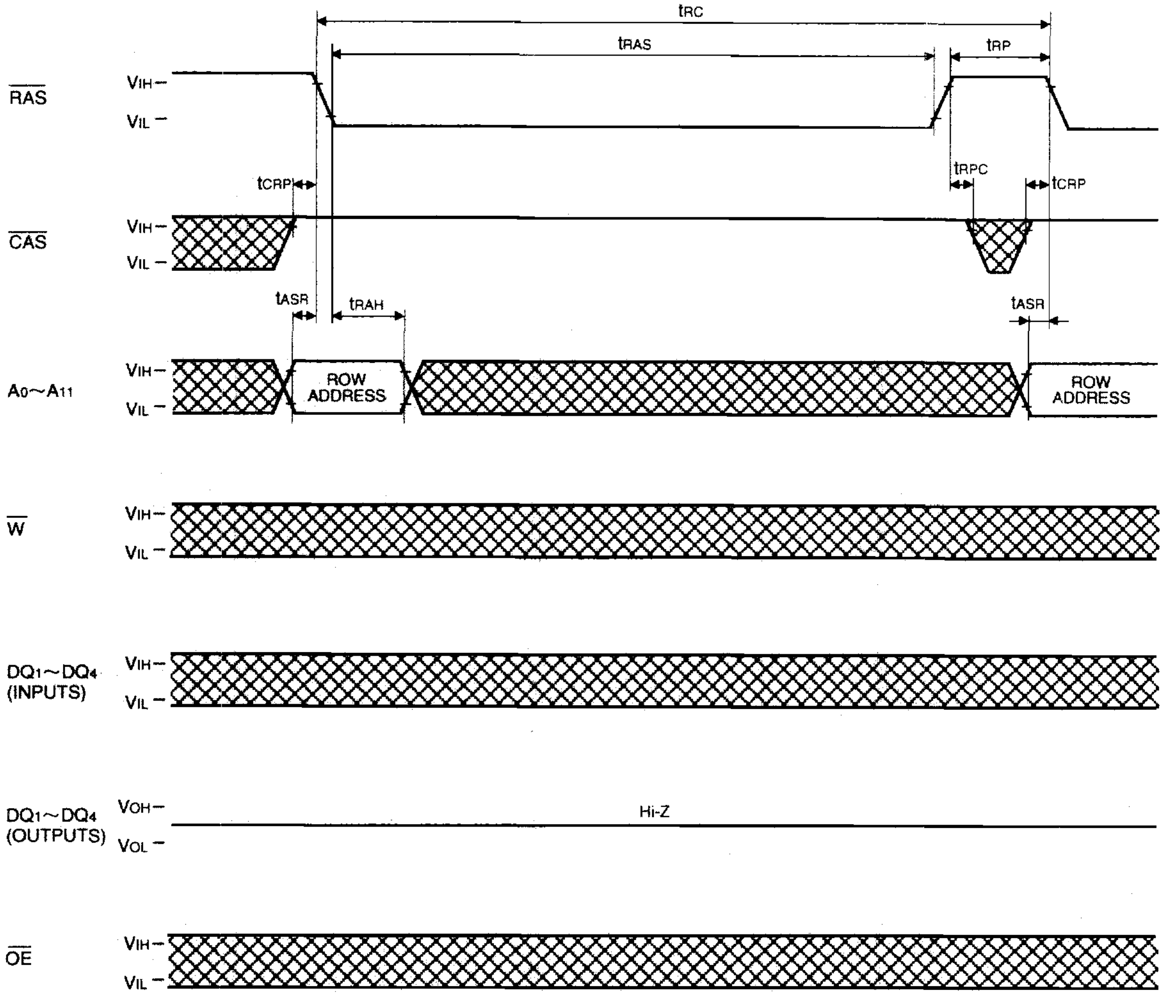


Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



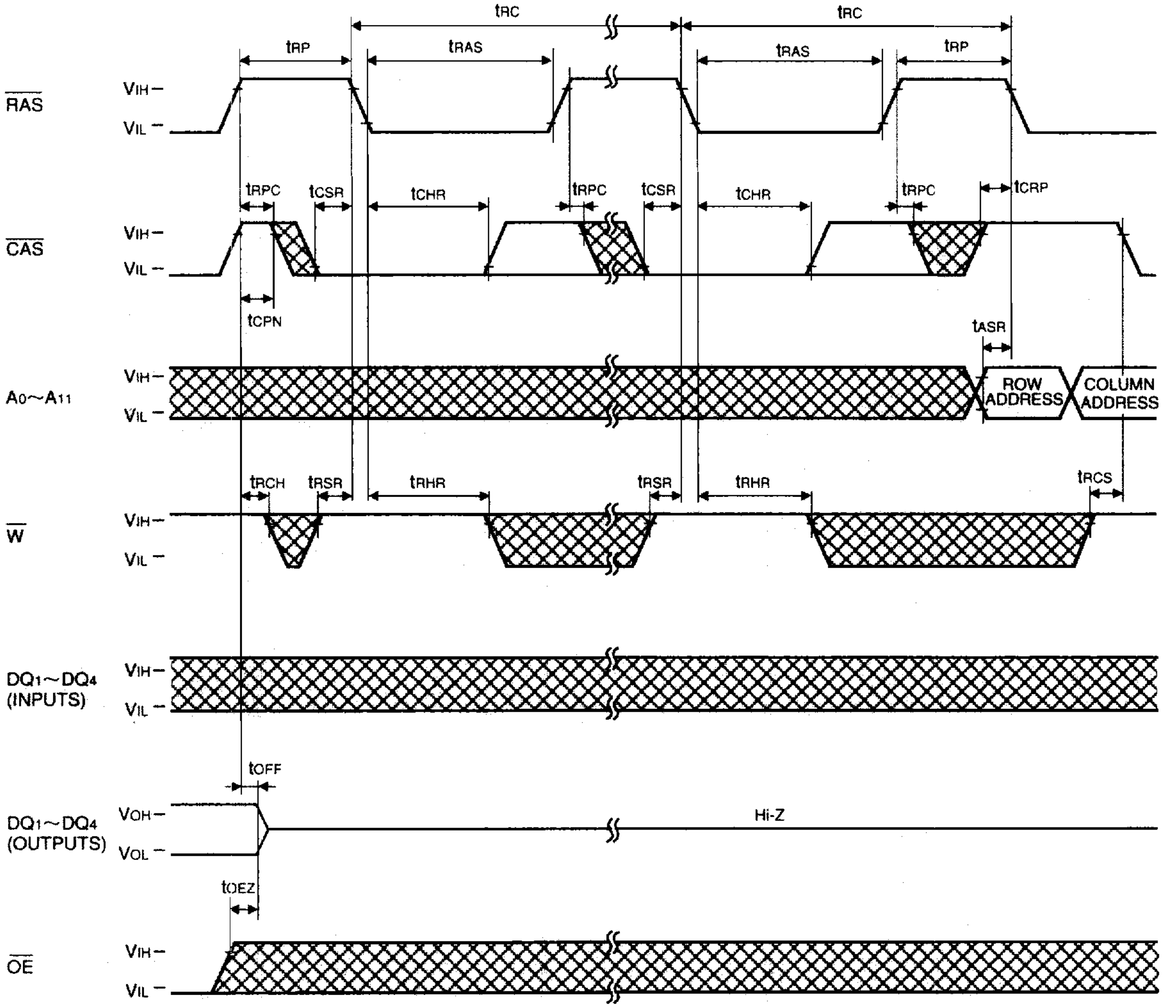
M5M4V16405CJ,TP-5,-5S : Under development

$\overline{\text{RAS}}$-only Refresh Cycle



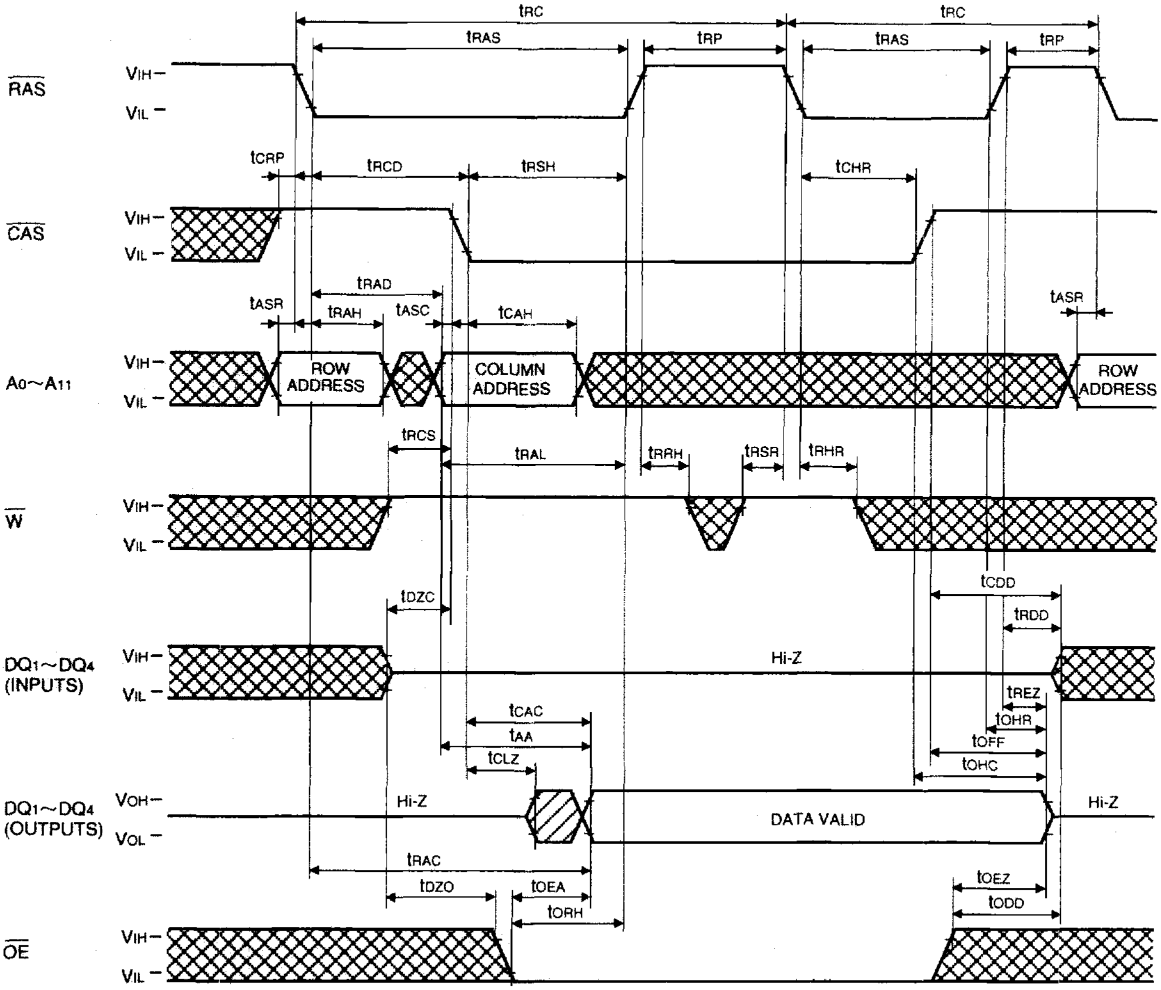
M5M4V16405CJ,TP-5,-5S : Under development

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Slow Refresh Cycle



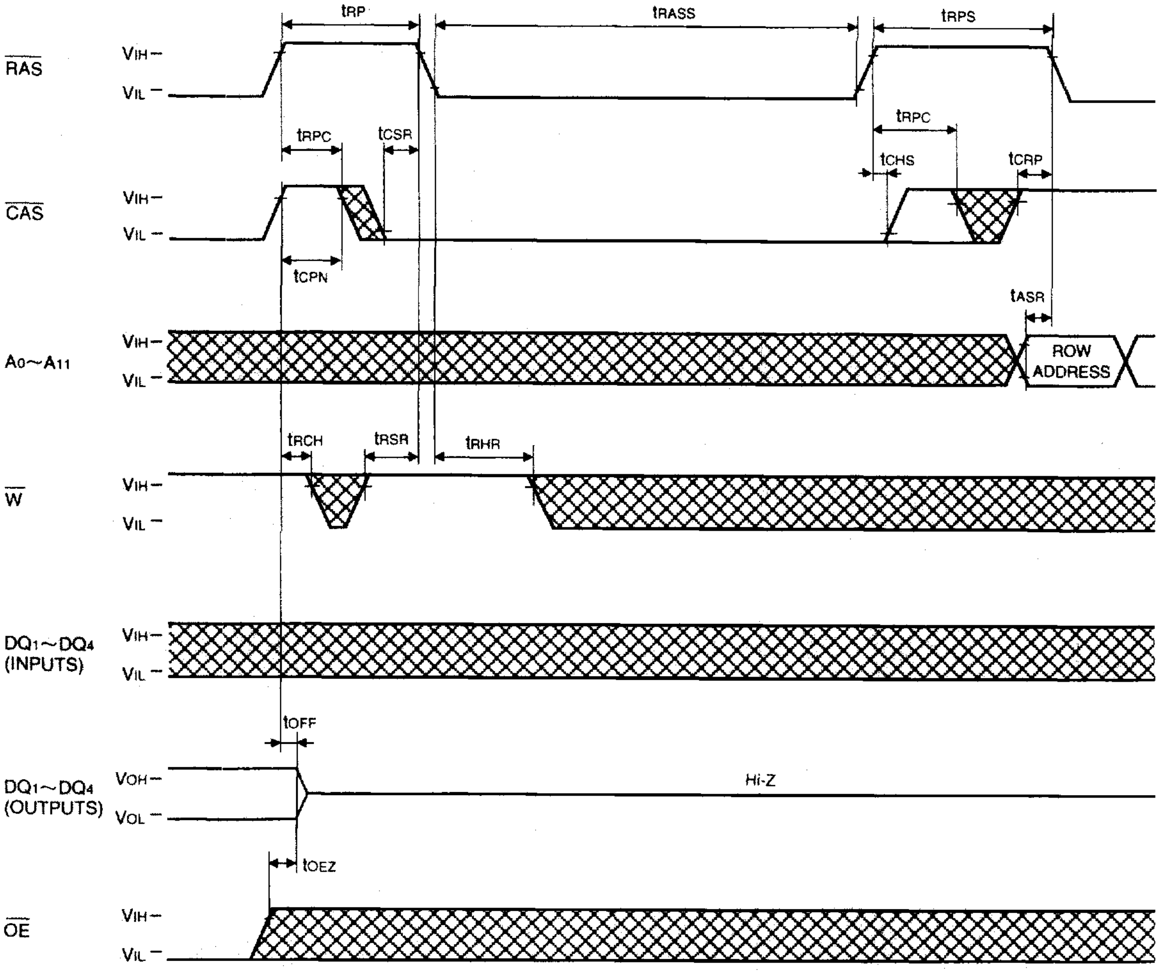
M5M4V16405CJ,TP-5,-5S : Under development

Hidden Refresh Cycle (Read) (Note 33)



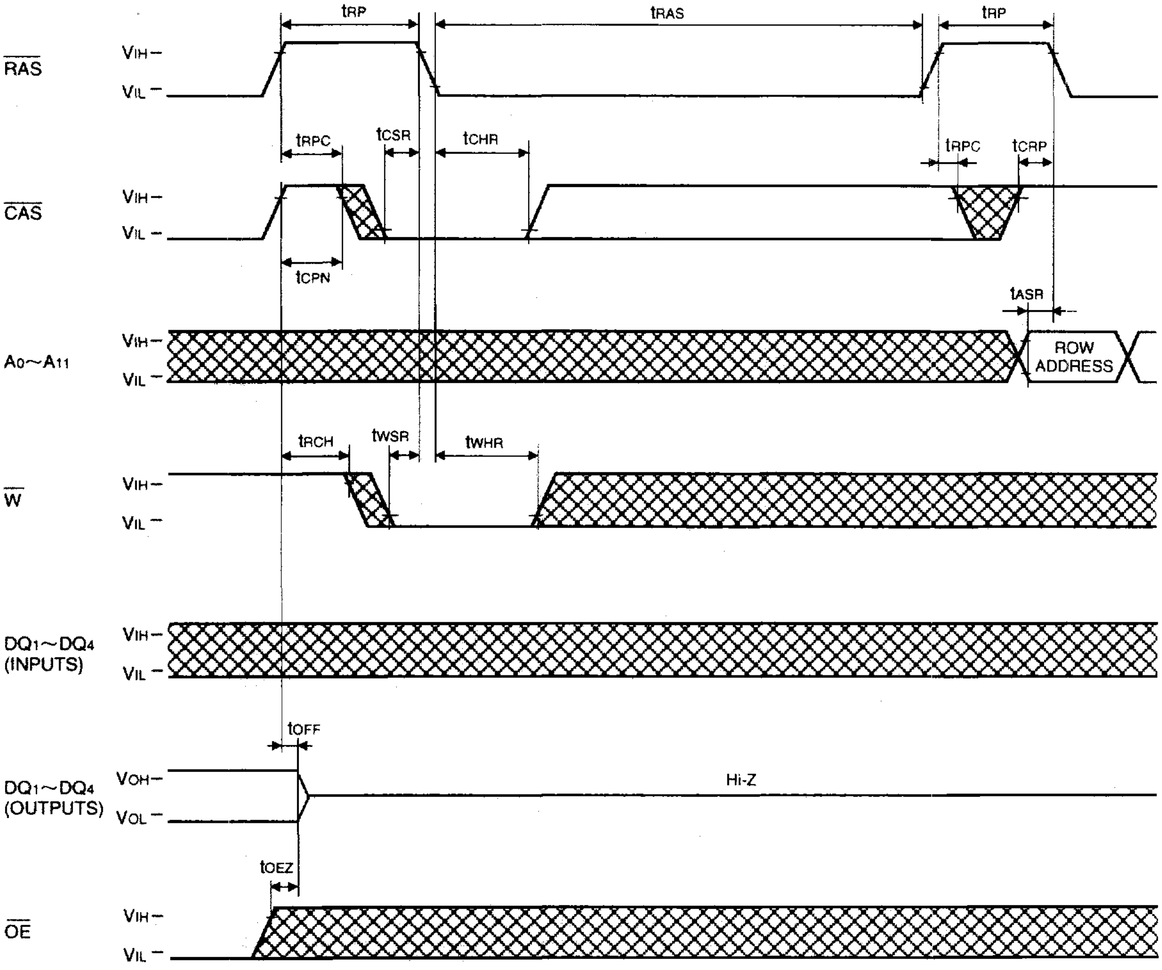
Note 33 : Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
In all cases tRSR and tRHR should be satisfied.

Self Refresh Cycle



M5M4V16405CJ,TP-5,-5S : Under development

TEST Mode SET Cycle



Note 34 : This cycle can be used for initialized cycle after power-up, however entried into Test Mode.