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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74AC194

4-bit Bidirectional Universal Shift Register



ADE-205-379 (Z)
1st. Edition
Sep. 2000

Description

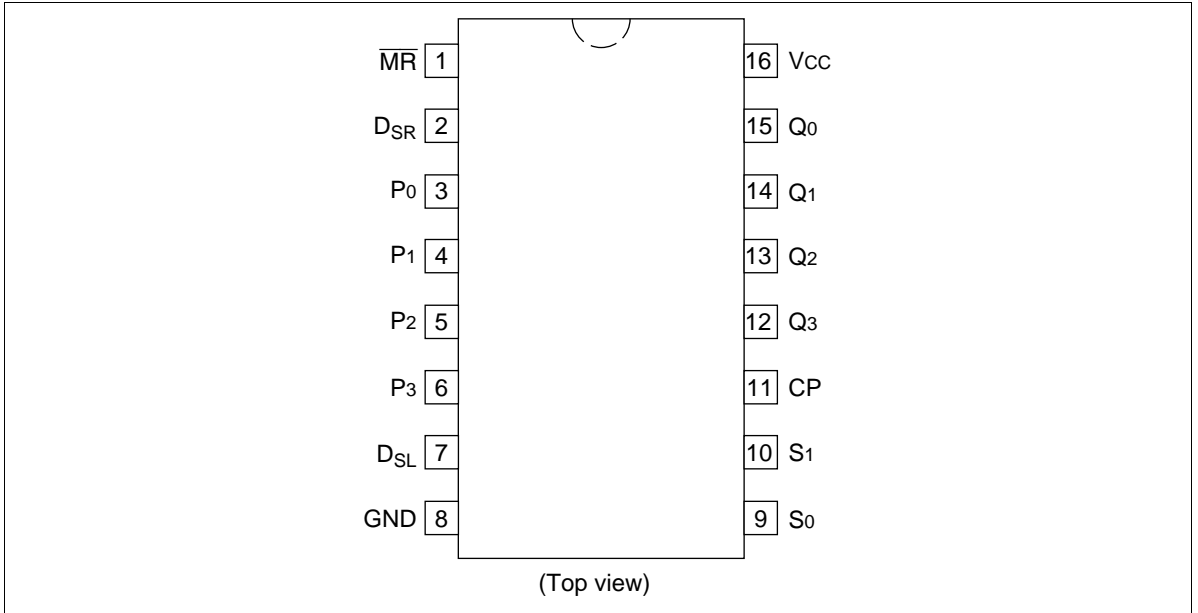
This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: parallel (broadside) load, shift right (in the direction Q_0 toward Q_3); shift left; inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1 , high. The data are loaded into their respective flip-flops and appear at the output after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shifts left serial input. Clocking of the flip-flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the clock input is high.

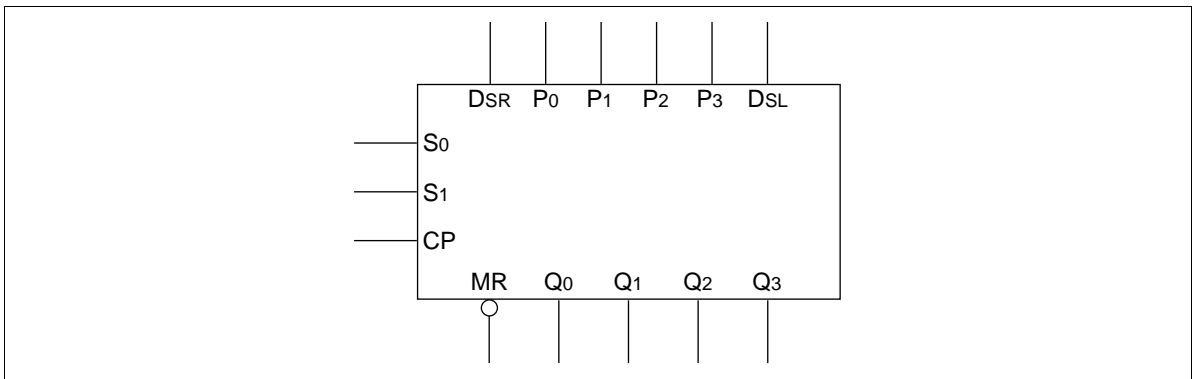
Features

- Asynchronous Master Reset
- Hole (Do Nothing) Mode
- Outputs Source/Sink 24 mA

Pin Arrangement



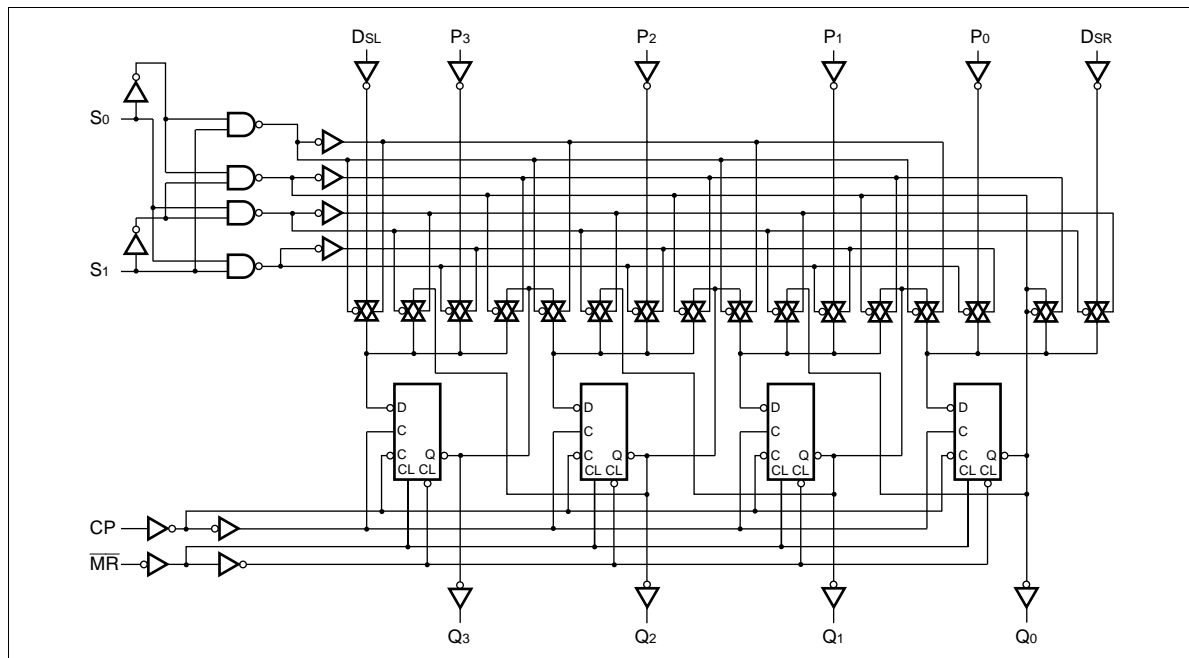
Logic Symbol



Pin Names

- S₀, S₁ Mode Control Inputs
- P₀ to P₃ Parallel Data Inputs
- D_{SR} Serial Data Input (Shift Right)
- D_{SL} Serial Data Input (Shift Left)
- CP Clock Pulse Input (Active Rising Edge)
- $\overline{\text{MR}}$ Asynchronous Master Reset Input (Active LOW)
- Q₀ to Q₃ Parallel Outputs

Logic Diagram



Mode Select Table

Operating Mode	Inputs						Output			
	MR	S ₁	S ₀	D _{SR}	D _{SL}	P _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	L	L	X	X	X	q ₀	q ₁	q ₂	q ₃
Shift Left	H	H	L	X	L	X	q ₁	q ₂	q ₃	L
	H	H	L	X	H	X	q ₁	q ₂	q ₃	H
Shift Right	H	L	H	L	X	X	L	q ₀	q ₁	q ₂
	H	L	H	H	X	X	H	q ₀	q ₁	q ₂
Parallel Load	H	H	H	X	X	p _n	p ₀	p ₁	p ₂	p ₃

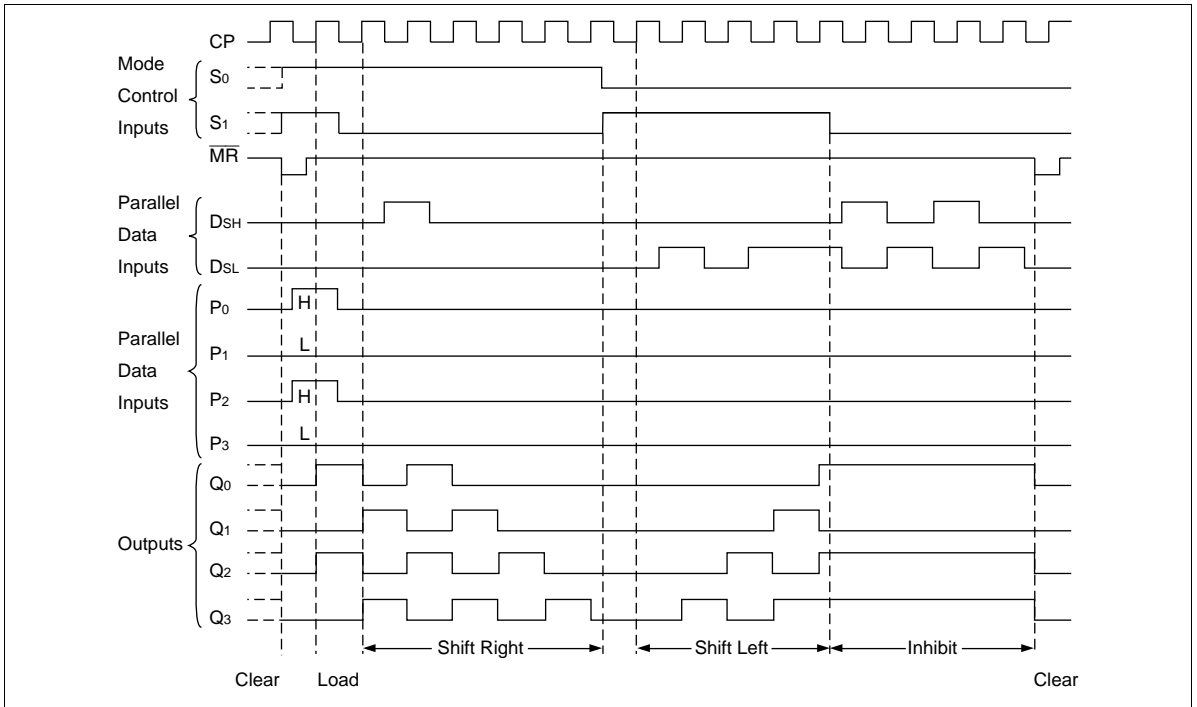
H : HIGH Voltage Level

L : LOW Voltage Level

p_n (q_n) : Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition

X : Immaterial

Timing Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$

AC Characteristics: HD74AC194

Item	Symbol	V _{CC} (V) ^{*1}	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	75	—	—	65	MHz	
		5.0	100	—	—	85		
Propagation delay CP to Q _n	t _{PLH}	3.3	1.0	—	13.0	1.0	15.0	ns
		5.0	1.0	—	10.0	1.0	11.5	
Propagation delay CP to Q _n	t _{PHL}	3.3	1.0	—	13.0	1.0	15.0	ns
		5.0	1.0	—	10.0	1.0	11.5	
Propagation delay $\overline{\text{MR}}$ to Q _n	t _{PHL}	3.3	1.0	—	10.5	1.0	12.5	ns
		5.0	1.0	—	8.0	1.0	9.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC194

Item	Symbol	V _{CC} (V) ^{*1}	Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF		Unit
			Typ	Guaranteed Minimum	Guaranteed Minimum	Guaranteed Minimum	
Setup time, HIGH or LOW P _n or D _{SR} or D _{SL} to CP	t _{su}	3.3	—	5.5	7.0	ns	
		5.0	—	4.0	5.0		
Hold time, HIGH or LOW P _n or D _{SR} or D _{SL} to CP	t _h	3.3	—	2.0	3.0	ns	
		5.0	—	1.5	2.0		
Setup time, HIGH or LOW S _n to CP	t _{su}	3.3	—	6.0	7.5	ns	
		5.0	—	4.5	5.5		
Hold time, HIGH or LOW S _n to CP	t _h	3.3	—	0.0	0.0	ns	
		5.0	—	0.0	0.0		
Recovery time $\overline{\text{MR}}$ to CP	t _{rec}	3.3	—	0.5	0.5	ns	
		5.0	—	0.5	0.5		
Pulse width	t _w	3.3	—	5.5	7.0	ns	
		5.0	—	4.5	5.0		

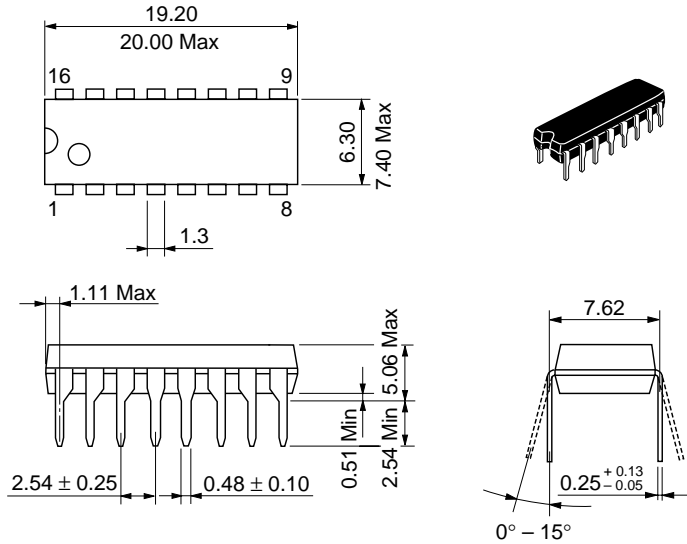
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5\text{ V}$
Power dissipation capacitance	C_{PD}	100	pF	$V_{CC} = 5.0\text{ V}$

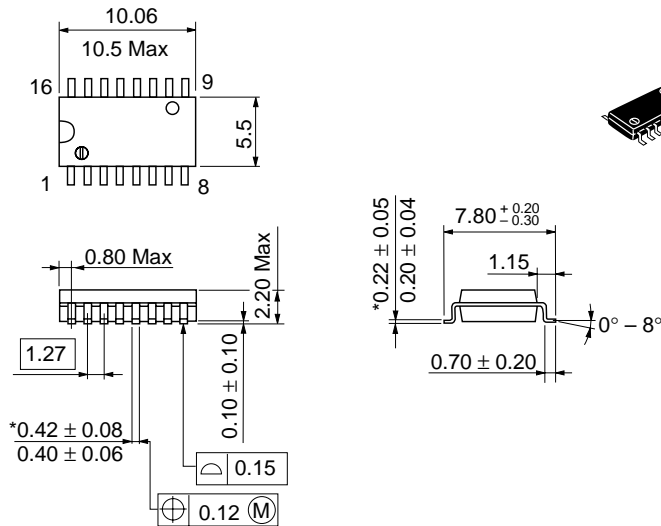
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

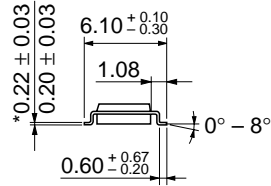
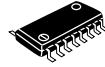
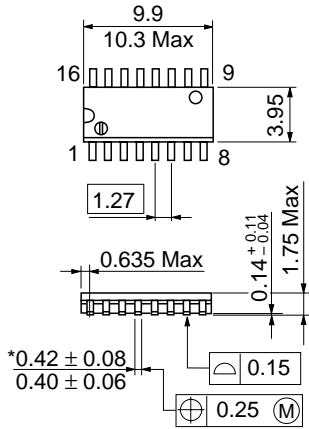
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

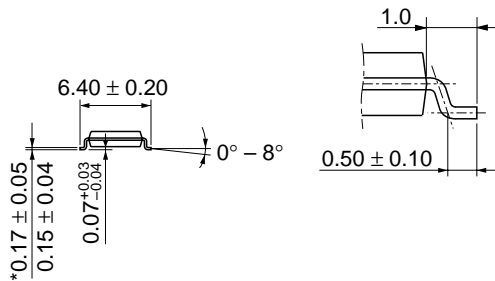
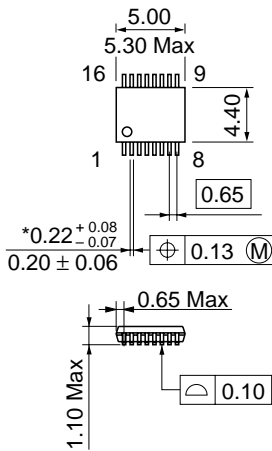
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
	Europe	:	http://www.hitachi-eu.com/hel/ecg
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
URL : <http://www.hitachi.com.hk>

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