

# WESTERN DIGITAL

C O R P O R A T I O N

WD5869

## WD5869 Dynamic Shift Register

### FEATURES

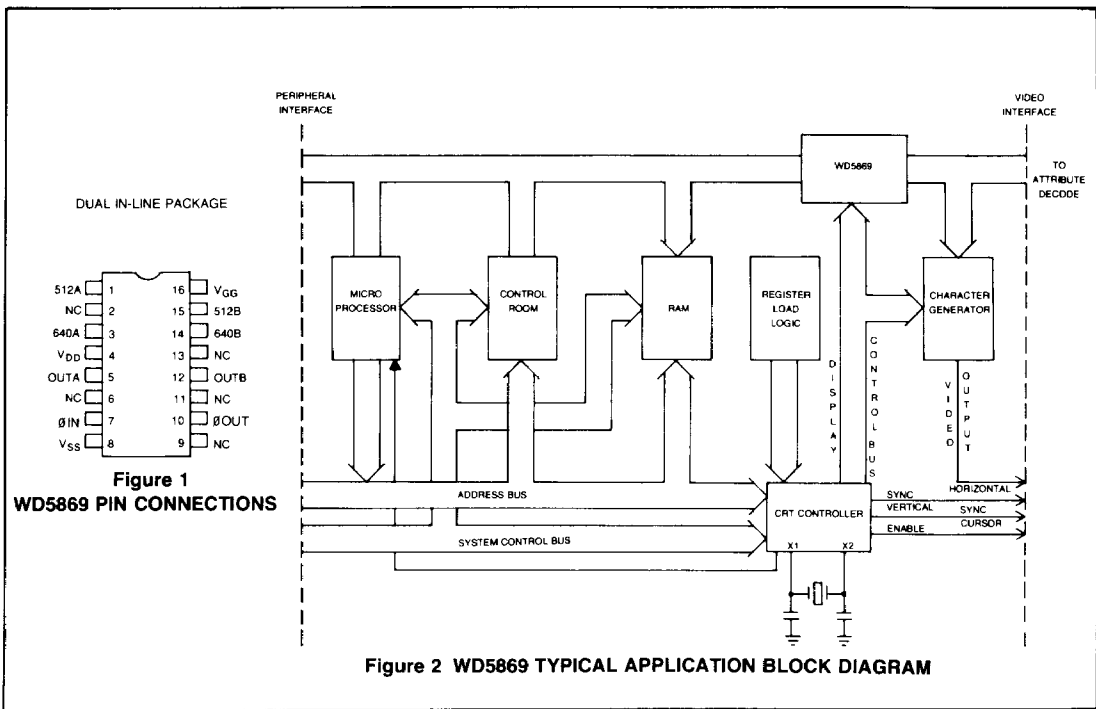
- DUAL 640 BIT
- ADDITIONAL TAPS AT 512 ON EACH REGISTER
- INTERNAL CLOCKING
- HIGH SPEED
- 3 STATE OUTPUT BUFFER

### GENERAL DESCRIPTION

The WD5869 Dual 640 Bit Dynamic Shift Register is a monolithic MOS integrated circuit designed for use in computer display peripherals. The clocks and recirculate logic are internal to reduce system component count, and 3 state output buffers provide bus interface. The WD5869 is available in a 16 pin molded plastic package, or a 16 pin ceramic package.

### APPLICATIONS

- CRT DISPLAYS
- COMPUTER PERIPHERALS
- CRYPTOGRAPHY



**SPECIFICATIONS**

**ABSOLUTE MAXIMUM RATINGS**

Data and Clock Input Voltage and Supply Voltages with respect to VSS

+0.3V to -20V

Power Dissipation

800mW at TA = 25°C

Storage Temperature

-55°C to +125°C (Plastic Package)  
-65°C to +150°C (Ceramic Package)

**TABLE 1 D.C. PARAMETERS**

**ELECTRICAL CHARACTERISTICS (DC)**

TA = 0°C to + 50°C, VSS = +5V ± 5%, VDD = -5V ± 5%, VGG = -12V ± 5%

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
I <sub>DD</sub>	POWER SUPPLY CURRENT		-50	mA	
	DATA INPUT LEVELS				
V <sub>IL</sub>	Logical Low Level	V <sub>SS</sub> -17.9	V <sub>SS</sub> -4.2	V	
V <sub>IH</sub>	Logical High Level	V <sub>SS</sub> -1.7	V <sub>SS</sub> +0.3	V	
I <sub>IL</sub>	DATA INPUT LEAKAGE		10	μA	V <sub>IN</sub> = -5V; All other Pins GND
C <sub>di</sub>	DATA INPUT CAPACITANCE		10	pf	V <sub>IN</sub> = 0V; f = 1MHZ, All other Pins GND
	CLOCK INPUT LEVELS				
V <sub>OH</sub>	Logical High Level	V <sub>SS</sub> -1.0	V <sub>SS</sub> +0.3	V	
V <sub>OL</sub>	Logical Low Level	V <sub>SS</sub> -17.9	V <sub>SS</sub> -14.5	V	
I <sub>CL</sub>	CLOCK INPUT LEAKAGE		10	μA	V <sub>O</sub> = -17.9V; All other Pins GND
C <sub>ci</sub>	CLOCK INPUT CAPACITANCE		200	pf	V <sub>O</sub> = 0V; f = 1MHZ, All other Pins GND
	DATA OUTPUT LEVELS				
V <sub>OH</sub>	Logical High Level	2.4		V	I Source = -50mA
V <sub>OL</sub>	Logical Low Level		V <sub>SS</sub> -0.4	V	I Sink = 1.6 mA

TABLE 2 A.C. PARAMETERS

WD5869

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
$\phi f$	CLOCK FREQUENCY	10	2000	KHz	$\phi tr = \phi tf = 20 \text{ ns}$
$\phi pw \text{ in}$	CLOCK PULSE WIDTH, In	0.15	1.0	$\mu\text{s}$	$\phi tf + \phi pw + \phi tr \leq 3.0 \text{ uS}$
$\phi pw \text{ out}$	CLOCK PULSE WIDTH, Out	1	1	$\phi pw \text{ in}$	
$\phi d$	CLOCK PHASE DELAY TIME, from rising edge	10		ns	
$\phi d$	CLOCK PHASE DELAY TIME, from falling edge	10		ns	
$\phi tr$	CLOCK TRANSITION TIME, rising edge		1.0	$\mu\text{s}$	$\phi tf + \phi pw + \phi tr \leq 3.0 \text{ uS}$
$\phi tf$	CLOCK TRANSITION TIME, falling edge		1.0	$\mu\text{s}$	
tds	DATA INPUT SET-UP TIME	80		ns	
tdh	DATA INPUT HOLD TIME	40		ns	
tpdl	DATA OUTPUT PROPAGATION DELAY, to low level		200	ns	
tpdh	DATA OUTPUT PROPAGATION DELAY, to high level		200	ns	

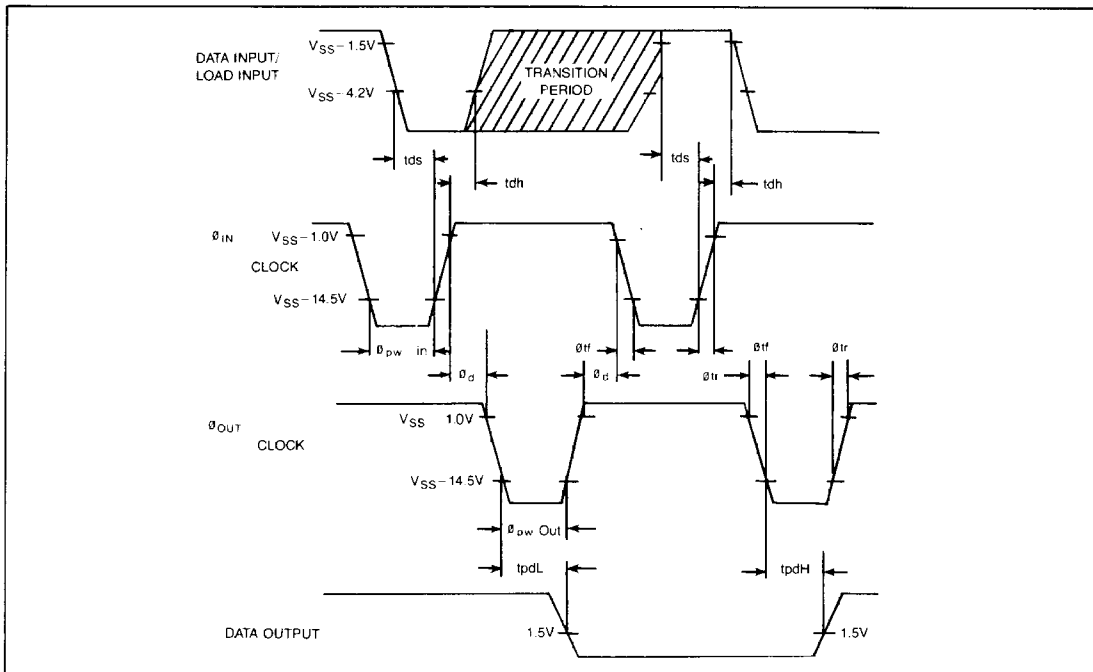


Figure 3 WD5869 TIMING DIAGRAM