MOTOROLA

# Military 54F521

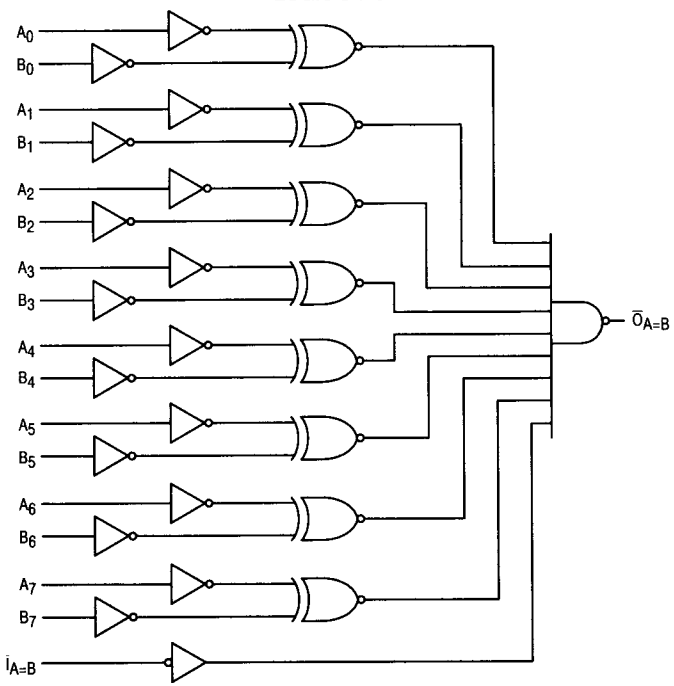
# 8-Bit Identity Comparator

**ELECTRICALLY TESTED PER:**
**MIL-M-38510/34701**

The 54F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

- Compares Two 8-Bit Words in 6.5 ns Typical
- Expandable To Any Word Length
- 20-Pin Package

**LOGIC DIAGRAM**




| TRUTH TABLE | | |
|---|---|---|
| Inputs | | Output |
| $\overline{I}_{A=B}$ | A, B | $\overline{O}_{A=B}$ |
| L | A = B* | L |
| L | A ≠ B | H |
| H | A = B* | H |
| H | A ≠ B | H |

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

**AVAILABLE AS:**

1) JAN: N/A
2) SMD: N/A
3) 883: 54F521/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

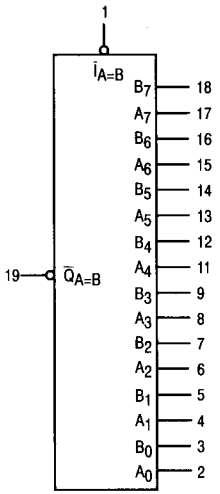
**PIN ASSIGNMENTS**

| FUNCT. | DIL 732-03 | FLATS 737-02 | LCC 756A-02 | BURN-IN (COND. A) |
|---|---|---|---|---|
| $\overline{I}_{A=B}$ | 1 | 1 | 1 | $V_{CC}$ |
| $A_0$ | 2 | 2 | 2 | $V_{CC}$ |
| $B_0$ | 3 | 3 | 3 | $V_{CC}$ |
| $A_1$ | 4 | 4 | 4 | $V_{CC}$ |
| $B_1$ | 5 | 5 | 5 | $V_{CC}$ |
| $A_2$ | 6 | 6 | 6 | $V_{CC}$ |
| $B_2$ | 7 | 7 | 7 | $V_{CC}$ |
| $A_3$ | 8 | 8 | 8 | $V_{CC}$ |
| $B_3$ | 9 | 9 | 9 | $V_{CC}$ |
| GND | 10 | 10 | 10 | GND |
| $A_4$ | 11 | 11 | 11 | $V_{CC}$ |
| $B_4$ | 12 | 12 | 12 | $V_{CC}$ |
| $A_5$ | 13 | 13 | 13 | $V_{CC}$ |
| $B_5$ | 14 | 14 | 14 | $V_{CC}$ |
| $A_6$ | 15 | 15 | 15 | $V_{CC}$ |
| $B_6$ | 16 | 16 | 16 | $V_{CC}$ |
| $A_7$ | 17 | 17 | 17 | $V_{CC}$ |
| $B_7$ | 18 | 18 | 18 | $V_{CC}$ |
| $\overline{O}_{A=B}$ | 19 | 19 | 19 | OPEN |
| $V_{CC}$ | 20 | 20 | 20 | $V_{CC}$ |

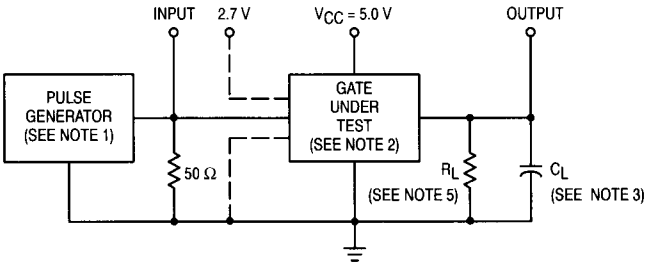
**BURN-IN CONDITIONS:**
**$V_{CC}$ = 5.0 V MIN/6.0 V MAX**

4

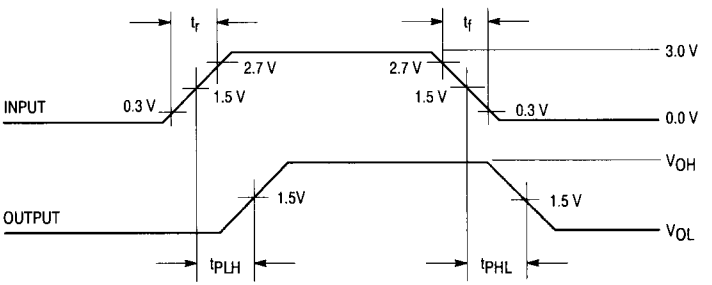
## LOGIC SYMBOL



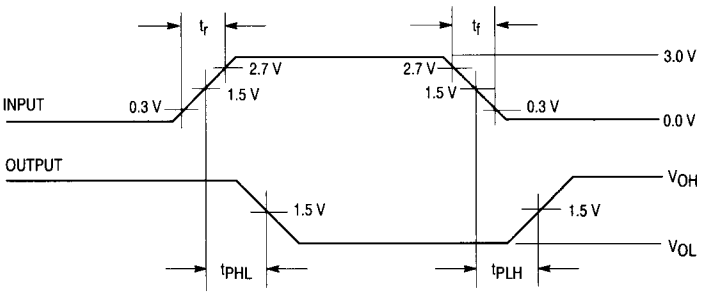

## TEST CIRCUIT



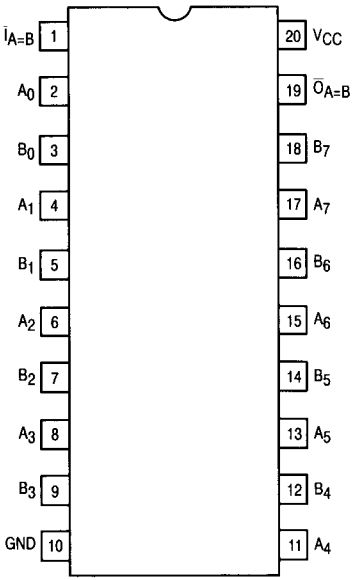

## WAVEFORM FOR IN-PHASE PROPAGATION DELAYS




## WAVEFORM FOR OUT-OF-PHASE PROPAGATION DELAYS




## CONNECTION DIAGRAM




**NOTES:**

1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, $t_p = 200$ ns, $Z_{OUT} \approx 50\ \Omega$, and PRR = 1.0 MHz.
2. Terminal conditions (pins not designated may be high $\geq 2.0$ V, low $\leq 0.8$ V, or open).
3. $C_L = 50$ pF $\pm$ 10%, including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 500\ \Omega \pm 5.0\%$.

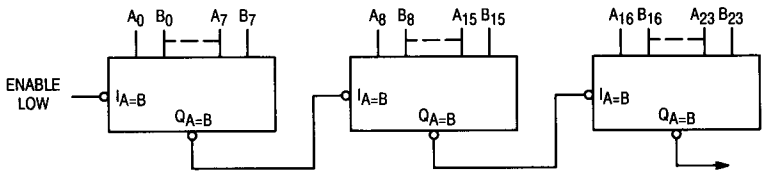
| Symbol | Parameter | Limits | | | | | | Unit | Test Condition (Unless Otherwise Specified) |
|---|---|---|---|---|---|---|---|---|---|
| | Static Parameters: | + 25°C | | + 125°C | | − 55°C | | | |
| | | Subgroup 1 | | Subgroup 2 | | Subgroup 3 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| $V_{OH}$ | Logical "1" Output Voltage | 2.5 | | 2.5 | | 2.5 | | V | $V_{CC}$ = 4.5 V, $I_{OH}$ = −1.0 mA, $V_{IN}$ = 2.0 V or 0.8 V, other inputs are GND. |
| $V_{OL}$ | Logical "0" Output Voltage | | 0.5 | | 0.5 | | 0.5 | V | $V_{CC}$ = 4.5 V, $I_{OL}$ = 20 mA, $V_{IN}$ = 0.8 V, other inputs are GND. |
| $V_{IC}$ | Input Clamping Voltage | | −1.2 | | | | | V | $V_{CC}$ = 4.5 V, $I_{IN}$ = −18 mA, other inputs are open. |
| $I_{IH}$ | Logical "1" Input Current | | 20 | | 20 | | 20 | µA | $V_{CC}$ = 5.5 V, $V_{IH}$ = 2.7 V, other inputs are open. |
| $I_{IHH}$ | Logical "1" Input Current | | 100 | | 100 | | 100 | µA | $V_{CC}$ = 5.5 V, $V_{IHH}$ = 7.0 V, other inputs are open. |
| $I_{OS}$ | Output Short Circuit Current | −60 | −150 | −60 | −150 | −60 | −150 | mA | $V_{CC}$ = 5.5 V, $V_{IN}$ = 5.5 V, other inputs are open, $V_{OUT}$ = 0 V. |
| $I_{IL}$ | Logical "0" Input Current | −0.03 | −0.6 | −0.03 | −0.6 | −0.03 | −0.6 | mA | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.5 V, other inputs are open. |
| $I_{CC}$ | Power Supply Current Off | | 32 | | 32 | | 32 | mA | $V_{CC}$ = 5.5 V, $V_{IN}$ = 5.5 V (all inputs). |
| $V_{IH}$ | Logical "1" Input Voltage | 2.0 | | 2.0 | | 2.0 | | V | $V_{CC}$ = 4.5 V. |
| $V_{IL}$ | Logical "0" Input Voltage | | 0.8 | | 0.8 | | 0.8 | V | $V_{CC}$ = 4.5 V. |
| | Functional Tests | Subgroup 7 | | Subgroup 8A | | Subgroup 8B | | | per Truth Table with $V_{CC}$ = 5.0 V, $V_{INL}$ = 0.5 V, and $V_{INH}$ = 2.5 V. |

4

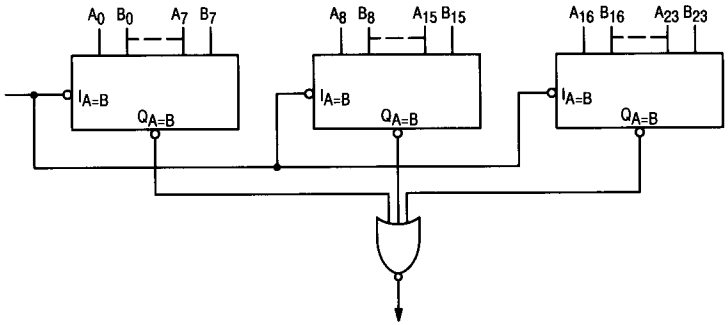
| Symbol | Parameter | Limits | | | | | | Unit | Test Condition (Unless Otherwise Specified) |
|---|---|---|---|---|---|---|---|---|---|
| | Switching Parameters: | + 25°C | | + 125°C | | − 55°C | | | |
| | | Subgroup 9 | | Subgroup 10 | | Subgroup 11 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PHL1}$ | Propagation Delay /Data-Output $A_n$ to $\overline{Q}_{A=B}$ | 1.5 | 10 | 1.0 | 15 | 1.0 | 15 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PLH1}$ | Propagation Delay /Data-Output $A_n$ to $\overline{Q}_{A=B}$ | 1.5 | 10 | 1.0 | 15 | 1.0 | 15 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PHL2}$ | Propagation Delay /Data-Output $B_n$ to $\overline{Q}_{A=B}$ | 1.5 | 10 | 1.0 | 15 | 1.0 | 15 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PLH2}$ | Propagation Delay /Data-Output $B_n$ to $\overline{Q}_{A=B}$ | 1.5 | 10 | 1.0 | 15 | 1.0 | 15 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PHL3}$ | Propagation Delay /Data-Output $\overline{I}_{A=B}$ to $\overline{Q}_{A=B}$ | 1.5 | 9.0 | 1.0 | 13.5 | 1.0 | 13.5 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PLH3}$ | Propagation Delay /Data-Output $\overline{I}_{A=B}$ to $\overline{Q}_{A=B}$ | 1.5 | 6.5 | 1.0 | 8.5 | 1.0 | 8.5 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PHL4}$ | Propagation Delay /Data-Output $A_n$ to $\overline{Q}_{A=B}$ | 1.5 | 10 | 1.0 | 15 | 1.0 | 15 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PLH4}$ | Propagation Delay /Data-Output $A_n$ to $\overline{Q}_{A=B}$ | 1.5 | 10 | 1.0 | 15 | 1.0 | 15 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PHL5}$ | Propagation Delay /Data-Output $B_n$ to $\overline{Q}_{A=B}$ | 1.5 | 10 | 1.0 | 15 | 1.0 | 15 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |
| $t_{PLH5}$ | Propagation Delay /Data-Output $B_n$ to $\overline{Q}_{A=B}$ | 1.5 | 10 | 1.0 | 15 | 1.0 | 15 | ns | $V_{CC}$ = 5.0 V, $C_L$ = 50 pF, $R_L$ = 500 Ω. |

## APPLICATION NOTE

### Ripple Expansion




### Parallel Expansion




4