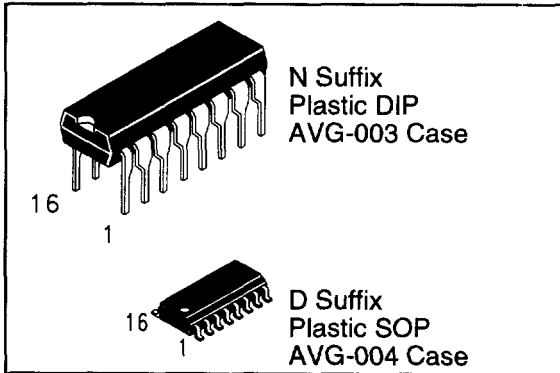


Dual JK Negative Edge-Triggered Flip-Flop

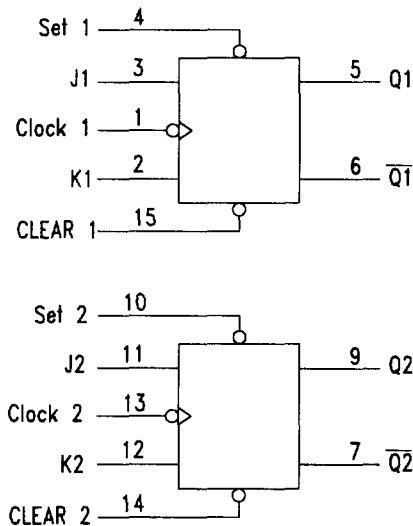
This device consists of two high-speed completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop by connecting the J and K inputs together.

- Advanced very high speed CMOS
- Outputs source/sink 24 mA
- Transmission line driving 50 ohms
- ACT has TTL compatible inputs
- Operation from 2 to 6 volts guaranteed
- DC & AC Parameters guaranteed over -40 to +85°C

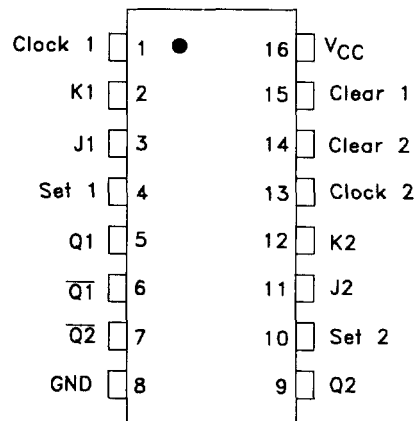
DV74AC112



LOGIC DIAGRAM



PIN ASSIGNMENT



PIN 16 = V_{CC}
PIN 8 = GND

TRUTH TABLE

Mode	Inputs				Output	
	Set	Clear	J	K	Q	Q̄
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
Undertermined *	L	L	X	X	H	H
Toggle	H	H	h	h	q̄	q
Load "0" (Reset)	H	H	l	h	L	H
Load "1" (Set)	H	H	h	l	H	L
Hold	H	H	i	l	q	q̄

H,h = High Level Logic

L,l = Low Level Logic

X = Don't Care

l,h,q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

* Both outputs will be HIGH while both Set and Clear are LOW, but the output states are unpredictable if Set and Clear go HIGH simultaneously.

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ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	AC112	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	± 20	mA
I _{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	± 50	mA
T _{STG}	Storage Temperature	- 65 to +150	°C

GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	2.0	5.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage, (Ref. to GND)	0		V _{CC}	V
t _r , t _f	Input Rise and Fall Time (V _{IN} from 30% to 70% V _{CC})			150	ns/V
	V _{CC} @ 3.0 V			40	ns/V
	V _{CC} @ 4.5 V			25	ns/V
T _A	Operating Ambient Temperature Range	-40		85	°C
C _{IN}	Input Capacitance		4.5		pF
CPD	Power Dissipation Capacitance		35		pF

DC ELECTRICAL CHARACTERISTICS

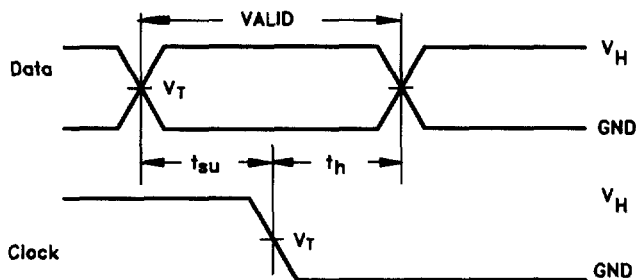
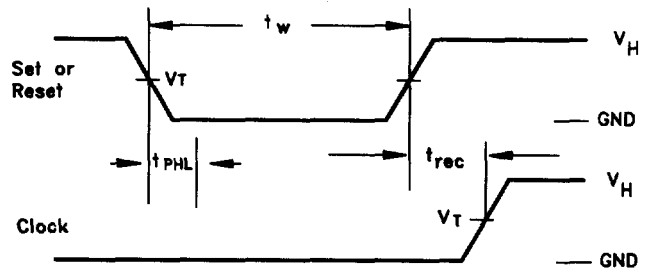
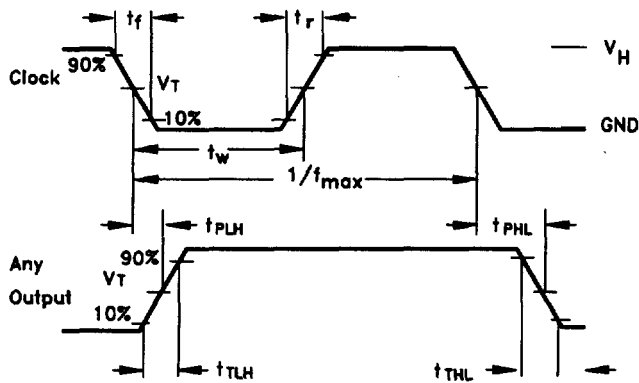
Symbol	Parameter	Conditions	V _{CC} (V)	AC112			Unit	
				T _A = +25°C		T _A = -40 to +85°C		
				Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	V _{OUT} = 0.1V or V _{CC} - 0.1 V	3.0	1.5	2.1	2.1	V	
			4.5	2.25	3.15	3.15		
			5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	V _{OUT} = 0.1V or V _{CC} - 0.1 V	3.0	1.5	0.9	0.9	V	
			4.5	2.25	1.35	1.35		
			5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	I _{OUT} = -50 μA	3.0	2.99	2.9	2.9	V	
			4.5	4.49	4.4	4.4		
			5.5	5.49	5.4	5.4		
		V _{IN} = V _{IL} or V _{IH}	-12mA	3.0		2.56	2.46	V
			I _{OH} -24mA	4.5		3.86	3.76	
	-24 mA	5.5		4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	I _{OUT} = 50 μA	3.0	0.002	0.1	0.1	V	
			4.5	0.001	0.1	0.1		
			5.5	0.001	0.1	0.1		
		V _{IN} = V _{IL} or V _{IH}	12mA	3.0		0.36	0.44	V
			I _{OL} 24mA	4.5		0.36	0.44	
	24 mA	5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	V _I = V _{CC} , GND	5.5		±0.1	±1.0	μA	
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5		4.0	40	μA	

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AC CHARACTERISTICS over full operating conditions

Symbol	Parameter	V _{CC} ±10% (V)	AC112				Unit
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		
			Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	3.3 5.0	145 145		125 125		MHz
t _{PLH}	Propagation Delay C _{Pn} to Q _n or Q _n	3.3 5.0	1.0 1.0	16.0 13.0	1.0 1.0	17.0 13.5	ns
t _{PHL}	Propagation Delay C _{Pn} to Q _n or Q _n	3.3 5.0	1.0 1.0	16.0 13.0	1.0 1.0	16.5 13.5	ns
t _{PLH}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	3.3 5.0	1.0 1.0	11.0 9.5	1.0 1.0	11.5 10.0	ns
t _{PHL}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	3.3 5.0	1.0 1.0	11.0 9.5	1.0 1.0	11.5 10.0	ns
t _s	Set-up Time, High or Low J _n or K _n to C _{Pn}	3.3 5.0	6.5 4.5		7.5 5.0		ns
t _h	Hold Time, High or Low J _n or K _n to C _{Pn}	3.3 5.0	0 0		0 0		ns
t _w	Pulse Width C _{Pn}	3.3 5.0	6.0 5.0		6.5 5.5		ns
t _w	Pulse Width C _{Dn} or S _{Dn}	3.3 5.0	6.0 5.0		7.5 5.5		ns
t _{rec}	Recovery Time C _{Dn} or S _{Dn} to C _P	3.3 5.0	0 0		0 0		ns

SWITCHING WAVEFORMS



Input and output threshold voltage:
 $V_T = 50\% V_{CC}$ for AC
 $V_H = V_{CC}$ for AC

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