HD66741

(128 x 80-dot Graphics LCD Controller/Driver)

HITACHI

Rev 0.1
July 20, 1998

Description

The HD66741, 128-by-80 dot-matrix graphics LCD controller and driver LSI, displays graphics such as kanji and pictograms. It can be configured to drive a dot-matrix liquid crystal display under the control of the microprocessor connected via the clock-synchronized serial or 4/8-bit bus. The HD66741 has a smooth vertical scroll display and a double-height display for the remaining bit map areas. It fixed-displays a part of the graphics icons so that the user can easily see a variety of information.

The HD66741 has various functions to reduce the power consumption of an LCD system such as low-voltage operation of 1.8 V min., a booster to generate maximum five-times LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions such as standby and sleep modes allows fine power control. The HD66741 is suitable for any portable battery-driven product requiring long-term driving capabilities such as cellular phones, pagers, or electronic wallets.

Features

- Control and drive of a 128 × 80-dot graphics LCD
- Fixed display of graphics icons (pictograms)
- 3 general ports built-in
- Low-power operation support:
  - Vcc = 1.8 to 5.5 V (low voltage)
  - V_{LCD} = 4.5 to 15.0 V (liquid crystal drive voltage)
  - Triple, quadruple, or five-times booster for liquid crystal drive voltage
  - 64-step contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors
  - Power-save functions such as the standby mode and sleep mode supported
  - Programmable drive duty ratios and bias values displayed on LCD
- High-speed clock-synchronized serial interface (serial transfer rate: 5 MHz max.)
- High-speed 4-/8-bit bus interface capability
- 128-segment × 80-common liquid crystal display driver
- Duty ratio and drive bias (selectable by program)
- Vertical smooth scroll

- Partial smooth scroll control (fixed display of graphics icons)
- Vertical double-height display by each display line
- Black-and-white reversed display
- No wait time for instruction execution and RAM access
- Internal oscillation and hardware reset
- n-raster-row AC liquid-crystal drive (C-pattern waveform drive)
- Shift change of segment and common driver

Table 1 Progammable Display Sizes and Duty Ratios

		Graphics Display				
Duty Ratio	**Optimum Drive Bias**	**Bit Map**	**12 x 13-dot Font Width**	**14 x 15-dot Font Width**	**16 x 16-dot Font Width**	**7 x 8-dot Font Width**
1/32	1/7	128 x 32 dots	2 lines x 10 characters	2 lines x 9 characters	2 lines x 8 characters	4 lines x 18 characters
1/40	1/7	128 x 40 dots	3 lines x 10 characters	2.5 lines x 9 characters	2.5 lines x 8 characters	5 line x 18 characters
1/48	1/8	128 x 48 dots	3 lines x 10 characters	3 lines x 9 characters	3 line x 8 characters	6 lines x 18 characters
1/56	1/8	128 x 56 dots	4 lines x 10 characters	3.5 lines x 9 characters	3.5 lines x 8 characters	7 lines x 18 characters
1/64	1/9	128 x 64 dots	5 lines x 10 characters	4 lines x 9 characters	4 lines x 8 characters	8 lines x 18 characters
1/72	1/9.5	128 x 72 dots	5 lines x 10 characters	4.5 lines x 9 characters	4.5 lines x 8 characters	9 lines x 18 characters
1/80	1/10	128 x 80 dots	6 lines x 10 characters	5 lines x 9 characters	5 lines x 8 characters	10 lines x 18 characters

<Target values>

Total Current Consumption Characteristics (Vcc = 3 V, TYP Conditions, LCD Drive Power Current Included)

				Total Power Consumption				
				Normal Display Operation				
Character Display Dot Size	Duty Ratio	R-C Oscillation Frequency	Frame Frequency	Internal Logic	LCD Power	Total*	Sleep Mode	Standby Mode
128 x 32 dots	1/32	75 kHz	73 Hz	(27 μA)	(16 μA)	Triple (75 μA)	(15 μA)	0.1 μA
128 x 40 dots	1/40	75 kHz	73 Hz	(27 μA)	(16 μA)	Triple (75 μA)	(15 μA)	
128 x 48 dots	1/48	75 kHz	74 Hz	(27 μA)	(16 μA)	Triple (75 μA)	(15 μA)	
128 x 56 dots	1/56	75 kHz	74 Hz	(27 μA)	(16 μA)	Triple (75 μA)	(15 μA)	
128 x 64 dots	1/64	75 kHz	73 Hz	(27 μA)	(18 μA)	Quadruple (99 μA)	(15 μA)	
128 x 72 dots	1/72	80 kHz	70 Hz	(32 μA)	(18 μA)	Quadruple (104 μA)	(15 μA)	
128 x 80 dots	1/80	90 kHz	70 Hz	(35 μA)	(20 μA)	Five-times (135 μA)	(15 μA)	

Note : When a triple, quadruple, or five-times booster is used:
the total power consumption = Internal logic current + LCD power current x 3 (triple booster),
the total power consumption = Internal logic current + LCD power current x 4 (quadruple booster), and
the total power consumption = Internal logic current + LCD power current x 5 (five-times booster)

Type Name

Types	External Dimensions	Operation Voltages
HD66741TB0	Bending TCP	1.8 V to 5.5 V
HCD66741BP	Au-bumped chip	

LCD Display Example

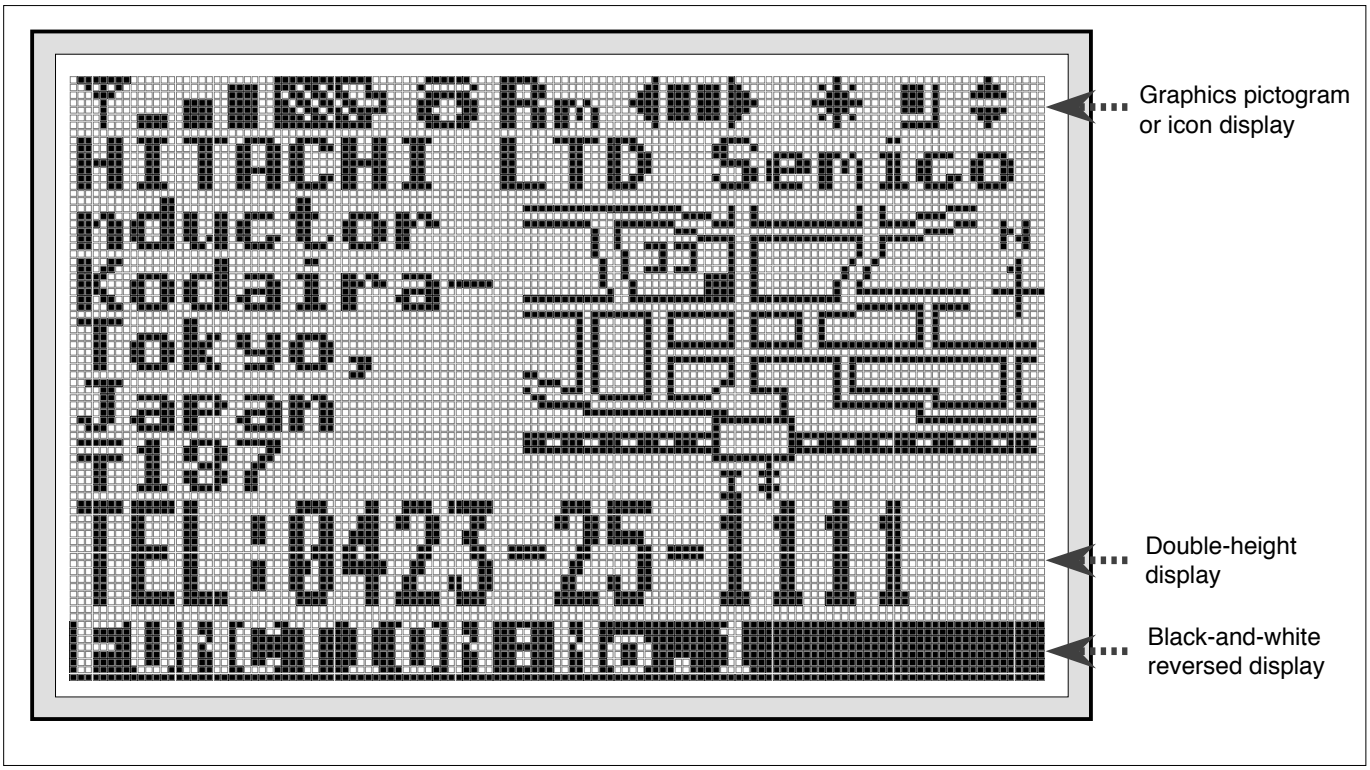


Figure 1 LCD Display Example

- 1/80 duty
- Graphics display area: 128 x 80 dots (dot matrix)
- Graphics-icon (pictogram) display at the top and bottom of the screen

LCD Family Comparison

Items	HD66705U	HD66717	HD66727
Character display sizes	12 characters x 2 lines	12 characters x 4 lines	12 characters x 4 lines
Graphic display sizes	—	—	—
Multiplexing icons	40	40	40
Annunciator	Static: 10	Static: 10	Static: 12
Key scan control	—	—	4 x 8
LED control ports	—	—	3
General output ports	—	—	3
Operating power voltages	2.4 V to 5.5 V	2.4 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 9 V	3 V to 13 V	3 V to 13 V
Serial bus	Clock-synchronized serial	I2C, Clock-synchronized serial	I2C, Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	—
Expansion driver control	Impossible	Impossible	Impossible
Liquid crystal drive duty ratios	1/10, 18	1/10, 18, 26, 34	1/10, 18, 26, 34
Liquid crystal drive biases	1/4	1/4, 1/6	1/4, 1/6
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Double or triple	Double or triple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	—	—	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	60 x 8	60 x 8	60 x 8
CGROM	9,600	9,600	11,520
CGRAM	32 x 5	32 x 5	32 x 6
SEGRAM	8 x 5	8 x 5	8 x 6
No. of CGROM fonts	240	240	240
No. of CGRAM fonts	4	4	4
Font sizes	5 x 8	5 x 8	5 x 8, 6 x 8
Bit map area	—	—	—
R-C oscillation resistor/ oscillation frequency	External resistor (40, 80 kHz)	External resistor (40-160 kHz)	External resistor (40-160 kHz)
Reset function	External	External	External
Low power control	Partial display off Oscillation off Liquid crystal power off	Partial display off Oscillation off Liquid crystal power off	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG only	SEG only	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-153	TCP-153	TCP-158
Bare chip	Yes	Yes	Yes
Bumped chip	Yes	Yes	Yes
No. of pins	153	153	158
Chip sizes	9.69 x 2.73	10.88 x 2.89	11.39 x 2.89
Pad intervals	120 μm	120 μm	120 μm

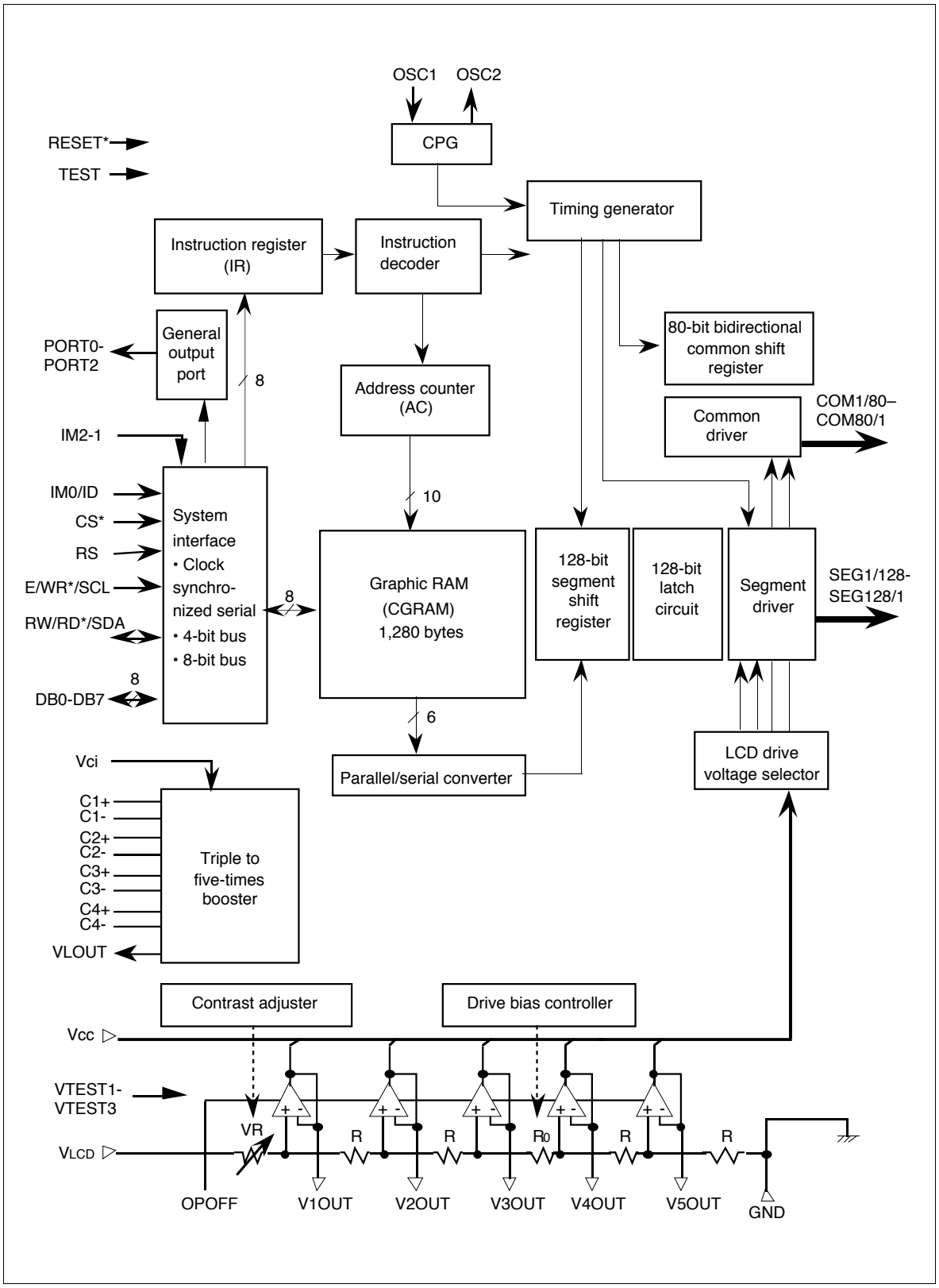
LCD Family Comparison (cont)

Items	HD66724	HD66725	HD66726
Character display sizes	12 characters x 3 lines	16 characters x 3 lines	16 characters x 5 lines
Graphic display sizes	72 x 26 dots	96 x 26 dots	96 x 42 dots
Multiplexing icons	144	192	192
Annunciator	1/2 duty: 144	1/2 duty: 192	1/2 duty: 192
Key scan control	8 x 4	8 x 4	8 x 4
LED control ports	—	—	—
General output ports	3	3	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 6.5 V	3 V to 6.5 V	4.5 V to 11 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	4 bits, 8 bits
Expansion driver control	Impossible	Impossible	Impossible
Liquid crystal drive duty ratios	1/2, 10, 18, 26	1/2, 10, 18, 26	1/2, 10, 18, 26, 34, 42
Liquid crystal drive biases	1/4 to 1/6.5	1/4 to 1/6.5	1/2 to 1/8
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Single, double or triple	Single, double, or triple	Single, double, triple, or quadruple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	3-dot unit	3-dot unit	—
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	20,736	20,736	20,736
CGRAM	384 x 8	384 x 8	480 x 8
SEGRAM	72 x 8	96 x 8	96 x 8
No. of CGROM fonts	240 + 192	240 + 192	240 + 192
No. of CGRAM fonts	64	64	64
Font sizes	6 x 8	6 x 8	6 x 8
Bit map areas	72 x 26	96 x 26	96 x 42
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor, incorporated (32 kHz)	External resistor, incorporated (50 kHz)
Reset function	External	External	External
Low power control	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG, COM	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-146	TCP-170	TCP-188
Bare chip	—	—	Yes
Bumped chip	Yes	Yes	Yes
No. of pins	146	170	188
Chip sizes	10.34 x 2.51	10.97 x 2.51	13.13 x 2.51
Pad intervals	80 μm	80 μm	100 μm

LCD Family Comparison (cont)

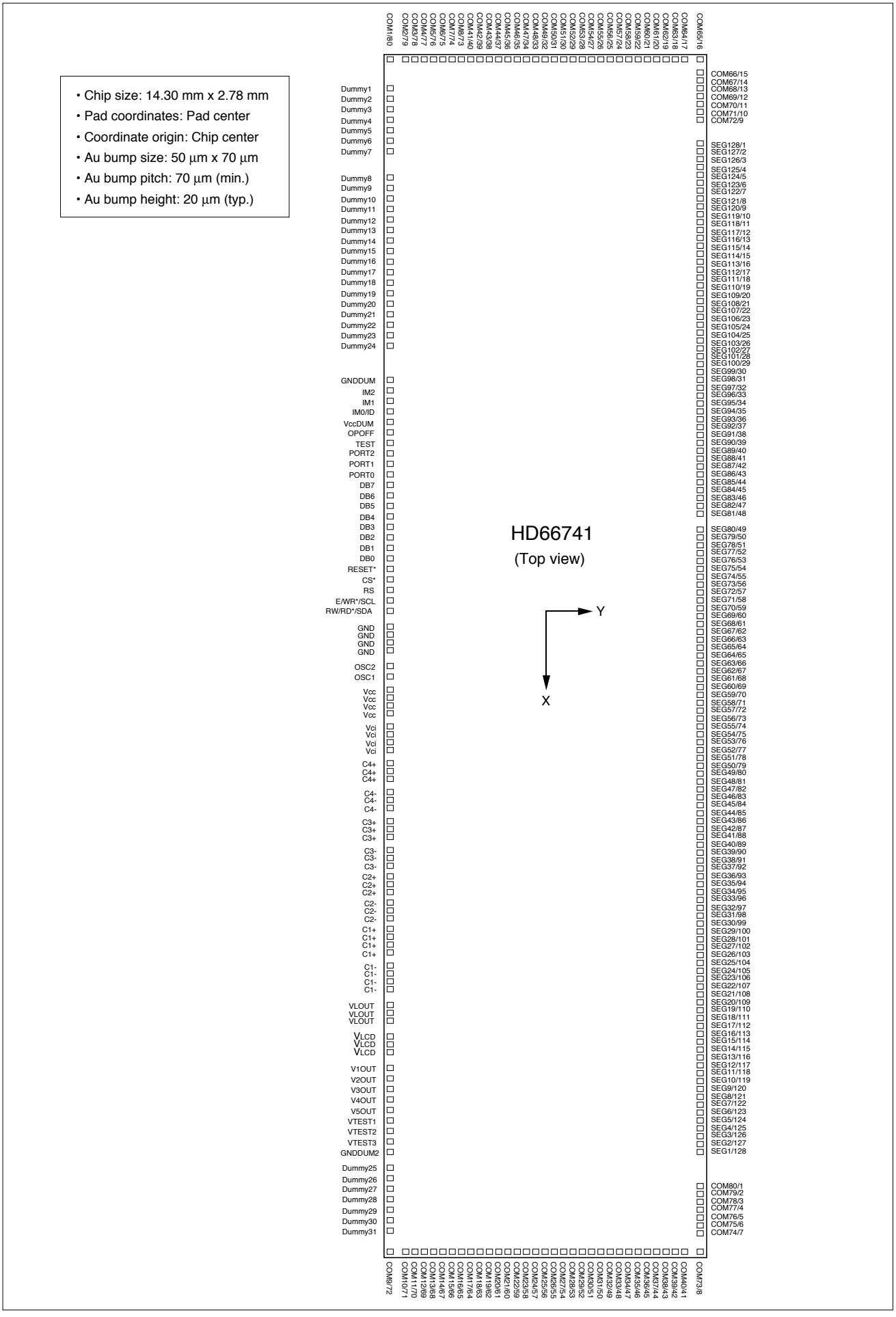
Items	(Under development) HD66728	(Under development) HD66741
Character display sizes	16 characters x 10 lines	—
Graphic display sizes	112 x 80 dots	128 x 80 dots
Multiplexing icons	—	—
Annunciator	—	—
Key scan control	8 x 4	—
LED control ports	—	—
General output ports	3	3
Operating power voltages	1.8 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	4.5 V to 15 V	4.5 V to 15 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits
Expansion driver control	Impossible	Impossible
Liquid crystal drive duty ratios	1/8, 16, 24, 32, 40, 1/48, 56, 64, 72, 80	1/8, 16, 24, 32, 40, 1/48, 56, 64, 72, 80
Liquid crystal drive biases	1/4 to 1/10	1/4 to 1/10
Liquid crystal drive waveforms	B, C	B, C
Liquid crystal voltage booster	Triple, quadruple, or five-times	Triple, quadruple, or five-times
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated
Horizontal smooth scroll	—	—
Vertical smooth scroll	Line unit	Line unit
Double-height display	Yes	Yes
DDRAM	160 x 8	—
CGROM	20,736	—
CGRAM	1,120 x 8	1,280 x 8
SEGRAM	—	—
No. of CGROM fonts	240 + 192	—
No. of CGRAM fonts	64	—
Font sizes	6 x 8	—
Bit map areas	112 x 80	128 x 80
R-C oscillation resistor/ oscillation frequency	External resistor (70–90 kHz)	External resistor (70–90 kHz)
Reset function	External	External
Low power control	Partial display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Oscillation off Liquid crystal power off
SEG/COM direction switching	SEG, COM	SEG, COM
QFP package	—	—
TQFP package	—	—
TCP package	TCP-243	TCP-254
Bare chip	—	—
Bumped chip	Yes	Yes
No. of pins	243	243
Chip sizes	13.67 x 2.78	14.30 x 2.78
Pad intervals	70 μm	70 μm

HD66741 Block Diagram



HD66741 Pad Arrangement

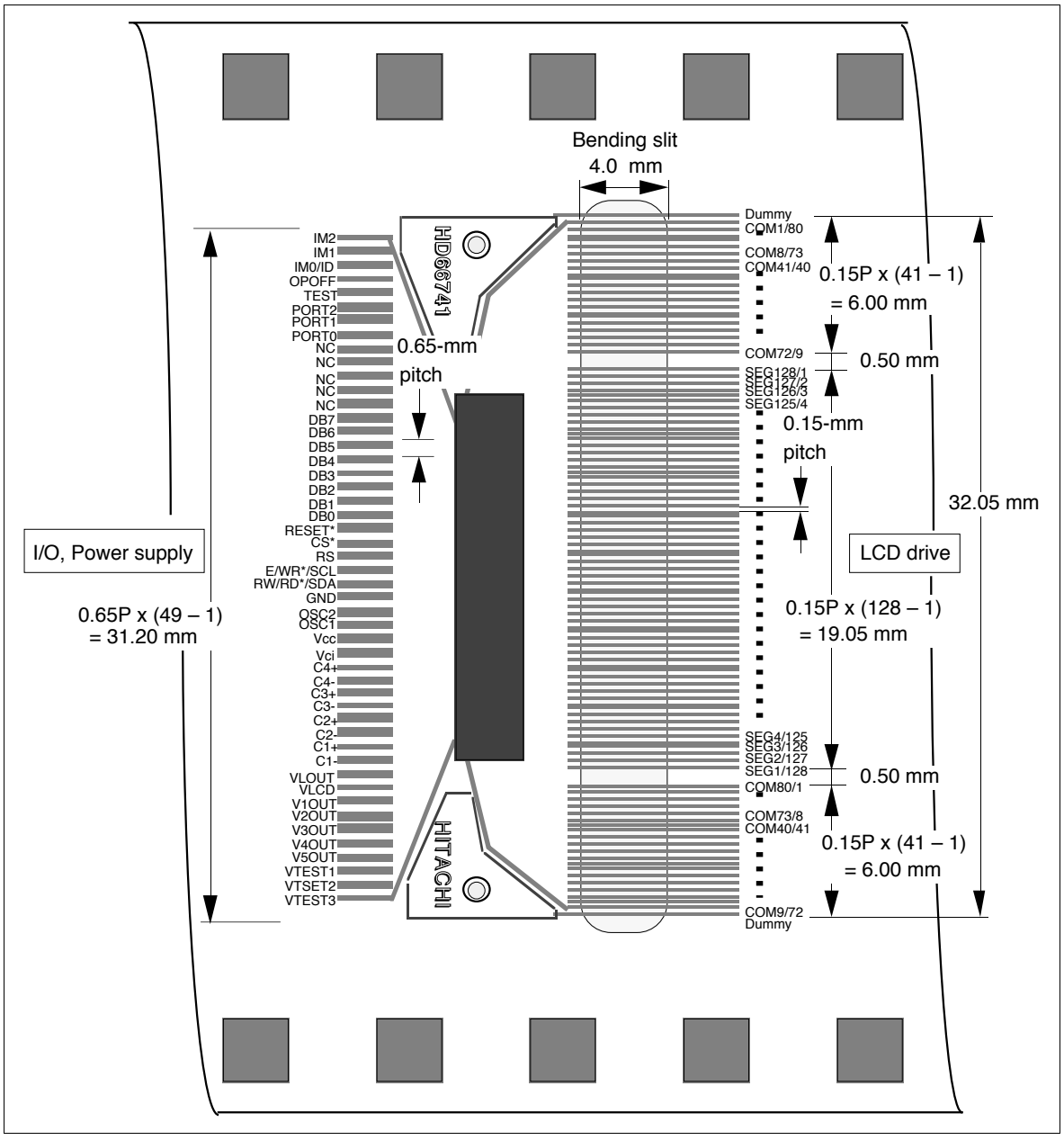
- Chip size: 14.30 mm x 2.78 mm
- Pad coordinates: Pad center
- Coordinate origin: Chip center
- Au bump size: 50 μm x 70 μm
- Au bump pitch: 70 μm (min.)
- Au bump height: 20 μm (typ.)



HD66741 Pad Coordinate

NO.	Pad Name	X	Y	NO.	Pad Name	X	Y	NO.	Pad Name	X	Y	NO.	Pad Name	X	Y
1	COM1/80	-6918	-1224	57	C1+	3404	-1174	130	SEG11/118	4909	1173	210	SEG91/38	-2805	1163
-	Dummy1	-6693	-1224	58	C1+	3504	-1174	131	SEG12/117	4812	1173	211	SEG92/37	-2889	1163
-	Dummy2	-6603	-1224	59	C1+	3604	-1174	132	SEG13/116	4716	1173	212	SEG93/36	-2973	1163
-	Dummy3	-6513	-1224	60	C1+	3704	-1174	133	SEG14/115	4620	1173	213	SEG94/35	-3057	1163
-	Dummy4	-6423	-1224	61	C1-	3834	-1174	134	SEG15/114	4523	1173	214	SEG95/34	-3141	1163
-	Dummy5	-6333	-1224	62	C1-	3934	-1174	135	SEG16/113	4427	1173	215	SEG96/33	-3225	1163
-	Dummy6	-6243	-1224	63	C1-	4034	-1174	136	SEG17/112	4330	1173	216	SEG97/32	-3309	1163
-	Dummy7	-6153	-1224	64	C1-	4134	-1174	137	SEG18/111	4234	1173	217	SEG98/31	-3393	1163
-	Dummy8	-5973	-1224	65	VLOUT	4264	-1174	138	SEG19/110	4137	1173	218	SEG99/30	-3478	1163
-	Dummy9	-5883	-1224	66	VLOUT	4365	-1174	139	SEG20/109	4041	1173	219	SEG100/29	-3562	1163
-	Dummy10	-5793	-1224	67	VLOUT	4465	-1174	140	SEG21/108	3944	1173	220	SEG101/28	-3646	1163
-	Dummy11	-5703	-1224	68	VLCD	4595	-1174	141	SEG22/107	3848	1173	221	SEG102/27	-3730	1163
-	Dummy12	-5613	-1224	69	VLCD	4695	-1174	142	SEG23/106	3751	1173	222	SEG103/26	-3814	1163
-	Dummy13	-5523	-1224	70	VLCD	4795	-1174	143	SEG24/105	3655	1173	223	SEG104/25	-3898	1163
-	Dummy14	-5433	-1224	71	V1OUT	4984	-1137	144	SEG25/104	3558	1173	224	SEG105/24	-3982	1163
-	Dummy15	-5343	-1224	72	V2OUT	5115	-1137	145	SEG26/103	3462	1173	225	SEG106/23	-4066	1163
-	Dummy16	-5253	-1224	73	V3OUT	5245	-1137	146	SEG27/102	3365	1173	226	SEG107/22	-4150	1163
-	Dummy17	-5163	-1224	74	V4OUT	5375	-1137	147	SEG28/101	3269	1173	227	SEG108/21	-4234	1163
-	Dummy18	-5073	-1224	75	V5OUT	5505	-1137	148	SEG29/100	3172	1173	228	SEG109/20	-4318	1163
-	Dummy19	-4983	-1224	76	VTEST1	5635	-1137	149	SEG30/99	3076	1173	229	SEG110/19	-4402	1163
-	Dummy20	-4893	-1224	77	VTEST2	5765	-1137	150	SEG31/98	2979	1173	230	SEG111/18	-4486	1163
-	Dummy21	-4803	-1224	78	VTEST3	5895	-1137	151	SEG32/97	2883	1173	231	SEG112/17	-4570	1163
-	Dummy22	-4713	-1224	79	GNDDUM2	6063	-1224	152	SEG33/96	2786	1173	232	SEG113/16	-4654	1163
-	Dummy23	-4623	-1224	-	Dummy25	6153	-1224	153	SEG34/95	2690	1173	233	SEG114/15	-4738	1163
-	Dummy24	-4533	-1224	-	Dummy26	6243	-1224	154	SEG35/94	2593	1173	234	SEG115/14	-4822	1163
2	GNDDUM	-4432	-1224	-	Dummy27	6333	-1224	155	SEG36/93	2497	1173	235	SEG116/13	-4907	1163
3	IM2	-4332	-1224	-	Dummy28	6423	-1224	156	SEG37/92	2400	1173	236	SEG117/12	-4991	1163
4	IM1	-4148	-1224	-	Dummy29	6513	-1224	157	SEG38/91	2304	1173	237	SEG118/11	-5075	1163
5	IM0/ID	-3972	-1224	-	Dummy30	6603	-1224	158	SEG39/90	2208	1173	238	SEG119/10	-5159	1163
6	VccDUM	-3872	-1224	-	Dummy31	6693	-1224	159	SEG40/89	2111	1173	239	SEG120/9	-5243	1163
7	OPOFF	-3772	-1224	80	COM9/72	6918	-1224	160	SEG41/88	2015	1173	240	SEG121/8	-5327	1163
8	TEST	-3596	-1224	81	COM10/71	6918	-1040	161	SEG42/87	1918	1173	241	SEG122/7	-5411	1163
9	PORT2	-3412	-1224	82	COM11/70	6918	-970	162	SEG43/86	1822	1173	242	SEG123/6	-5495	1163
10	PORT1	-3228	-1224	83	COM12/69	6918	-900	163	SEG44/85	1725	1173	243	SEG124/5	-5579	1163
11	PORT0	-3044	-1224	84	COM13/68	6918	-830	164	SEG45/84	1629	1173	244	SEG125/4	-5663	1163
12	DB7	-2860	-1224	85	COM14/67	6918	-760	165	SEG46/83	1532	1173	245	SEG126/3	-5747	1163
13	DB6	-2677	-1224	86	COM15/66	6918	-690	166	SEG47/82	1436	1173	246	SEG127/2	-5831	1163
14	DB5	-2493	-1224	87	COM16/65	6918	-620	167	SEG48/81	1339	1173	247	SEG128/1	-5915	1163
15	DB4	-2309	-1224	88	COM17/64	6918	-550	168	SEG49/80	1243	1173	248	COM72/9	-6171	1153
16	DB3	-2125	-1224	89	COM18/63	6918	-480	169	SEG50/79	1146	1173	249	COM71/10	-6251	1153
17	DB2	-1941	-1224	90	COM19/62	6918	-410	170	SEG51/78	1050	1173	250	COM70/11	-6330	1153
18	DB1	-1757	-1224	91	COM20/61	6918	-340	171	SEG52/77	953	1173	251	COM69/12	-6410	1153
19	DB0	-1573	-1224	92	COM21/60	6918	-270	172	SEG53/76	857	1173	252	COM68/13	-6490	1153
20	RESET*	-1389	-1224	93	COM22/59	6918	-200	173	SEG54/75	760	1173	253	COM67/14	-6569	1153
21	CS*	-1205	-1224	94	COM23/58	6918	-130	174	SEG55/74	664	1173	254	COM66/15	-6649	1153
22	RS	-1021	-1224	95	COM24/57	6918	-60	175	SEG56/73	567	1173	255	COM65/16	-6918	1224
23	E/WR*/SCL	-858	-1224	96	COM25/56	6918	10	176	SEG57/72	471	1173	256	COM64/17	-6918	1060
24	RW/RD*/SDA	-728	-1224	97	COM26/55	6918	80	177	SEG58/71	374	1173	257	COM63/18	-6918	990
25	GND	-545	-1224	98	COM27/54	6918	150	178	SEG59/70	278	1173	258	COM62/19	-6918	920
26	GND	-415	-1224	99	COM28/53	6918	220	179	SEG60/69	181	1173	259	COM61/20	-6918	850
27	GND	-285	-1224	100	COM29/52	6918	290	180	SEG61/68	85	1173	260	COM60/21	-6918	780
28	GND	-155	-1224	101	COM30/51	6918	360	181	SEG62/67	-12	1173	261	COM59/22	-6918	710
29	OSC2	27	-1224	102	COM31/50	6918	430	182	SEG63/66	-108	1173	262	COM58/23	-6918	640
30	OSC1	211	-1224	103	COM32/49	6918	500	183	SEG64/65	-204	1173	263	COM57/24	-6918	570
31	Vcc	391	-1167	104	COM33/48	6918	570	184	SEG65/64	-301	1173	264	COM56/25	-6918	500
32	Vcc	522	-1167	105	COM34/47	6918	640	185	SEG66/63	-397	1173	265	COM55/26	-6918	430
33	Vcc	652	-1167	106	COM35/46	6918	710	186	SEG67/62	-494	1173	266	COM54/27	-6918	360
34	Vcc	782	-1167	107	COM36/45	6918	780	187	SEG68/61	-590	1173	267	COM53/28	-6918	290
35	Vci	992	-1174	108	COM37/44	6918	850	188	SEG69/60	-687	1173	268	COM52/29	-6918	220
36	Vci	1092	-1174	109	COM38/43	6918	920	189	SEG70/59	-783	1173	269	COM51/30	-6918	150
37	Vci	1192	-1174	110	COM39/42	6918	990	190	SEG71/58	-880	1173	270	COM50/31	-6918	80
38	Vci	1292	-1174	111	COM40/41	6918	1060	191	SEG72/57	-976	1173	271	COM49/32	-6918	10
39	C4+	1422	-1174	112	COM73/8	6918	1224	192	SEG73/56	-1073	1173	272	COM48/33	-6918	-60
40	C4+	1522	-1174	113	COM74/7	6649	1153	193	SEG74/55	-1169	1173	273	COM47/34	-6918	-130
41	C4+	1622	-1174	114	COM75/6	6569	1153	194	SEG75/54	-1266	1173	274	COM46/35	-6918	-200
42	C4-	1752	-1174	115	COM76/5	6490	1153	195	SEG76/53	-1362	1173	275	COM45/36	-6918	-270
43	C4-	1852	-1174	116	COM77/4	6410	1153	196	SEG77/52	-1459	1173	276	COM44/37	-6918	-340
44	C4-	1952	-1174	117	COM78/3	6330	1153	197	SEG78/51	-1555	1173	277	COM43/38	-6918	-410
45	C3+	2083	-1174	118	COM79/2	6251	1153	198	SEG79/50	-1652	1173	278	COM42/39	-6918	-480
46	C3+	2183	-1174	119	COM80/1	6171	1153	199	SEG80/49	-1748	1173	279	COM41/40	-6918	-550
47	C3+	2283	-1174	120	SEG1/128	5874	1173	200	SEG81/48	-1964	1163	280	COM8/73	-6918	-620
48	C3-	2413	-1174	121	SEG2/127	5777	1173	201	SEG82/47	-2048	1163	281	COM7/74	-6918	-690
49	C3-	2513	-1174	122	SEG3/126	5681	1173	202	SEG83/46	-2133	1163	282	COM6/75	-6918	-760
50	C3-	2613	-1174	123	SEG4/125	5584	1173	203	SEG84/45	-2217	1163	283	COM5/76	-6918	-830
51	C2+	2743	-1174	124	SEG5/124	5488	1173	204	SEG85/44	-2301	1163	284	COM4/77	-6918	-900
52	C2+	2843	-1174	125	SEG6/123	5391	1173	205	SEG86/43	-2385	1163	285	COM3/78	-6918	-970
53	C2+	2943	-1174	126	SEG7/122	5295	1173	206	SEG87/42	-2469	1163	286	COM2/79	-6918	-1040
54	C2-	3073	-1174	127	SEG8/121	5198	1173	207	SEG88/41	-2553	1163				
55	C2-	3173	-1174	128	SEG9/120	5102	1173	208	SEG89/40	-2637	1163				
56	C2-	3274	-1174	129	SEG10/119	5005	1173	209	SEG90/39	-2721	1163				

TCP Dimensions (HD66741TB0)



Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2, IM1	2	I	GND or V_{CC}	Selects the MPU interface mode: IM2 "GND" IM1 "GND" MPU interface mode: Clock-synchronized serial interface IM2 "GND" IM1 "Vcc" MPU interface mode: 68-system parallel bus interface IM2 "Vcc" IM1 "GND" MPU interface mode: Setting inhibited IM2 "Vcc" IM1 "Vcc" MPU interface mode: 80-system parallel bus interface
IM0/ID	1	I	GND or V_{CC}	Selects the transfer bus length for a parallel bus interface. GND: 8-bit bus, Vcc: 4-bit bus Inputs the ID of the device ID code for a serial bus interface.
CS*	1	I	MPU	Selects the HD66741: Low: HD66741 is selected and can be accessed High: HD66741 is not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	1	I	MPU	Selects the register for a parallel bus interface. Low: Instruction High: RAM access Selects the key scan interrupt method in the standby period for a serial interface. Fix this pin to the Vcc or GND level for a serial interface.
E/WR*/SCL	1	I	MPU	For an 80-system parallel bus interface, serves as a write strobe signal and writes data at the low level. For a 68-system parallel bus interface, serves as an enable signal to activate data read/write operation. Inputs the serial transfer clock for a serial interface. Fetches data at the rising edge of a clock.
RW/RD*/ SDA	1	I or I/O	MPU	For an 80-system parallel bus interface, serves as a write strobe signal and reads data at the low level. For a 68-system parallel bus interface, serves as a signal to select data read/write operation. Low: Write High: Read Serves as the bidirectional serial transfer data for a serial interface. Sends/Receives data.
DB0–DB7	8	I/O	MPU	Serves as a bidirectional data bus for a parallel bus interface. For a 4-bit bus, data transfer uses DB7-DB4; fix unused DB3-DB0 to the Vcc or GND level. Fix all pins to the Vcc or GND level for a serial interface.
PORT0–PORT2	3	O	General output	General output ports. These ports cannot drive current such as for LEDs or backlighting control. Boost the current using an external transistor.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
COM1/80–COM80/1	80	O	LCD	Output signals for common drive: COM1 to COM8 for the first line, COM9 to COM16 for the second line, COM17 to COM24 for the third line, COM25 to COM32 for the fourth line, and COM73 to COM80 for the 10th line. All the unused pins output unselected waveforms. In the display-off period (D = 0), sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/80 is COM1. If CMS = 1, COM1/80 is COM80. Note that the start position of the common output (the first line) is shifted by CN1–CN0 bits.
SEG1/128–SEG128/1	128	O	LCD	Output signals for segment drive. In the display-off period (D = 0), sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/128 is SEG1. If SGS = 1, SEG1/128 is SEG128.
V1OUT–V5OUT	5	I or O	Open or external bleeder-resistor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins externally.
V_{LCD}	3	—	Power supply	Power supply for LCD drive. V_{LCD} – GND = 15 V max.
V_{CC}, GND	8	—	Power supply	V_{CC}: +1.8 V to +5.5 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For external clock supply, insert the dumping resistance (about 600 Ω) and input clock pulses to OSC1.
Vci	5	I	Power supply	Inputs a reference voltage and supplies power to the booster; generates the liquid crystal display drive voltage from the operating voltage. The boosting output voltage must not be larger than the absolute maximum ratings. Must be left disconnected when the booster is not used.
VLOUT	3	O	V_{LCD} pin/booster capacitance	Potential difference between Vci and GND is triple- to five-times-boosted and then output. Magnitude of boost is selected by instruction.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
C1+, C1–	8	—	Booster capacitance	External capacitance should be connected here for boosting.
C2+, C2–	6	—	Booster capacitance	External capacitance should be connected here when using the triple or more booster.
C3+, C3–	6	—	Booster capacitance	External capacitance should be connected here when using the quadruple and five-times booster.
C4+, C4–	6	—	Booster capacitance	External capacitance should be connected here when using the five-times booster.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low.
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{CC}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
VccDUM	1	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM	1	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy	5	—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST1	1	I	GND or V_{CC}	Adjusts the driving capability of the internal operational amplifier for the LCD. This signal enters the normal drive mode in the GND side, and it enters the high-power drive mode in the V_{CC} side. When the display quality is not sufficient, use the high-power drive mode even though the power-consumption current is large.
VTEST2	1	—	—	Test pin. Must be left disconnected.
VTEST3	1	I	V_{CC} or GND	Adjusts the driving capability of the internal operational amplifier for the LCD. This signal enters the normal drive mode or high-power mode in the GND side according to the VTEST1 pin setting, and it enters the low-power drive mode in the V_{CC} side. Use this signal in the low-power mode so that the display quality is not lowered.

Block Function Description

System Interface

The HD66741 has five types of system interfaces, and a clock-synchronized serial, a 68-system 4-bit/8-bit bus, and a 80-system 4-bit/8-bit bus. The interface mode is selected by the IM2-0 pins.

The HD66741 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display control, and address information for the graphic RAM (CGRAM).

The DR temporarily stores data to be written into or read from the CGRAM. Data written into the DR from the MPU is automatically written into the CGRAM by internal operation. When address information is written into the IR, data is read and then stored in the DR from the CGRAM by internal operation. Data is read through the DR when reading from the RAM, and the first read data is invalid and the second and the following data are normal. After reading, data in the CGRAM at the next address is sent to the DR for the next reading from the MPU.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 3 Register Selection by RS and R/W Bits

R/W Bits	RS Bits	Operations
0	0	Write instructions to IR
1	0	Disabled
0	1	DR write as an internal operation (DR to CGRAM)
1	1	DR read as an internal operation (CGRAM to DR)

General Output Ports (PORT0 to PORT 2)

The HD66741 has three general output ports. These ports control drive current such as that for LEDs or backlighting by using the current boosted by an external transistor.

Address Counter (AC)

The address counter (AC) assigns addresses to the CGRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the CGRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the RDM bit automatically updates or does not update the AC.

Graphic RAM (CGRAM)

The graphic RAM (CGRAM) stores bit-pattern data of 128 x 80 dots. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the CGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another.

Oscillation Circuit (OSC)

The HD66741 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 80 common signal drivers (COM1 to COM80) and 128 segment signal drivers (SEG1 to SEG128). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Display pattern data is sent serially through a 128-bit shift register and latched when all needed data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs. The shift direction of 128-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Booster (DC-DC Converter)

The booster generates triple, quadruple, or five-times voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Boost output level from triple to five-times boost can be selected by software. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/4 bias to 1/10 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 64 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

CGRAM Address Map

Table 4 Relationship between Display Position and CGRAM Address (1)

Segment Driver		SEG1/128	SEG2/127	SEG3/126	SEG4/125	SEG5/124	SEG6/123	SEG7/122	SEG8/121	SEG9/120	SEG10/119	SEG11/118	SEG12/117	SEG13/116	SEG14/115	SEG15/114	SEG16/113	SEG17/112	•••	SEG123/5	SEG124/4	SEG126/3	SEG127/2	SEG128/1	Segment / Common
Address	SGS="0"	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	•••	07B	07C	07D	07E	07F	(HEX)
	SGS="1"	07F	07E	07D	07C	07B	07A	079	078	077	076	075	074	073	072	071	070	06F	•••	004	003	002	001	000	
	DB0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	•••	0	0	1	0	0	COM1
	DB1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	•••	0	1	1	0	0	COM2
	DB2	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	•••	0	0	1	0	0	COM3
	DB3	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	•••	0	0	1	0	0	COM4
	DB4	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	•••	0	0	1	0	0	COM5
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	•••	0	0	1	0	0	COM6
	DB6	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	•••	0	1	1	1	0	COM7
	DB7	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	•••	0	0	0	0	0	COM8
Address	SGS="0"	080	081	082	083	084	085	086	087	088	089	08A	08B	08C	08D	08E	08F	090	•••	0FB	0FC	0FD	0FE	0FF	(HEX)
	SGS="1"	0FF	0FE	0FD	0FC	0FB	0FA	0F9	0F8	0F7	0F6	0F5	0F4	0F3	0F2	0F1	0F0	0EF	•••	084	083	082	081	080	
	DB0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	•••	0	1	1	1	0	COM9
	DB1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	•••	1	0	0	0	1	COM10
	DB2	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	•••	0	0	0	0	1	COM11
	DB3	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	•••	0	0	0	1	0	COM12
	DB4	0	0	0	0	1		0	0	1	0	0	0	1	0	0	0	0	•••	0	0	1	0	0	COM13
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	•••	0	1	0	0	0	COM14
	DB6	0	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	•••	1	1	1	1	1	COM15
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	•••	0	0	0	0	0	COM16
Address	SGS="0"	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	•••	17B	17C	17D	17E	17F	(HEX)
	SGS="1"	17F	17E	17D	17C	17B	17A	179	178	177	176	175	174	173	172	171	170	16F	•••	104	103	102	101	100	
	DB0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	•••	1	1	1	1	1	COM17
	DB1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	•••	0	0	0	1	0	COM18
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	•••	0	0	0	0	0	COM24
Address	SGS="0"	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	180	•••	1FB	1FC	1FD	1FE	1FF	(HEX)
	SGS="1"	1FF	1FE	1FD	1FC	1FB	1FA	1F9	1F8	1F7	1F6	1F5	1F4	1F3	1F2	1F1	1F0	1EF	•••	184	183	182	181	180	
	DB0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	•••	0	0	0	1	0	COM25
	DB1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	•••	0	0	1	1	0	COM26
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	•••	0	0	0	0	0	COM32
Address	SGS="0"	200	201	202	203	204	205	206	207	208	209	20A	20B	20C	20D	20E	20F	210	•••	27B	27C	27D	27E	27F	(HEX)
	SGS="1"	27F	27E	27D	27C	27B	27A	279	278	277	276	275	274	273	272	271	270	26F	•••	204	203	202	201	200	
	DB0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	•••	0	0	0	1	0	COM33
	DB1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	•••	0	0	1	1	0	COM34
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	•••	0	0	0	0	0	COM40

Note: A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Table 5 Relationship between Display Position and CGRAM Address (2)

Segment Driver		SEG1/128	SEG2/127	SEG3/126	SEG4/125	SEG5/124	SEG6/123	SEG7/122	SEG8/121	SEG9/120	SEG10/119	SEG11/118	SEG12/117	SEG13/116	SEG14/115	SEG15/114	SEG16/113	SEG17/112	...	SEG124/5	SEG125/4	SEG126/3	SEG127/2	SEG128/1	Segment / Common
Address	SGS="0"	280	281	282	283	284	285	286	287	288	289	28A	28B	28C	28D	28E	28F	290	•••	2FB	2FC	2FD	2FE	2FF	(HEX)
	SGS="1"	2FF	2FE	2FD	2FC	2FB	2FA	2F9	2F8	2F7	2F6	2F5	2F4	2F3	2F2	2F1	2F0	2EF	•••	284	283	282	281	280	
	DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1		•••	1	1	1	1	1	COM41
	DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	•••	0	0	0	1	0	COM42
	DB2	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	0	0	•••	0	1	1	0	0	COM43
	DB3	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	0	•••	0	0	0	1	0	COM44
	DB4	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	•••	0	0	0	0	1	COM45
	DB5	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	1	1	•••	1	0	0	0	1	COM46
	DB6	0	0	1	1	1	1	1	0	0	0	1	1	1	0	1	1	1	•••	0	1	1	1	0	COM47
	DB7	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	•••	0	0	0	0	0	COM48
Address	SGS="0"	300	301	302	303	304	305	306	307	308	309	30A	30B	30C	30D	30E	30F	310	•••	37B	37C	37D	37E	37F	(HEX)
	SGS="1"	37F	37E	37D	37C	37B	37A	379	378	377	376	375	374	373	372	371	370	36F	•••	304	303	302	301	300	
	DB0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	•••	1	1	1	1	1	COM49
	DB1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	•••	1	0	0	0	0	COM50
	DB2	0	0	1	1	1	1	1	0	0	0	0	0	1	0	1	0	0	•••	1	1	1	1	0	COM51
	DB3	0	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1	0	•••	0	0	0	0	1	COM52
	DB4	0	0	1	1	1	1	1	0	0	0	1	1	1	0	1	1	1	•••	0	0	0	0	1	COM53
	DB5	0	0	0	1	1	1	0	0	0	0	1	1	0	0	0	1	1	•••	1	0	0	0	1	COM54
	DB6	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1	1	1	•••	0	1	1	1	0	COM55
	DB7	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	•••	0	0	0	0	0	COM56
Address	SGS="0"	380	381	382	383	384	385	386	387	388	389	38A	38B	38C	38D	38E	38F	390	•••	3FB	3FC	3FD	3FE	3FF	(HEX)
	SGS="1"	3FF	3FE	3FD	3FC	3FB	3FA	3F9	3F8	3F7	3F6	3F5	3F4	3F3	3F2	3F1	3F0	3EF	•••	384	383	382	381	380	
	DB0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	•••	0	0	1	0	0	COM57
	DB1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	•••	0	1	1	0	0	COM58
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1	1	0	•••	0	0	0	0	0	COM64
Address	SGS="0"	400	401	402	403	404	405	406	407	408	409	40A	40B	40C	40D	40E	40F	410	•••	47B	47C	47D	47E	47F	(HEX)
	SGS="1"	47F	47E	47D	47C	47B	47A	479	478	477	476	475	474	473	472	471	470	46F	•••	404	403	402	401	400	
	DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1	0	•••	0	1	1	1	0	COM65
	DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	•••	1	0	0	0	1	COM66
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	•••	0	0	0	0	0	COM72
Address	SGS="0"	480	481	482	483	484	485	486	487	488	489	48A	48B	48C	48D	48E	48F	490	•••	4FB	4FC	4FD	4FE	4FF	(HEX)
	SGS="1"	4FF	4FE	4FD	4FC	4FB	4FA	4F9	4F8	4F7	4F6	4F5	4F4	4F3	4F2	4F1	4F0	4EF	•••	484	483	482	481	480	
	DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1	0	•••	0	1	1	1	0	COM73
	DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	•••	1	0	0	0	1	COM74
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮
	DB7	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	•••	0	0	0	0	0	COM80

Note: A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66741 can be controlled by the MPU. Before starting internal operation of the HD66741, control information is temporarily stored in these registers to allow interfacing with various peripheral control devices or MPUs which operate at different speeds. The internal operation of the HD66741 is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signal (DB0 to DB7), make up the HD66741 instructions. There are five categories of instructions that:

- Control the display
- Control power management
- Set internal CGRAM addresses
- Transfer data with the internal CGRAM

Normally, instructions that perform data transfer with the internal CGRAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66741 CGRAM addresses after each data write can lighten the MPU program load.

Because instructions are executed in 0 cycle, instructions can be written in succession.

Instruction Descriptions

Start Oscillation

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Figure 2 Start Oscillation Instruction

Driver Output Control

CMS: Selects the output shift direction of a common driver. When CMS = "0", COM1/80 shifts to COM1, and COM80/1 to COM80. When CMS = "1", COM1/80 shifts to COM80, and COM80/1 to COM1. Output position of a common driver shifts depending on the CN1–0 bit setting. For details, see the Display On/Off Control section.

SGS: Selects the output shift direction of a segment driver. When SGS = "0", SEG1/128 shifts to SEG1, and SEG128/1 to SEG128. When SGS = "1", SEG1/128 shifts SEG128, and SEG128/1 to SEG1.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**1**	**CMS**	**SGS**

Figure 3 Driver Output Control Instruction

Power Control

AMP: When AMP = 1, each voltage follower for V1 to V5 pins and the booster are turned on. When AMP = 0, current consumption can be reduced while the display is not being used.

SLP: When SLP = 1, the HD66741 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

a. Power control (AMP, SLP, and STB bits)
b. Port control (PT2-0 bits)

During the sleep mode, the other CGRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66741 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Voltage follower circuit on/off (AMP = 1/0)
c. Start oscillation
d. Port control (PT2-0 bits)

During the standby mode, the CGRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**1**	**AMP**	**SLP**	**STB**

Figure 4 Power Control Instruction

Contrast Control 1/2

SW: Switches the bit configuration for the contrast control instruction.

CT4–CT0: When SW = 0, they control the LCD drive voltage (potential difference between V1 and GND) to adjust contrast. A 64-step adjustment is also possible by using the CT5 bit which are set in the entry mode register. For details, see the Contrast Adjuster section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**0**	**0**	**1**	**0**	**SW**	**CT4**	**CT3**	(SW = 0)
								BT1	**BT0**	(SW = 1)
0	0	**0**	**0**	**0**	**1**	**1**	**CT2**	**CT1**	**CT0**	(SW = 0)
							BS2	**BS1**	**BS0**	(SW = 1)

Figure 5 Contrast-Control 1/2 Instruction

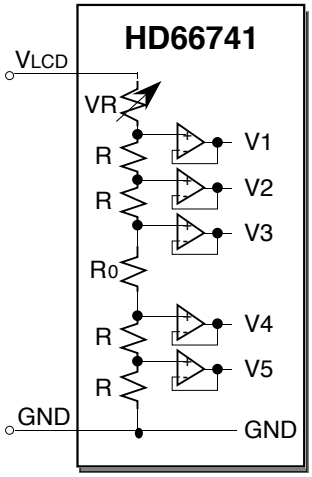


Figure 6 Contrast Adjuster

Table 6 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value						
CT5	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**	**Variable Resistor (VR)**
0	0	0	0	0	0	3.20 x R
0	0	0	0	0	1	3.15 x R
0	0	0	0	1	0	3.10 x R
0	0	0	0	1	1	3.05 x R
0	0	0	1	0	0	3.00 x R
			•			•
			•			•
0	1	1	1	1	1	1.65 x R
1	0	0	0	0	0	1.60 x R
1	0	0	0	0	1	1.55 x R
1	0	0	0	1	0	1.50 x R
			•			•
			•			•
1	1	1	1	0	1	0.15 x R
1	1	1	1	1	0	0.10 x R
1	1	1	1	1	1	0.05 x R

BT1-0: When SW = 1, they switch the output of V5OUT between triple, quadruple, and five-times boost. The liquid crystal display drive voltage level can be selected according to its drive duty ratio and bias. A lower amplification of the booster consumes less current.

BS2-0: When SW = 1, they set the crystal display drive bias value within the range of 1/4 to 1/10 bias. The liquid crystal display drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector section.

Table 7 BT Bits and Output Level

BT1	BT0	V5OUT Output Level
0	0	Triple boost (no boost)
0	1	Quadruple boost
1	0	Five-times boost
1	1	Setting inhibited

Table 8 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	Liquid Crystal Display Drive Bias Value
0	0	0	1/10 bias drive
0	0	1	1/9.5 bias drive
0	1	0	1/9 bias drive
0	1	1	1/8 bias drive
1	0	0	1/7 bias drive
1	0	1	1/6 bias drive
1	1	0	1/5 bias drive
1	1	1	1/4 bias drive

Entry Mode

After power-on reset, ensure the setting. Since the DB0 bit is the test bit, set DB0 when SW = 0, and clear DB0 when SW = 1.

REV: Displays all character and graphics display sections with black-and-white reversal when SW = 0 and REV = 1. For details, see the Reversed Display Function section.

I/D: When SW = 0, increments (I/D = 1) or decrements (I/D = 0) the CGRAM address by 1 when data is written into or read from the CGRAM.

CT5: Sets the most significant bit (CT5) for contrast adjustment when SW = 1. A 64-step adjustment is also possible by using the CT4–CT0 bits which are set in the contrast-control 1/2 instruction.

RDM: When SW = 1 and RDM = 0, the RDM increments or decrements the address counter value according to the I/D bit setting after reading the data from the CGRAM. When RDM = 1, the address counter value is not updated after the data has been read from the CGRAM. The address counter value is used when the RAM data is read, modified, and written. Since the first read data is invalid, the read must be continuously done twice. After writing to the CGRAM, the address counter value must be updated.

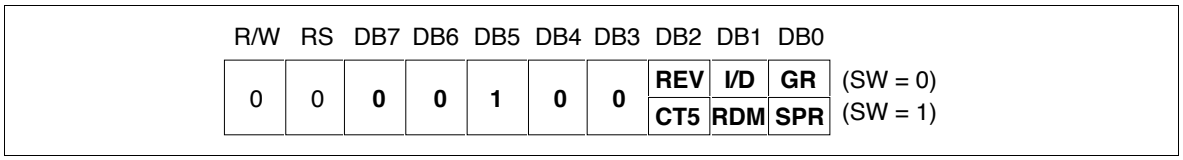


Figure 7 Entry Mode Set Instruction

Display On/Off Control

D: Display is on when SW = 0 and D = 1 and off when D = 0. When off, the display data remains in the CGRAM, and can be displayed instantly by setting D = 1. When D is 0, the display is off with the SEG1 to SEG128 outputs and COM1 to COM80 outputs set to the GND level. Because of this, the HD66741 can control charging current for the LCD with AC driving.

DL10: When SW = 0, DL10 can be set. When DL10 = 1, the 10th line is displayed at double height.

DL9–DL7: When SW = 1, DL9–DL7 can be set. Double-height display is specified for any display line. When DL7 = 1, the seventh line is displayed at double height. Double-height display is used for the eighth line when DL8 = 1 and for the ninth line when DL9 = 1. For double-height display for the first to the sixth lines, control them by using DL1–DL6 bits in the display-line control instruction.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**0**	**1**	**1**	**0**	**D**	**DL10**	**LC**	(SW = 0)
							DL9	**DL8**	**DL7**	(SW = 1)

Figure 8 Display On/Off Control Instruction

Display Line Control

NL3-0: Set NL2–NL0 bits when SW = 0, and the NL3 bit when SW = 1 to specify the display lines. A line consists of 8 dots. Display lines change the liquid crystal display drive duty ratio. CGRAM address mapping does not depend on the number of display lines.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**0**	**1**	**1**	**1**	**NL2**	**NL1**	**NL0**	(SW = 0)
							CN1	**CN0**	**NL3**	(SW = 1)

Figure 9 Display-line Control Instruction

Table 9 NL Bits and Display Lines

NL3	NL2	NL1	NL0	Display Size	LCD Drive Duty	Common Driver Used
0	0	0	0	128 x 8 dots	1/8 Duty	COM1–COM8
0	0	0	1	128 x 16 dots	1/16 Duty	COM1–COM16
0	0	1	0	128 x 24 dots	1/24 Duty	COM1–COM24
0	0	1	1	128 x 32 dots	1/32 Duty	COM1–COM32
0	1	0	0	128 x 40 dots	1/40 Duty	COM1–COM40
0	1	0	1	128 x 48 dots	1/48 Duty	COM1–COM48
0	1	1	0	128 x 56 dots	1/56 Duty	COM1–COM56
0	1	1	1	128 x 64 dots	1/64 Duty	COM1–COM64
1	0	0	0	128 x 72 dots	1/72 Duty	COM1–COM72
1	0	0	1	128 x 80 dots	1/80 Duty	COM1–COM80

CN1–CN0: Set CN1–CN0 bits when SW = 1. When CN1–0 = 01, the display position is shifted by 16 dots (two lines) below and display starts from COM17. When the liquid crystal is driven at low duty in the system wait state, it can display partially at the center of the screen. For details, see the Partial-display-on Function section.

When CN1–CN0 = 10, the display position is shifted by 8 dots (one line) above and second-line display starts from COM1. The 8 dots of the first line are moved to the lowest edge of the display screen. The output position of the lowest edge depends on the drive duty setting. In vertical smooth scrolling, PS1–PS0 bits can selectively fixed-display only the first to the third lines. Combining these functions enables the fixed display of one line of the lowest edge. For details, see the Partial Smooth Scroll Display Function section.

Table 10 Common Driver Pin Function

	Common Driver Pin Function					
	CN 1–0 = 00 (Normal Output)		CN 1–0 = 01 (Center Output)		CN1–0 = 10 (Lowest-edge Output)	
Common Driver Pin	CMS = 0	CMS = 1	CMS = 0	CMS = 1	CMS = 0	CMS = 1
COM1/80	**COM1**	COM80	COM65	COM64	COM9	COM8
COM2/79	COM2	COM79	COM66	COM63	COM10	COM7
⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM7/72	COM7	COM74	COM71	COM58	COM15	COM2
COM8/73	COM8	COM73	COM72	COM57	COM16	**COM1**
COM9/72	COM9	COM72	COM73	COM56	COM17	COM80
COM10/71	COM10	COM71	COM74	COM55	COM18	COM79
⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM15/66	COM15	COM66	COM79	COM50	COM23	COM73
COM16/65	COM16	COM65	COM80	COM49	COM24	COM72
COM17/64	COM17	COM64	**COM1**	COM48	COM25	COM71
COM18/63	COM18	COM63	COM2	COM47	COM26	⋮
⋮	⋮	⋮	⋮	⋮	⋮	COM66
COM24/57	COM24	COM57	COM8	COM41	COM32	COM65
COM25/56	COM25	COM56	COM9	COM40	COM33	COM64
⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM32/49	COM32	COM49	COM16	COM33	COM40	COM57
COM33/48	COM33	COM48	COM17	COM32	COM41	COM56
⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM40/41	COM40	COM41	COM24	COM25	COM48	COM49
COM41/40	COM41	COM40	COM25	COM24	COM49	COM48
⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM48/33	COM48	COM33	COM32	COM17	COM56	COM41
COM49/32	COM49	COM32	COM33	COM16	COM57	COM40
⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM56/25	COM56	COM25	COM40	COM9	COM64	COM33
COM57/24	COM57	COM24	COM41	COM8	COM65	COM32
⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM64/17	COM64	COM17	COM48	**COM1**	COM72	COM25
COM65/16	COM65	COM16	COM49	COM80	COM73	COM24
⋮	⋮	⋮	⋮	⋮	⋮	⋮
COM72/9	COM72	COM9	COM56	COM73	COM80	COM17
COM73/8	COM73	COM8	COM57	COM72	**COM1**	COM16
⋮	⋮	⋮	⋮	⋮	COM2	COM15
COM79/2	COM79	COM2	COM63	COM66	⋮	⋮
COM80/1	COM80	**COM1**	COM64	COM65	COM8	COM9

Double-height Display Control

DL3-1: Can be specified when SW = 0. Specify the double-height display for any line. When DL1 = 1, the first line (8 dots) is displayed as 16 dots at double height. When DL2 = 1, the second line is displayed at double height. When DL3 = 1, the third line is displayed at double height. Double-height display of multiple lines is possible. For details, see the Double-height Display section.

DL6-4: Can be specified when SW = 1. Specify the double-height display for any line. When DL4 = 1, the fourth line (8 dots) is displayed at double height. When DL5 = 1, the fifth line is displayed at double height. When DL6 = 1, the sixth line is displayed at double height. For the seventh to 10th lines, control double-height display by using the DL7–DL10 bits in the display-line control instruction.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**0**	**0**	**0**	**DL3** **DL6**	**DL2** **DL5**	**DL1** **DL4**

Figure 10 Double-height Display Control Instruction

Vertical Scroll Control 1/2

SN3-0: Set SN2 to SN0 bits when SW = 0. Set the SN3 bit when SW = 1. Specify the display start line output from COM1. Because the CGRAM is assigned a 10-line display area in which a line consists of 8 dots, the data is displayed sequentially from the first line to the 10th line then repeated from the first line again. In partial smooth scrolling, these bits specify the display start line for the next line of the fixed-display line. For details, see the Partial Smooth Scroll Display Function section.

SL2–0: Select the top raster-row to be displayed (display-start raster-row) in the display-start line specified by SN2 to SN0. Any raster-row from the first to eighth can be selected (table 19). This function is used to achieve vertical smooth scrolling together with SN2 to SN0. For details, see the Vertical Smooth Scroll section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**1**	**0**	**0**	**1**	**SN2**	**SN1**	**SN0**	(SW = 0)
							<0>	**<0>**	**SN3**	(SW = 1)
0	0	**0**	**1**	**0**	**1**	**0**	**SL2**	**SL1**	**SL0**	(SW = 0)
							<0>	**PS1**	**PS0**	(SW = 1)

Figure 11 Vertical Scroll Control 1/2 Instruction

Table 11 SN Bits and Display-start Lines

SN3	SN2	SN1	SN0	Display-start Line
0	0	0	0	1st line
0	0	0	1	2nd line
0	0	1	0	3rd line
0	0	1	1	4th line
0	1	0	0	5th line
0	1	0	1	6th line
0	1	1	0	7th line
0	1	1	1	8th line
1	0	0	0	9th line
1	0	0	1	10th line

Table 12 SL Bits and Display-start Raster-row

SL2	SL1	SL0	Display-start Raster-row
0	0	0	1st raster-row
0	0	1	2nd raster-row
0	1	0	3rd raster-row
0	1	1	4th raster-row
1	0	0	5th raster-row
1	0	1	6th raster-row
1	1	0	7th raster-row
1	1	1	8th raster-row

PS1–0: Specify PS1 to PS0 bits when SW = 1. When PS1–0 = 01, only the first line is fixed-displayed in vertical smooth scrolling, and the other display lines are smooth-scrolled. When PS1–0 = 10, the first and second lines are fixed-displayed. When PS1–0 = 11, the first to third lines are fixed-displayed. For details, see the Partial Smooth Scroll Display Function section.

Port Control

PT2-0: Control the output level of a port output pin (PORT2-PORT0). When PT0 = 0, the PORT0 pin outputs the GND level, and when PT0 = 1, it outputs the VCC level. Similarly, PT1 and PT2 bits control PORT1 and PORT2 output levels respectively.

B/C: When SW = 1 and B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD driving. When B/C = 1, a C-pattern waveform is generated and alternates (n-raster-row reversed AC drive) in each raster-row specified by bits EOR and NW4–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

DCC: When SW = 1 and DCC = 0, a booster operates with the 64-divided clock of the operating frequency. When DCC = 1, the booster operates with the 32-divided clock. When the booster operates with the 64-divided clock, current consumption in the booster is low, but boosting ability is weak.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**1**	**1**	**1**	**0**	**PT2**	**PT1**	**PT0**	(SW = 0)
							<0>	**DCC**	**B/C**	(SW = 1)

Figure 12 Port Control Instruction

LCD-Driving-Waveform Control

EOR: When the C-pattern waveform is set (B/C = 1) and SW = 1 and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the LCD drive duty ratio and n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW4–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW4–NW0 alternate in every set value + 1 raster-row, and the first to the 32nd raster-rows can be selected. When SW = 0, bits NW2, NW1, and NW0 can be set. When SW = 1, bits NW4 and NW3 can be set.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**1**	**1**	**1**	**1**	**NW2**	**NW1**	**NW0**	(SW = 0)
							EOR	**NW4**	**NW3**	(SW = 1)

Figure 13 LCD-Driving-Waveform Control Instruction

RAM Address Set

AD10-0: Initially set CGRAM addresses to the address counter (AC). Once the CGRAM data is written, the AC is automatically updated according to the I/D bit. This allows consecutive accesses without resetting addresses. Once the CGRAM data is read, the AC is automatically updated according to the I/D bit when RDM = 0, and not updated when RDM = 1. Set RDM to 1 when read, modify, and write are done in every one-byte data. CGRAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**1**	**0**	**1**	**AD10**	**AD9**	**AD8**	**AD7**	**AD6**
0	0	**1**	**1**	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**

Figure 14 RAM Address Set Instruction

Table 13 AD Bits and CGRAM Settings

RM	AD10–AD0	CGRAM Setting
1	"000"H–"07F"H	Bit map data for COM1 to COM8
1	"080"H–"0FF"H	Bit map data for COM9 to COM16
1	"100"H–"17F"H	Bit map data for COM17 to COM24
1	"180"H–"1FF"H	Bit map data for COM25 to COM32
1	"200"H–"27F"H	Bit map data for COM33 to COM40
1	"280"H–"2FF"H	Bit map data for COM41 to COM48
1	"300"H–"37F"H	Bit map data for COM49 to COM56
1	"380"H–"3FF"H	Bit map data for COM57 to COM64
1	"400"H–"47F"H	Bit map data for COM65 to COM72
1	"480"H–"4FF"H	Bit map data for COM73 to COM80

Write Data to CGRAM

WD7-0 : Write 8-bit data to the CGRAM. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting. During the sleep and standby modes, the CGRAM cannot be accessed.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	**WD7**	**WD6**	**WD5**	**WD4**	**WD3**	**WD2**	**WD1**	**WD0**

Figure 15 Write Data to CGRAM Instruction

Read Data from CGRAM

RD7-0 : Read 8-bit data from the CGRAM. In the parallel bus interface mode, the first-byte data read will be invalid immediately after the CGRAM address set, and the consecutive second-byte data will be read normally. In the serial interface mode, two bytes will be invalid immediately after the start byte, and the consecutive third-byte data will be read normally. For details, see the Serial Data Transfer section.

After a CGRAM read, when RDM = 0, the address is automatically incremented or decremented by 1 according to the I/D bit. When RDM = 1, the address is not updated.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	**RD7**	**RD6**	**RD5**	**RD4**	**RD3**	**RD2**	**RD1**	**RD0**

Figure 16 Read Data from CGRAM Instruction

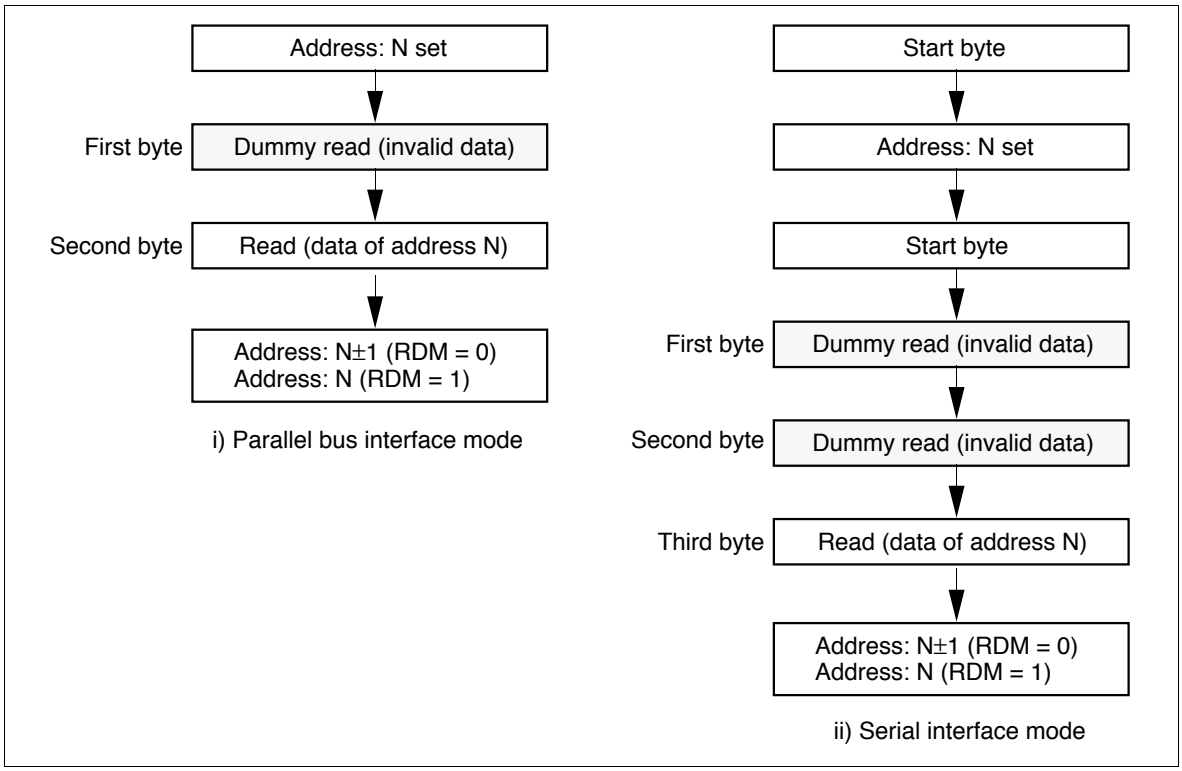


Figure 17 CGRAM Read Sequence

Table 14 Instruction List

Register Name	Code										Description	Execution Cycle
	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Start oscillation	0	0	0	0	0	0	0	0	1	1	Starts the oscillation standby mode.	—
Driver output control	0	0	0	0	0	0	0	1	CMS	SGS	Selects the common driver shift direction (CMS) and segment driver shift direction (SGS).	0
Power control	0	0	0	0	0	0	1	AMP	SLP	STB	Turns on LCD power supply (AMP), and sets the sleep mode (SLP) and standby mode (STB).	0
Contrast control 1	0	0	0	0	0	1	0	SW	CT4	CT3	Sets the register selection (SW) or upper contrast adjustment bits (CT4-3).	0
									BT1	BT0	Sets the register selection (SW) or boost level (BT1/0).	0
Contrast control 2	0	0	0	0	0	1	1	CT2	CT1	CT0	Sets the lower contrast adjustment bits (CT2-0).	0
								BS2	BS1	BS0	Sets the LCD bias value (BS2-0).	0
Entry mode set	0	0	0	0	1	0	0	REV	I/D	1	Sets the black-and-white reversal (REV) or address update direction after RAM access (I/D).	0
								CT5	RDM	0	Sets the higher contrast adjustment bit (CT5) or read, modify, write (RDM).	0
Display on/off control	0	0	0	0	1	1	0	D	DL10	0	Sets display on (D) or double-height display line (DL10).	0
								DL9	DL8	DL7	Specifies double-height display lines (DL9–DL7).	0
Display line control	0	0	0	0	1	1	1	NL2	NL1	NL0	Sets the number of display lines (NL2-0).	0
								CN1	CN0	NL3	Specifies centering (CN1–0) or the number of display lines (NL3).	0
Double-height display control	0	0	0	1	0	0	0	DL3	DL2	DL1	Specifies double-height display lines (DL3-1).	0
								DL6	DL5	DL4	Specifies double-height display lines (DL6–4).	0

Table 14 Instruction List (cont)

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
Vertical scroll control 1	0	0	0	1	0	0	1	SN2	SN1	SN0	Sets the display-start line (SN2-0).	0
								<0>	<0>	SN3	Sets the display-start line (SN3).	0
Vertical scroll control 2	0	0	0	1	0	1	0	SL2	SL1	SL0	Sets the display-start raster-row (SL2-0).	0
								<0>	PS1	PS0	Sets the partial scroll (PS1–0).	0
Port control	0	0	0	1	1	1	0	PT2	PT1	PT0	Sets the general port output (PT2-0).	0
								<0>	DCC	BC	Selects the boosting cycle (DCC) or LCD drive AC waveform (B/C).	0
LCD-driving-waveform control	0	0	0	1	1	1	1	NW2	NW1	NW0	Sets the number of n-raster-rows (NW2–0) in C-pattern AC drive.	0
								EOR	NW4	NW3	Sets the EOR output (EOR) or the number of n-raster-rows (NW4–3) in C-pattern AC drive.	0
RAM address set (upper bits)	0	0	1	0	1			AD10–6 (upper bits)			Initially sets the upper addresses of the CGRAM to the address counter (AC).	0
RAM address set (lower bits)	0	0	1	1				AD5-0 (lower bits)			Initially sets the lower addresses of the CGRAM to the AC.	0
Write data to RAM	0	1				Write data					Writes data to CGRAM.	0
Read data from RAM	1	1				Read data					Reads data from CGRAM.	0

Note: The upper column of each register can be set when SW = 0. The lower column can be set when SW = 1.

Bit definition:

CMS = 0: COM1/80 => COM1

SGS = 0: SEG1/128 => SEG1

AMP = 1: Operational amplifier and booster circuit on

SLP = 1: Sleep mode

STB = 1: Standby mode

SW = 0: Upper register setting

SW = 1: Lower register setting

CT5-0: Contrast adjustment

BT1/0: Boost level selection (00: Triple, 01: Quadruple, 10: Five-times)

BS2-0: LCD drive bias selection

REV = 0: Normal display

REV = 1: Black-and-white reversed display of the graphics display

ID = 1: Address increment

ID = 0: Address decrement

RDM = 1: Read, modify, and write mode (Not automatically update the address counter after reading)

D = 1: Display on

NL3-0: Display line setting (0000: 1/8 duty ratio, 0001: 1/16 duty ratio, 0010: 1/24 duty ratio, 0011: 1/32 duty ratio, 0100: 1/40 duty ratio, 0101: 1/48 duty ratio, 0110: 1/56 duty ratio, 0111: 1/64 duty ratio, 1000: 1/72 duty ratio, 1001: 1/80 duty ratio)

DL1-10: Double-height line specifications (DL1: 1st line, DL2: 2nd line, DL3: 3rd line, DL4: 4th line, DL5: 5th line, DL6: 6th line, DL7: 7th line, DL8: 8th line, DL9: 9th line, DL10: 10th line)

SN3-0: Display-start line (0000: 1st line, 0001: 2nd line, 0010: 3rd line, 0011: 4th line, 0100: 5th line, 0101: 6th line, 0110: 7th line, 0111: 8th line, 1000: 9th line, 1001: 10th line)

SL2-0: Display-start raster-row specifications (000: 1st raster-row...111: 8th raster-row)

CN1–0 Centering specifications (00: no centering, 01: 16-dot shift below, 10: 8-dot shift above)

PT2-0: Port output control (PT2 = 1: PORT2 = Vcc, PT1 = 1: PORT1 = Vcc, PT0 = 1: PORT0 = Vcc)

B/C = 0: B-pattern waveform drive

B/C = 1: C-pattern waveform drive

EOR = 1: EOR alternating drive at C-pattern waveform

NW4–0: Reversed number of n raster-rows at C-pattern waveform drive (alternating with the set value + one raster-row)

DCC = 0: Boosted at 1/64-divided clock

DCC = 1: Boosted at 1/32-divided clock

ADD10-0: CGRAM address set (000H-4FFH)

Reset Function

The HD66741 is internally initialized by RESET input. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period and the 1000-clock cycle period following reset cancellation, no instruction or CGRAM data access from the MPU is accepted. Any initializing instruction must wait for 1,000 clock cycles after the reset is canceled so that execution of the clear display instruction can be completed. The reset input must be held for at least 1 ms.

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (SGS = 0, CMS = 0)
3. Power control (AMP = 0: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
4. Triple boost (BT1/0 = 00), 1/10 bias drive (BS2/1/0 = 000), Weak contrast (CT5-0 = 00000)
5. Entry mode set (REV = 0: Normal display, I/D = 1: Increment by 1, RDM = 0: Automatically update after reading)
6. Display on/off control (D = 0: Display off, CEN = 0: Normal position)
7. Display line control (NL3/2/1/0 = 1001: 1/80 duty ratio)
8. Double-height display off (DL10–1 = 0000000000)
9. Vertical scroll control (SN3/2/1/0 = 0000: First line displayed at the top, SL2/1/0: First raster-row displayed at the top of the first line, PS1/0 = 00: Partial scroll off)
10. Port control (PT2/1/0 = 000: PORT2/1/0 output = GND level)
11. 1/64-divided clock boost (DCC = 0)
12. B-pattern waveform AC drive (B/C = 0, EOR = 0, NW4/3/2/1/0 = 00000)

CGRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Booster output pins (VLOUT): Outputs Vcc level
3. Oscillator output pin (OSC2): Outputs oscillation signal
4. General output ports (PORT0–PORT2): Output GND level

Serial Data Transfer

Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The HD66741 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66741 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66741. The HD66741, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66741 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued, and when RS = 1, data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in table 26.

After receiving the start byte, the HD66741 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. To transfer data consecutively, note that only the display-clear instruction requires a longer execution time than the others (see table 24, Instruction List).

Two bytes of CGRAM read data after the start byte are invalid. The HD66741 starts to read correct CGRAM data from the third byte.

Table 15 Start Byte Format

Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

Table 16 RS and R/W Bit Function

RS	R/W	Function
0	0	Writes instruction
0	1	Invalid
1	0	Writes RAM data
1	1	Reads RAM data

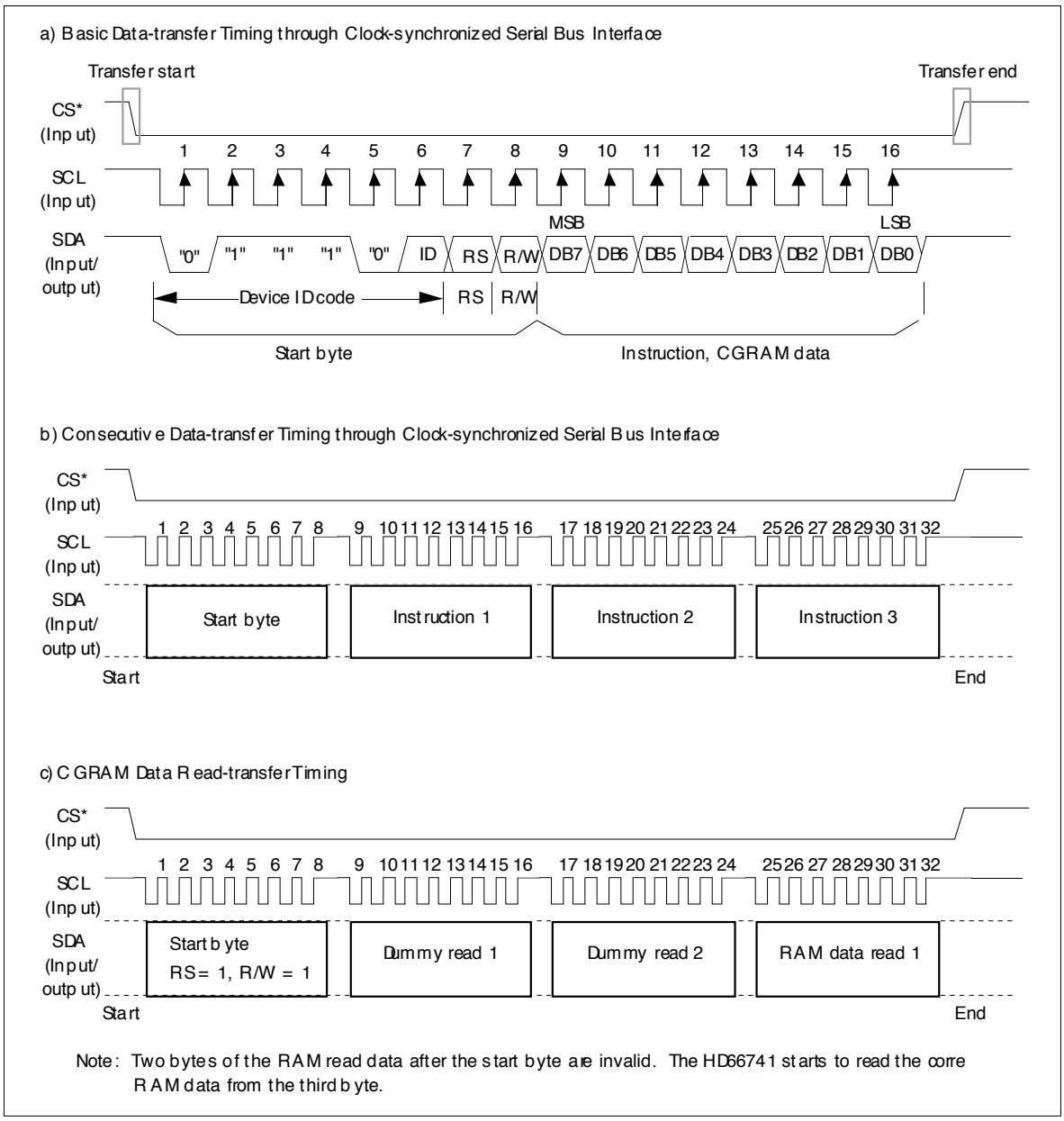


Figure 18 Clock-synchronized Serial Interface Timing Sequence

Parallel Data Transfer

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/Vcc/GND level allows E-clock-synchronized 8-bit parallel data transfer. Setting the IM2/1/0 (interface mode) to the Vcc/Vcc/GND level allows 80-system 8-bit parallel data transfer. When the number of buses or the mounting area is limited, use a 4-bit bus interface or serial data transfer.

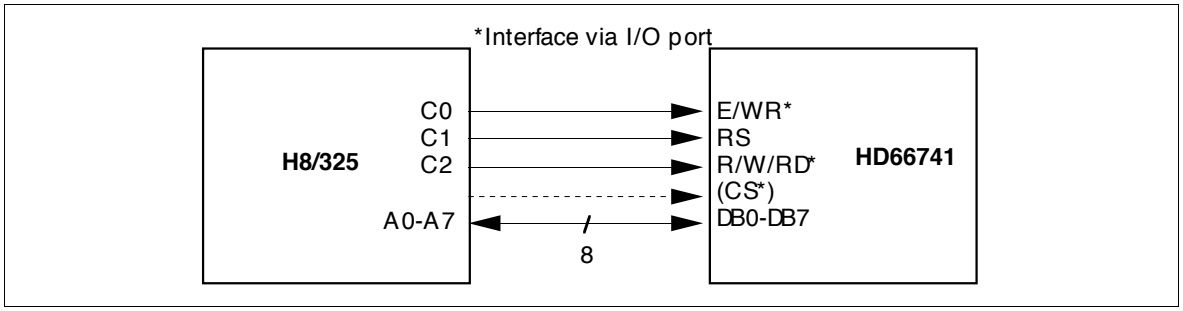


Figure 19 Interface to 8-bit Microcomputer

4-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/Vcc/Vcc level allows E-clock-synchronized 4-bit parallel data transfer using pins DB7-DB4. Setting the IM2/1/0 (interface mode) to the Vcc/Vcc/Vcc level allows 80-system 4-bit parallel data transfer. The 8-bit instructions and RAM data are divided into four upper/lower bits and the transfer starts from the upper four bits.

Note: Transfer synchronization function for a 4-bit bus interface
The HD66741 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 4-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the four upper and lower bits can be corrected by a reset triggered by consecutively writing a 0000 instruction four times. The next transfer starts from the upper four bits. Executing synchronization function periodically can recover any runaway in the display system.
When the 4-bit synchronization function is executed, the blink synchronization is executed simultaneously.

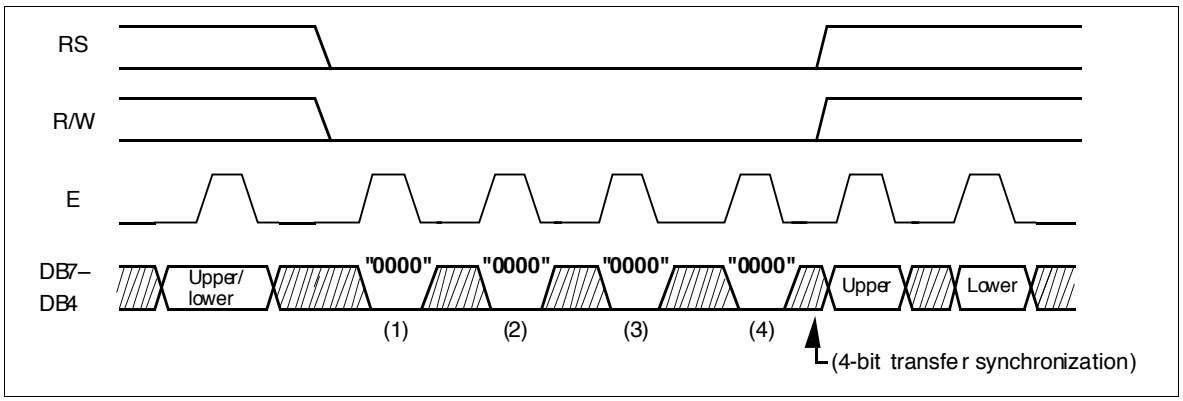


Figure 20 4-bit Transfer Synchronization

Oscillation Circuit

The HD66741 can either be supplied with operating pulses externally (external clock mode) or oscillate using an internal R-C oscillator with an external oscillator-resistor (external resistor oscillation mode). Note that in R-C oscillation, the oscillation frequency is changed according to the internal capacitance value, the external resistance value, or operating power-supply voltage. Insert the dumping resistance of about 2 kΩ to prevent malfunctions caused by over-shoot or under-shoot noise in the external clock mode.

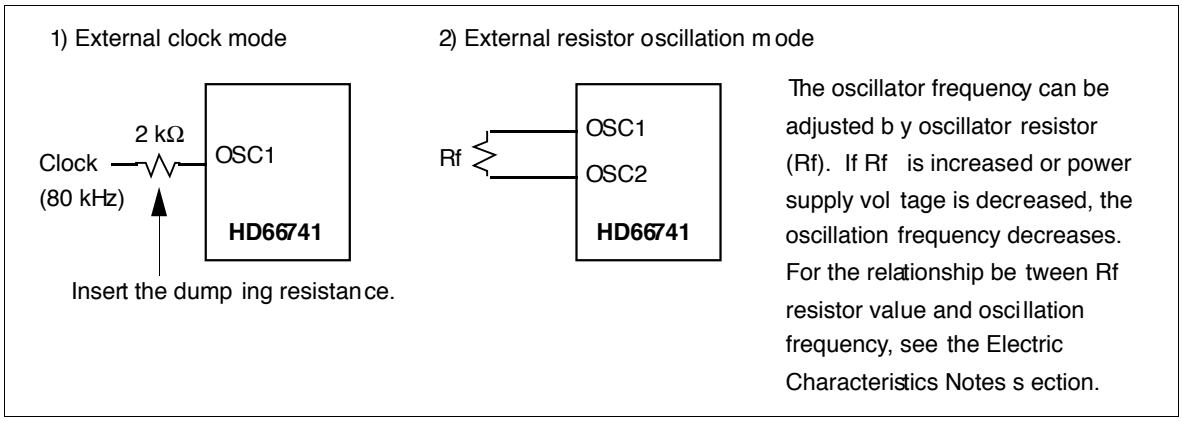


Figure 21 Oscillation Circuits

Table 17 Relationship between Drive Duty Ratio and Frame Frequency (fosc = 75 kHz)

	Display mode									
	1-line Display	2-line Display	3-line Display	4-line Display	5-line Display	6-line Display	7-line Display	8-line Display	9-line Display	10-line Display
	Set value for NL3–0									
LCD Drive	**0000**	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1000**	**1001**
Multiplexing duty ratio	1/8	1/16	1/24	1/32	1/40	1/48	1/56	1/64	1/72	1/80
Drive bias (recommended value)	1/4	1/5	1/6	1/6	1/7	1/8	1/8	1/9	1/9.5	1/10
Frame frequency	73 Hz	73 Hz	73 Hz	73 Hz	72 Hz	74 Hz	74 Hz	73 Hz	65 Hz	59 Hz
One-frame frequency	1,024	1,024	1,032	1,024	1,040	1,008	1,008	1,024	1,152	1,280

Note: If the frame frequency is low and the display flickers, increase the oscillation frequency (fosc). Particularly in the 9-line display and 10-line display modes, note that the frame frequency is lowered.

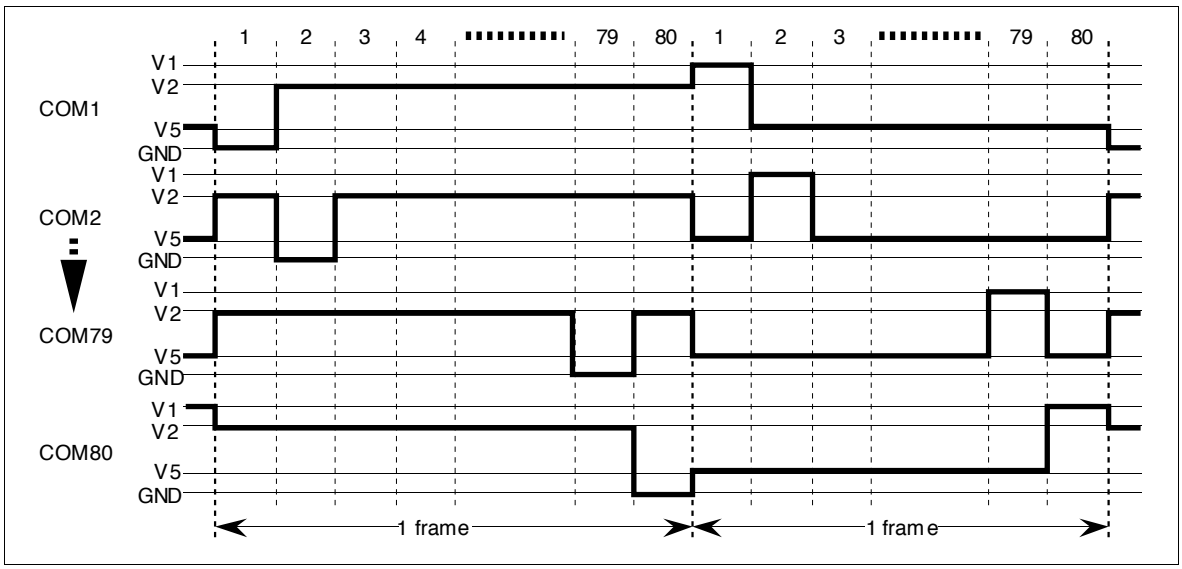


Figure 22 LCD Drive Output Waveform (B-pattern AC Drive with 1/80 Multiplexing Duty Ratio)

n-raster-row Reversed AC Drive

The HD66741 supports not only the LCD reversed AC drive in a one-frame unit (B-pattern waveform) but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 32 raster-rows (C-pattern waveform). When a problem affecting display quality occurs, such as crosstalk at high-duty driving of more than five lines (1/40 duty), the n-raster-row reversed AC drive (C-pattern waveform) can improve the quality. Determine the number of raster-rows n (NW bit set value + 1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-rows is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.

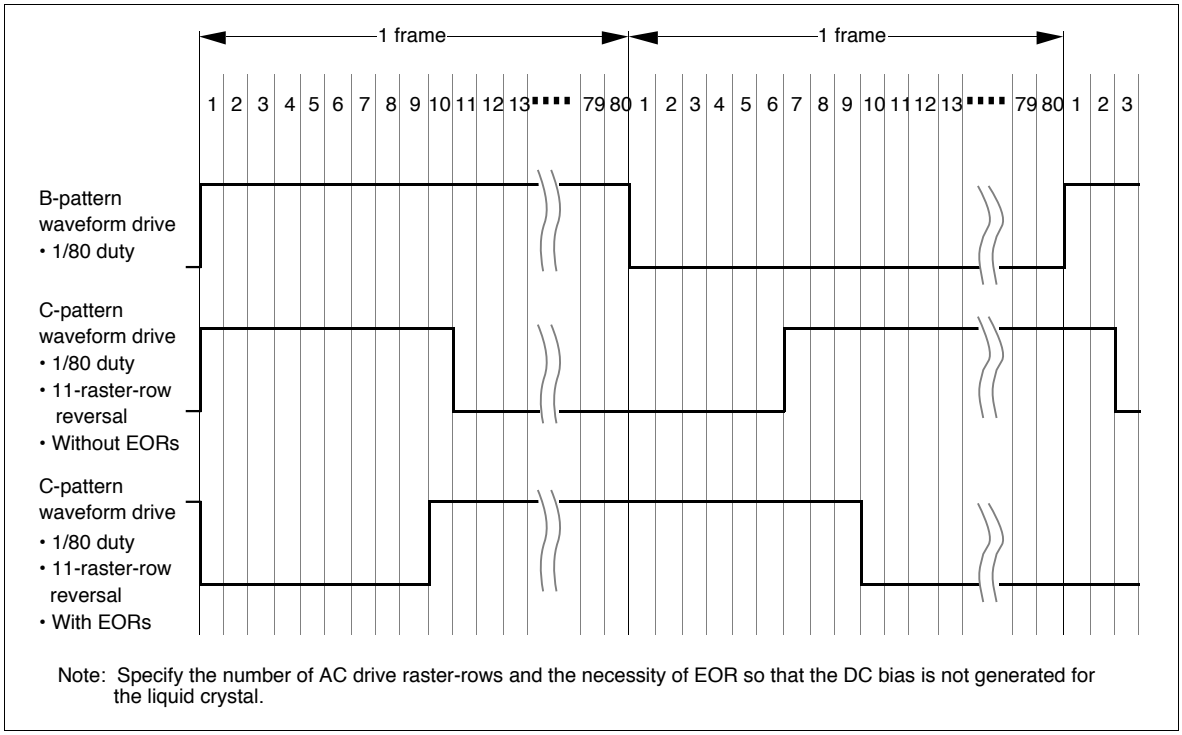


Figure 23 Example of an AC Signal under n-raster-row Reversed AC Drive

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal booster, circuits should be connected as shown in figure 41. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register.

The HD66741 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential difference between V_{LCD} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.

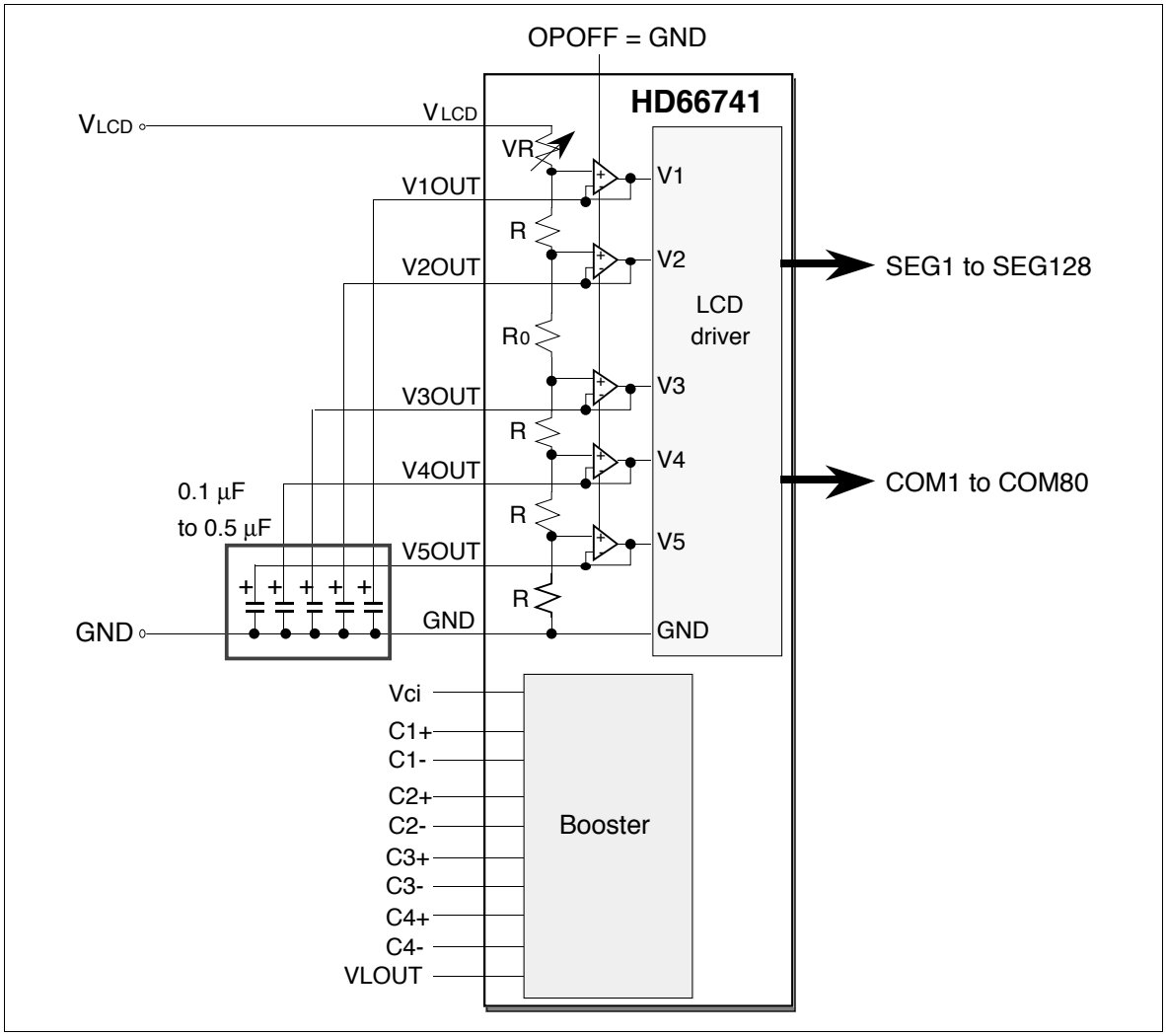


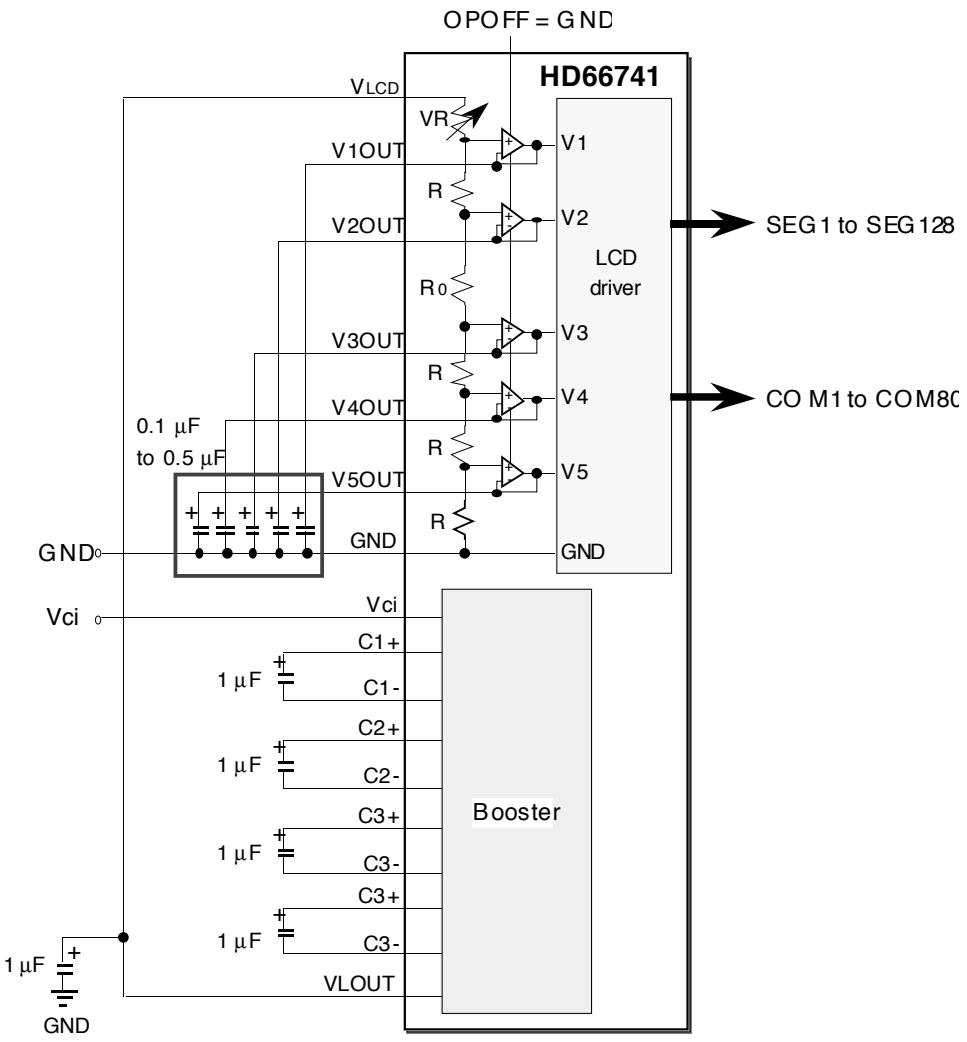
Figure 24 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal booster, circuits should be connected as shown in figure 42. Here, contrast can be adjusted through the CT bits of the contrast control instruction. Temperature can be compensated either through the CT bits or by controlling the reference voltage for the booster (Vci pin) using a thermistor.

Note that Vci is both a reference voltage and power supply for the booster. The reference voltage must therefore be adjusted using an emitter-follower or a similar element so that sufficient current can be supplied. In this case, Vci must be equal to or smaller than the V_{CC} level.

The HD66741 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, potential difference between V_{LCD} and V1 must be 0.1 V or higher, and that between V4 and GND must be 1.4 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.



Notes:
1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (17 V). Particularly, Vci must be 3.3 V or less for five-times boosting.
2. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.
3. Polarized capacitors must be connected correctly.
4. Circuits for temperature compensation should be based on the sample circuit in figure 43.

Figure 25 Internal Booster for LCD Drive Voltage Generation

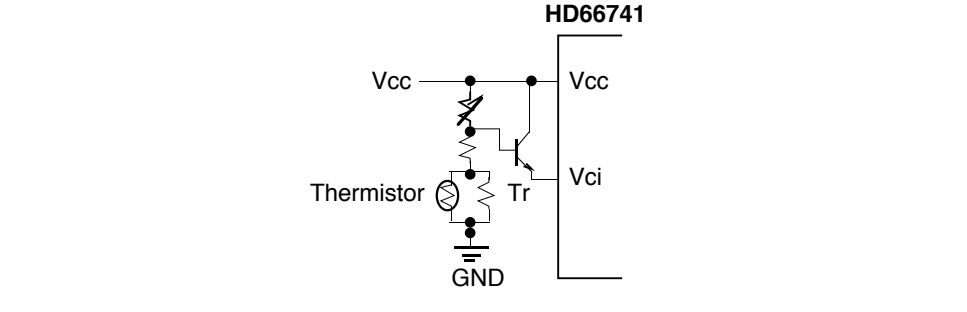


Figure 26 Temperature Compensation Circuit

Switching the Boosting Multiplying Factor

Instruction bits (BT1/0 bits) can optionally select the boosting multiplying factor of the internal booster. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the boosting multiplying factor for the minimum requirements. For details, see the Partial-display-on Function section.

Due to the maximum boosting multiplying factor, the following external capacitor needs to be connected. For example, when the maximum boosting is quadrupled, the capacitors between C4+ and C4– for five-times boosting are not needed, so these pins must be open.

Table 18 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Triple boosting output
0	1	Quadruple boosting output
1	0	Five-times boosting output
1	1	Setting inhibited

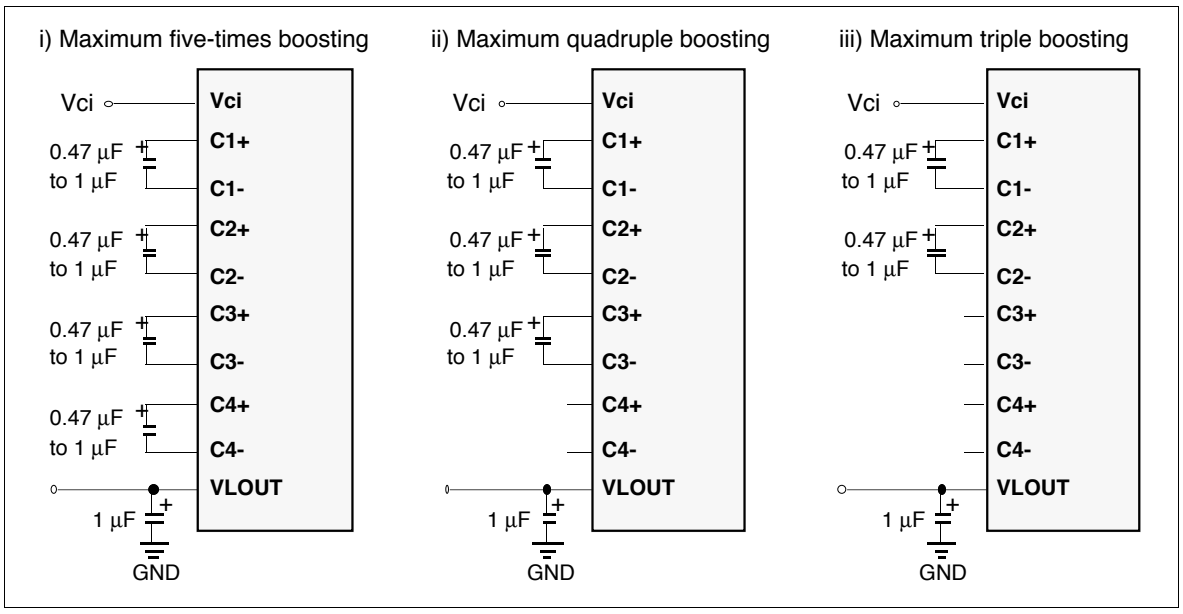


Figure 27 Booster Output Multiplying Factor Switching

Example of Power-supply Voltage Generator for More Than Five-times Boosting Output

The HD66741 incorporates the booster for up to five-times boosting. However, the LCD drive voltage (VLCD) will not be enough for five-times boosting from Vcc when the power-supply voltage of Vcc is low or when the LCD drive voltage is high for the high-contrast LCD display. In this case, the reference voltage (Vci) for boosting can be set higher than the power-supply voltage of Vcc.

Set the Vci input voltage for the booster to 5.5 V or less within the range of Vcc + 1.0 V. Control the Vci voltage so that the boosting output voltage (VLOUT) should be less than the absolute maximum ratings (17 V).

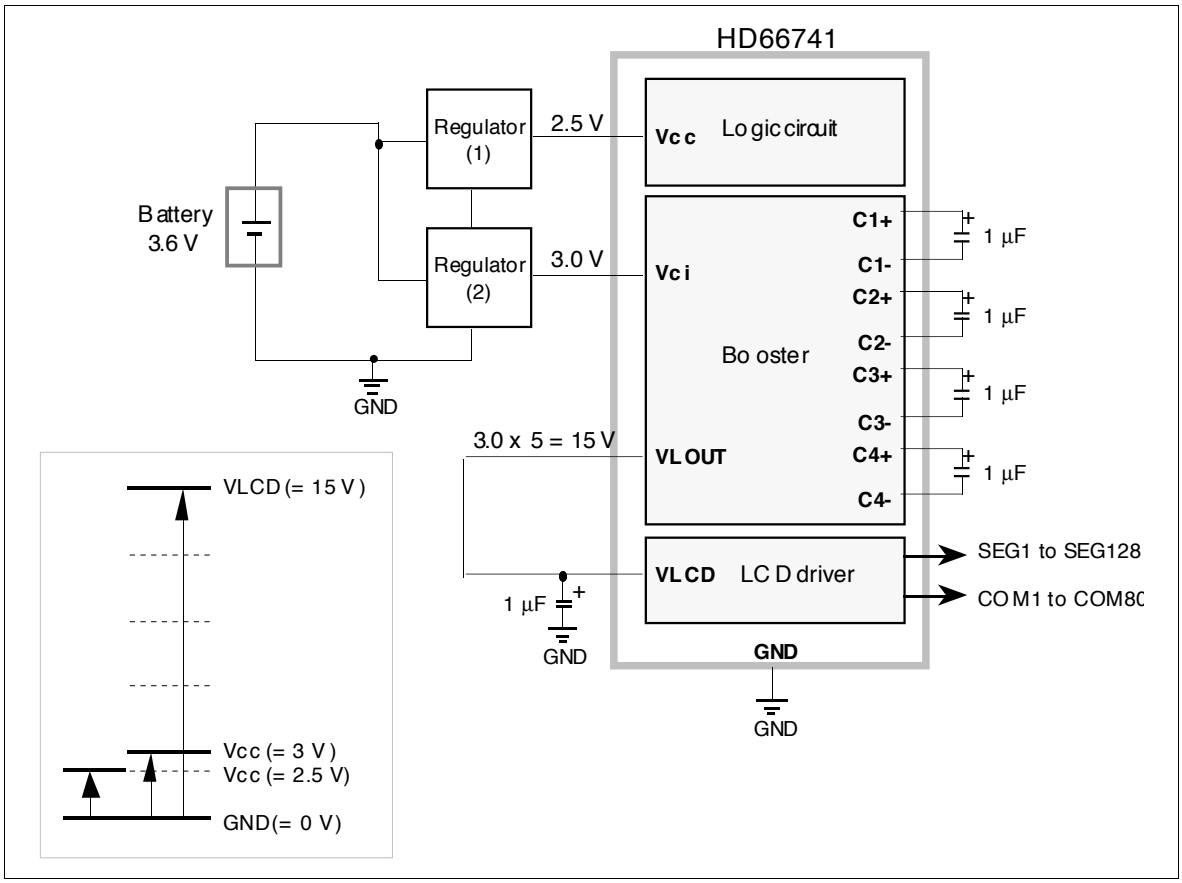
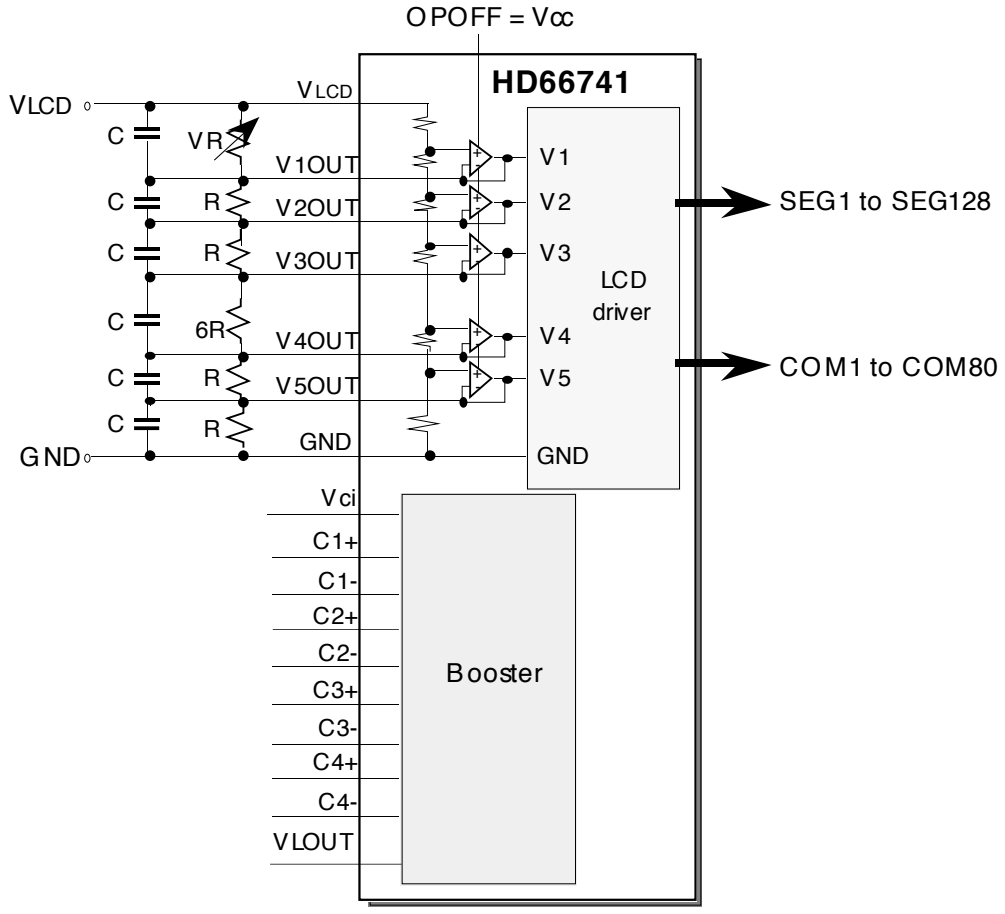


Figure 28 Usage Example of Booster at Vci > Vcc

When External Bleeder Resistors are Used

When internal operational amplifiers cannot fully drive the LCD panel used, V1 to V5 voltages can be supplied through external bleeder resistors or external voltage follower operational amplifier (figure 46). Here, the OPOFF pin must be set to the V_{CC} level to turn off the internal operational amplifiers. Since the internal contrast adjuster is disabled, contrast must be adjusted externally. Connection of external bleeder-resistors can specify a given bias value from 1/4 to 1/10. Figure 46 shows connection for 1/10-bias drive voltage generation. Internal boosters can be used as they are. However, use the external power supply since the through current in bleeder resistors becomes large, loads in the internal booster are heavy, and the boosting output voltage drops.



Notes: 1. Resistance of each external bleeder resistor should be 2 kΩ to 10 kΩ.
2. Add 0.1 µF to 0.5 µF capacitors in parallel with each external bleeder resistor.
3. The bias current value for driving LCDs can be varied by adjusting the resistance (6R) betweer the V3OUT and V4OUT pins.
4. The internal contrast adjuster is disabled; contrast must be adjusted either by controlling the external variable resistor between VLCD and V1 for the booster.

Figure 29 Circuit Using External Bleeder Resistors

Contrast Adjuster

Software can adjust 64-step contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between V_{LCD} and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor between V_{LCD} and V1 (VR) can be precisely adjusted in a 0.05 x R unit within a range from 0.05 x R through 3.20 x R, where R is a reference resistance obtained by dividing the total resistance.

The HD66741 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT5-0 bits must be adjusted so that potential difference between V_{LCD} and V1 is 0.1 V or higher and that between V4 and GND is 1.4 V or higher when liquid-crystal drives, particularly when the VR is small.

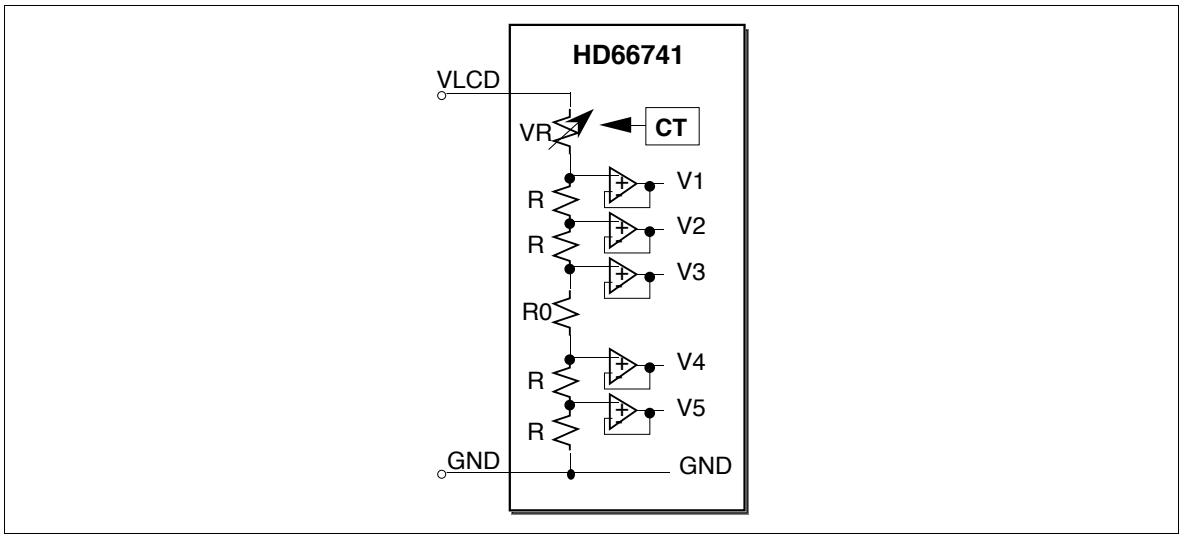


Figure 30 Contrast Adjuster

Table 19 Contrast Adjustment Bits (CT) and Variable Resistor Values

CT Set Value						Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT5	CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	0	3.20 x R	(Small)	(Light)
0	0	0	0	0	1	3.15 x R		
0	0	0	0	1	0	3.10 x R		
0	0	0	0	1	1	3.05 x R		
0	0	0	1	0	0	3.00 x R		
0	0	0	1	0	1	2.95 x R		
0	0	0	1	1	0	2.90 x R		
0	0	0	1	1	1	2.85 x R		
0	0	1	0	0	0	2.80 x R		
0	0	1	0	0	1	2.75 x R		
0	0	1	0	1	0	2.70 x R		
0	0	1	0	1	1	2.65 x R		
0	0	1	1	0	0	2.60 x R		
0	1	1	1	1	1	1.65 x R		
1	0	0	0	0	0	1.60 x R		
1	0	0	0	0	1	1.55 x R		
1	0	0	0	1	0	1.50 x R		
1	0	0	0	1	1	1.45 x R		
1	0	0	1	0	0	1.40 x R		
1	0	0	1	0	1	1.35 x R		
1	0	0	1	1	0	1.30 x R		
1	0	0	1	1	1	1.25 x R		
1	0	1	0	0	0	1.20 x R		
1	1	1	0	0	1	1.15x R		
1	1	1	1	0	0	0.20 x R		
1	1	1	1	0	1	0.15 x R		
1	1	1	1	1	0	0.10 x R		
1	1	1	1	1	1	0.05 x R	(Large)	(Deep)

Table 20 Contrast Adjustment per Bias Drive Voltage

Bias	LCD drive voltage: V_{DR}	Contrast adjustment range
1/10 bias drive	$\frac{10 \times R}{10 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.757 \times (V_{LCD}-GND) \le V_{DR} \le 0.995 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{10 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{10 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/9.5 bias drive	$\frac{9.5 \times R}{9.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.748 \times (V_{LCD}-GND) \le V_{DR} \le 0.994 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{9.5 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{9.5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/9 bias drive	$\frac{9 \times R}{9 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.737 \times (V_{LCD}-GND) \le V_{DR} \le 0.994 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{9 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{9 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/8 bias drive	$\frac{8 \times R}{8 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.714 \times (V_{LCD}-GND) \le V_{DR} \le 0.993 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{8 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{8 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/7 bias drive	$\frac{7 \times R}{7 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.686 \times (V_{LCD}-GND) \le V_{DR} \le 0.993 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{7 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{7 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/6 bias drive	$\frac{6 \times R}{6 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.652 \times (V_{LCD}-GND) \le V_{DR} \le 0.992 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{6 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{6 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/5 bias drive	$\frac{5 \times R}{5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.610 \times (V_{LCD}-GND) \le V_{DR} \le 0.990 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{5 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/4 bias drive	$\frac{4 \times R}{4 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \le V_{DR} \le 0.988 \times (V_{LCD}-GND)$ - Limit of potential difference between V4 and GND : $\frac{2 \times R}{4 \times R + VR} \times (V_{LCD}-GND) \ge 1.4$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{4 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]

Liquid Crystal Display Drive Bias Selector

An optimum liquid crystal display bias value can be selected using BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL3-0 bits). Liquid crystal display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is an ideal value where the optimum contrast is obtained. Driving by using a lower value than the optimum bias value provides lower contrast and lower liquid crystal display voltage (potential difference between V1 and GND). When the liquid crystal display voltage is insufficient even if a five-times booster is used or output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid crystal bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT4-0 bits) and selecting the booster output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N} + 1}$$

Table 21 Optimum Drive Bias Values

LCD drive duty ratio	1/80	1/72	1/64	1/56	1/48	1/40	1/32	1/24	1/16	1/8
(NL3-0 set value)	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
Optimum drive bias value	1/10	1/9.5	1/9	1/8	1/8	1/7	1/6	1/6	1/5	1/4
(BS2-0 set value)	000	001	010	011	011	100	101	101	110	111

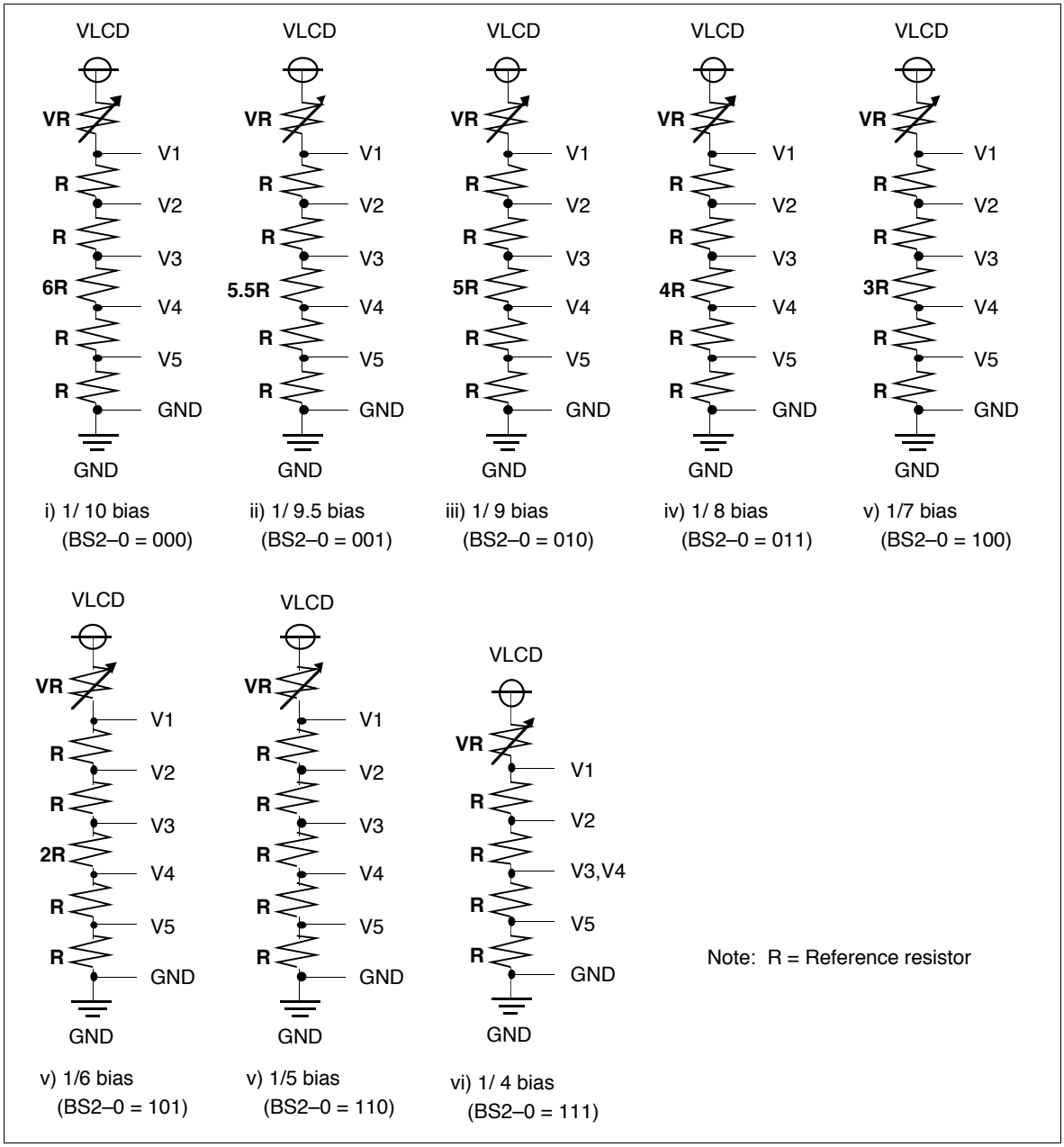


Figure 31 Liquid Crystal Display Drive Bias Circuit

LCD Panel Interface

The HD66741 has a function for changing the common driver/segment driver output shift direction using the CMS bit and SGS bit to meet the chip mounting positions of the HD66741. This is to facilitate the interface wiring to the LCD panel with COG or TCP installed.

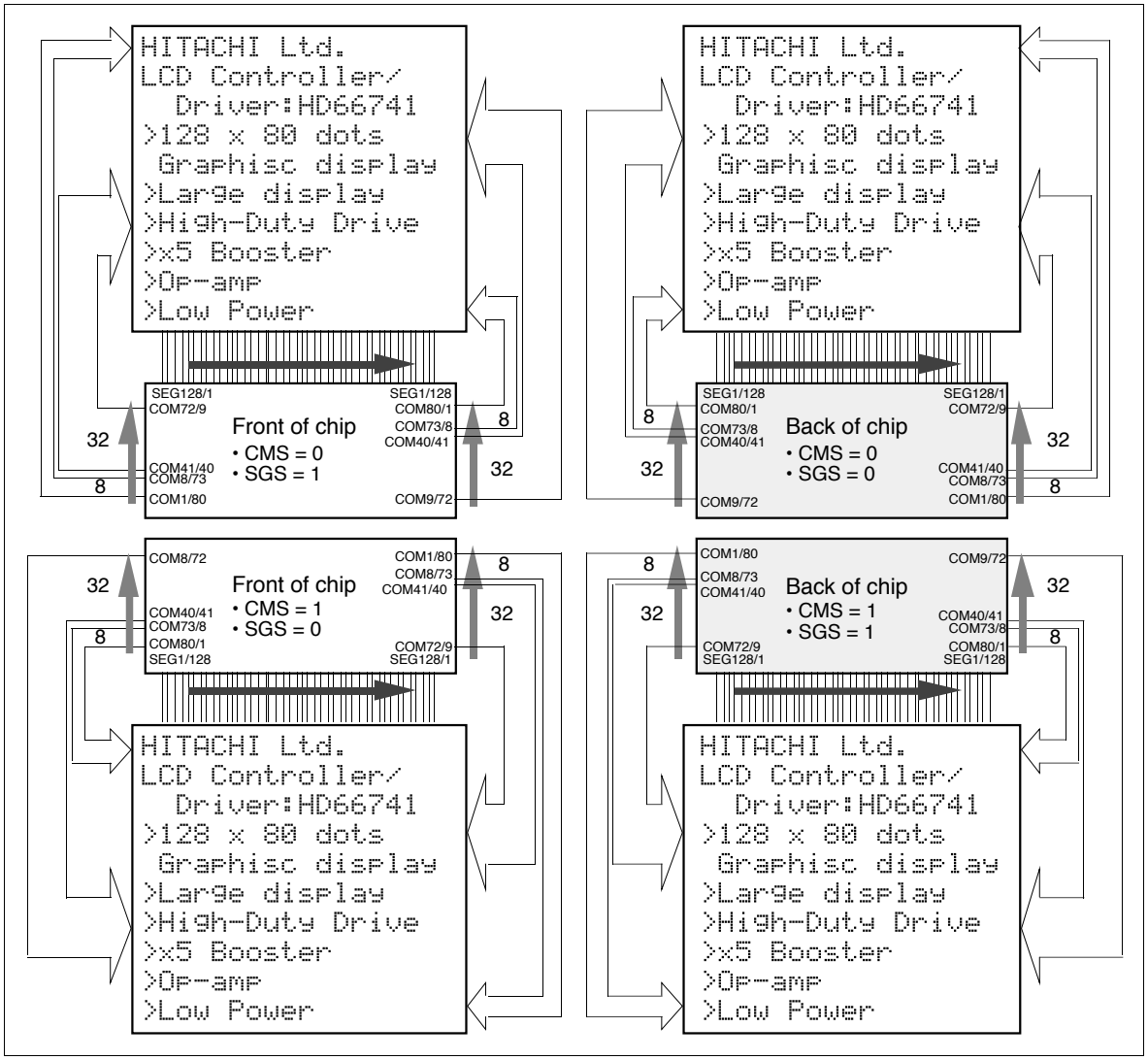


Figure 32 1/80 Duty Drive Pattern Wiring

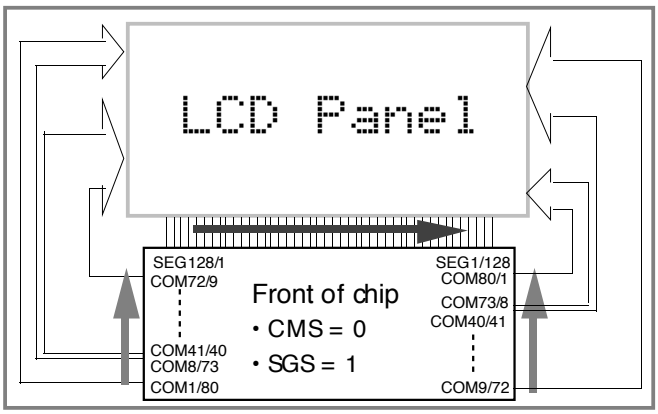


Figure 33 1-line Display Pattern Wiring

Table 22 Number of Left and Right Extension Lines of Common Driver

Drive Duty Ratio	Left Edge of Screen	Right Edge of Screen
1/48	16 (COM1–8, 41–48)	32 (COM9–40)
1/56	24 (COM1–8, 41–56)	32 (COM9–40)
1/64	32 (COM1–8, 41–64)	32 (COM9–40)
1/72	40 (COM1–8, 41–72)	32 (COM9–40)
1/80	40 (COM1–8, 41–72)	40 (COM9–40, 73–80)

Vertical Smooth Scroll Display

The HD66741 can scroll graphics display vertically in units of raster-rows. This is achieved by writing display data into a one-line area that is not being used for display. In other words, one line can be used to achieve continuous smooth vertical scroll even in a 9-line or less display. Here, after the 10th line is displayed, the first line is displayed again. When the 10th line is fully displayed, all one-line display data must be rewritten immediately after scrolling because there is no non-displayed area. Additionally, when display areas of a graphics icon such as a pictogram or a menu bar are partially fixed-displayed, the remaining areas can be displayed. For details, see the Partial Smooth Scroll Display Function section.

Specifically, this function is controlled by incrementing or decrementing the value in the display-start line bits (SL2 to SL0) and display-start raster-row bits (SN3 to SN0) by 1. For example, to smoothly scroll up, first set line bits SN3 to SN0 to 0000, and increment SL2 to SL0 by 1 from 000 to 111 to scroll seven raster-rows. Then increment line bits SN3 to SN0 to 0001, and again increment SL2 to SL0 by 1 from 000 to 111. If the vertical double-height display is at the top of the line, scrolling is done by each two raster-row.

When the response speed of the liquid crystal is low or when high-speed scrolling is needed, two- to four-raster-row scrolling is recommended.

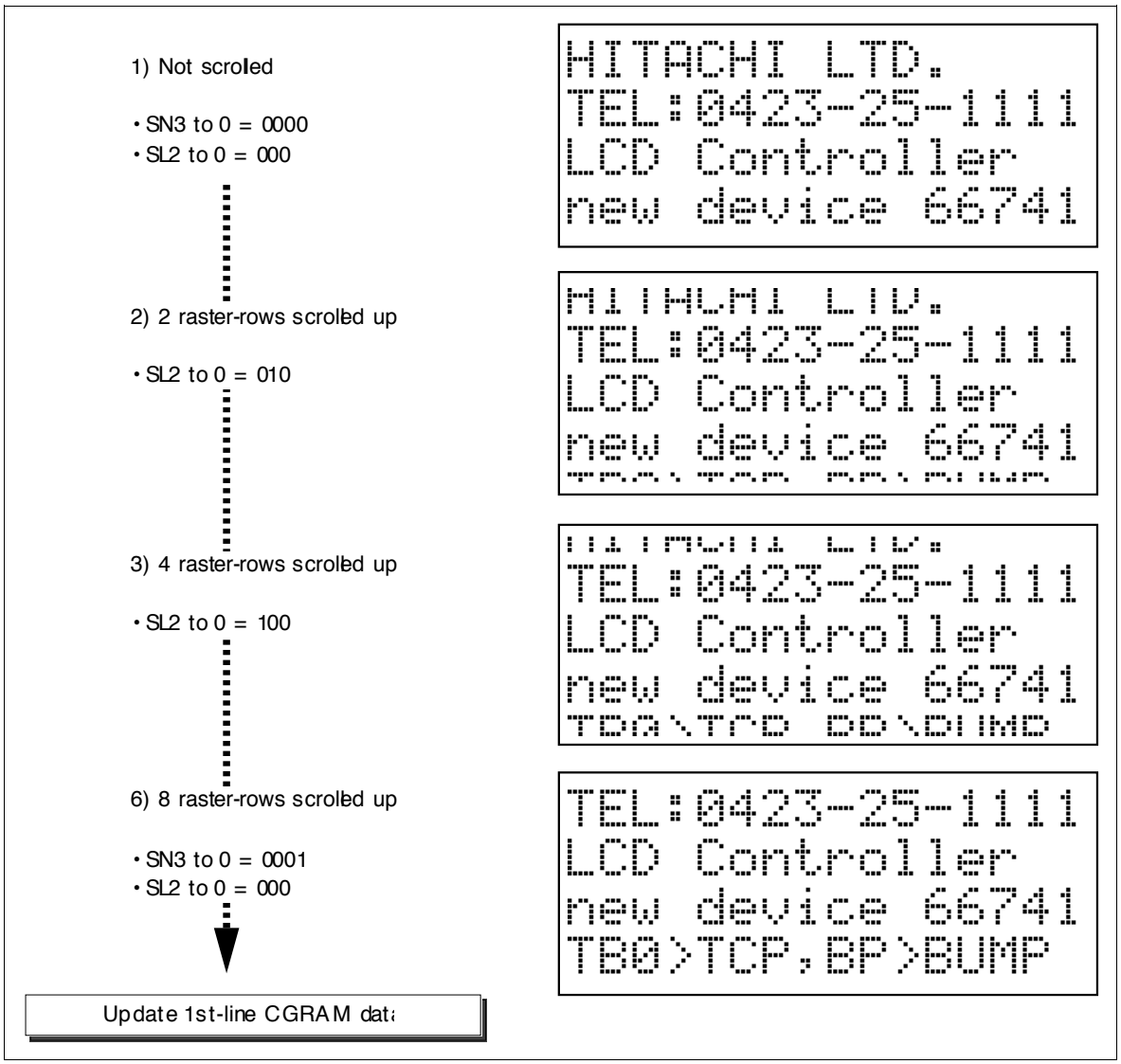


Figure 34 Vertical Smooth Scroll (4-line Display)

Setting Instructions (10-line Display: NL3-0 = 1001)

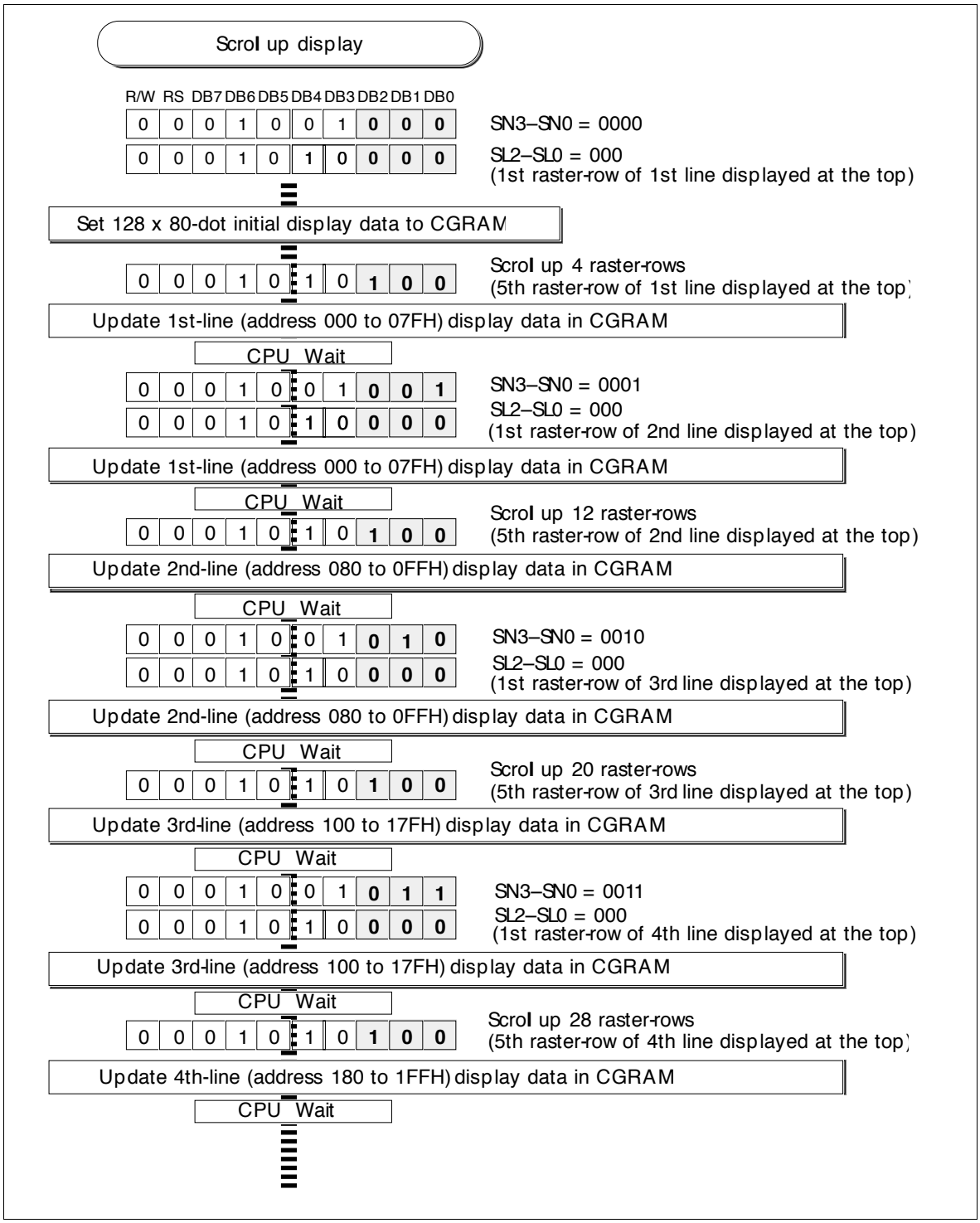


Figure 35 Setting Instructions for Vertical Smooth Scroll

Double-height Display

The HD66741 can double the height of any desired area from the first to 10th lines. A line can be selected by the DL1 to DL10 bits as listed in table 38. All the font characters or graphics display patterns stored in the CGRAM can be doubled in height, allowing easy recognition. Note that there should be no space between the lines for double-height display (figure 61).

In vertical smooth scrolling, when the display-start setting line is displaying at double height, scrolling can be done by each two-line (dot).

Table 23 Double-height Display Specifications

Bit Setting	Display Position
DL1 = 1	1st line: double-height
DL2 = 1	2nd line: double-height
DL3 = 1	3rd line: double-height
DL4 = 1	4th line: double-height
DL5 = 1	5th line: double-height
DL6 = 1	6th line: double-height
DL7 = 1	7th line: double-height
DL8 = 1	8th line: double-height
DL9 = 1	9th line: double-height
DL10 = 1	10th line: double-height

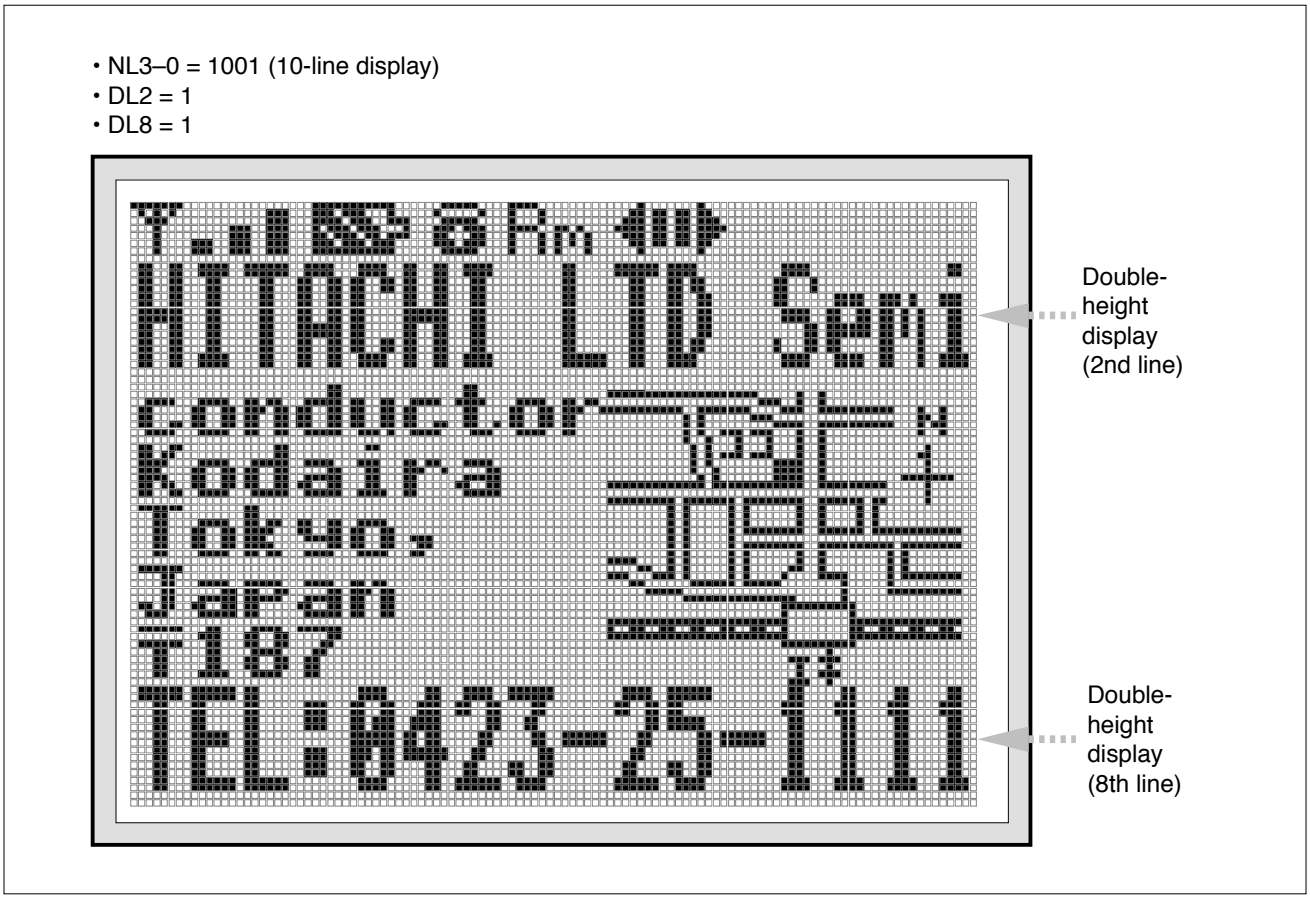


Figure 36 Double-height Display (2nd and 8th Lines)

Partial Smooth Scroll Display Function

The HD66741 can partially fixed-display the areas of a graphics icon, such as a pictogram or a menu bar, and perform vertical smooth scrolling of the remaining bit-map areas. Since the PS1 to PS0 bits do not perform smooth scrolling of the upper first to third display lines but does fixed-display, pictograms can be placed. When CN1 to CN0 bits are set to 10, the first line is displayed at the bottom edge of the LCD screen, and the menu bar can be fixed-displayed at the bottom. This function can largely control the bit-map rewrite frequencies and reduce software loads.

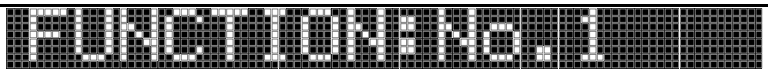
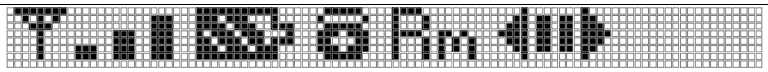
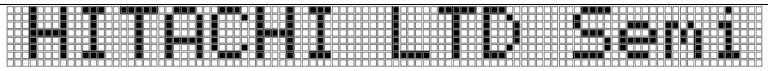
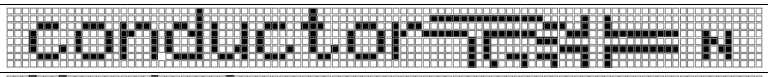
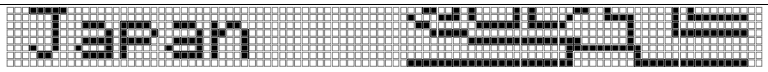
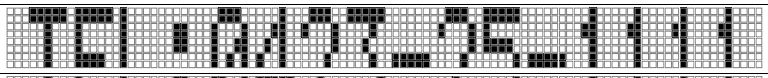
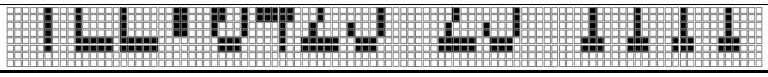
Table 24 Bit Setting and Display Lines

Bit Setting	COM Position	CN1–0 = 00					CN1–0 = 10				
		SN3–0 = 0000	SN3–0 = 0001	SN3–0 = 0010	SN3–0 = 0011	SN3–0 = 0011	SN3–0 = 0000	SN3–0 = 0001	SN3–0 = 0010	SN3–0 = 0011	SN3–0 = 0100
PS1–0 = 00	COM1	1st line	2nd line	3rd line	4th line	5th line	2nd line	3rd line	4th line	5th line	6th line
		2nd line	3rd line	4th line	5th line	6th line	3rd line	4th line	5th line	6th line	7th line
		3rd line	4th line	5th line	6th line	7th line	4th line	5th line	6th line	7th line	8th line
		4th line	5th line	6th line	7th line	8th line	5th line	6th line	7th line	8th line	9th line
		5th line	6th line	7th line	8th line	9th line	6th line	7th line	8th line	9th line	10th line
		6th line	7th line	8th line	9th line	10th line	7th line	8th line	9th line	10th line	1st line
		7th line	8th line	9th line	10th line	1st line	8th line	9th line	10th line	1st line	2nd line
		8th line	9th line	10th line	1st line	2nd line	9th line	10th line	1st line	2nd line	3rd line
		9th line	10th line	1st line	2nd line	3rd line	10th line	1st line	2nd line	3rd line	4th line
	COM80	10th line	1st line	2nd line	3rd line	4th line	1st line	2nd line	3rd line	4th line	5th line
PS1–0 = 01	COM1	1st line	1st line	1st line	1st line	1st line	1st line	2nd line	3rd line	4th line	5th line
		1st line	2nd line	3rd line	4th line	5th line	2nd line	3rd line	4th line	5th line	6th line
		2nd line	3rd line	4th line	5th line	6th line	3rd line	4th line	5th line	6th line	7th line
		3rd line	4th line	5th line	6th line	7th line	4th line	5th line	6th line	7th line	8th line
		4th line	5th line	6th line	7th line	8th line	5th line	6th line	7th line	8th line	9th line
		5th line	6th line	7th line	8th line	9th line	6th line	7th line	8th line	9th line	10th line
		6th line	7th line	8th line	9th line	10th line	7th line	8th line	9th line	10th line	2nd line
		7th line	8th line	9th line	10th line	2nd line	8th line	9th line	10th line	2nd line	3rd line
		8th line	9th line	10th line	2nd line	3rd line	9th line	10th line	2nd line	3rd line	4th line
	COM80	9th line	10th line	2nd line	3rd line	4th line	1st line	1st line	1st line	1st line	1st line
PS1–0 = 10	COM1	1st line	1st line	1st line	1st line	1st line	2nd line	2nd line	2nd line	2nd line	2nd line
		2nd line	2nd line	2nd line	2nd line	2nd line	1st line	2nd line	3rd line	4th line	5th line
		1st line	2nd line	3rd line	4th line	5th line	2nd line	3rd line	4th line	5th line	6th line
		2nd line	3rd line	4th line	5th line	6th line	3rd line	4th line	5th line	6th line	7th line
		3rd line	4th line	5th line	6th line	7th line	4th line	5th line	6th line	7th line	8th line
		4th line	5th line	6th line	7th line	8th line	5th line	6th line	7th line	8th line	9th line
		5th line	6th line	7th line	8th line	9th line	6th line	7th line	8th line	9th line	10th line
		6th line	7th line	8th line	9th line	10th line	7th line	8th line	9th line	10th line	3rd line
		7th line	8th line	9th line	10th line	3rd line	8th line	9th line	10th line	3rd line	4th line
	COM80	8th line	9th line	10th line	3rd line	4th line	1st line	1st line	1st line	1st line	1st line
PS1–0 = 11	COM1	1st line	1st line	1st line	1st line	1st line	2nd line	2nd line	2nd line	2nd line	2nd line
		2nd line	2nd line	2nd line	2nd line	2nd line	3rd line	3rd line	3rd line	3rd line	3rd line
		3rd line	3rd line	3rd line	3rd line	3rd line	1st line	2nd line	3rd line	4th line	5th line
		1st line	2nd line	3rd line	4th line	5th line	2nd line	3rd line	4th line	5th line	6th line
		2nd line	3rd line	4th line	5th line	6th line	3rd line	4th line	5th line	6th line	7th line
		3rd line	4th line	5th line	6th line	7th line	4th line	5th line	6th line	7th line	8th line
		4th line	5th line	6th line	7th line	8th line	5th line	6th line	7th line	8th line	9th line
		5th line	6th line	7th line	8th line	9th line	6th line	7th line	8th line	9th line	10th line
		6th line	7th line	8th line	9th line	10th line	7th line	8th line	9th line	10th line	4th line
	COM80	7th line	8th line	9th line	10th line	4th line	1st line	1st line	1st line	1st line	1st line

Notes: 1. The shadow lines above are fixed-displayed. They do not depend on the setting values of the SN3–0 or SL3–0 bits.
2. The SN3–0 and SL3–0 bits specify the next first scroll display line of the fixed-displayed lines.
3. When the drive duty ratio is nine lines (1/72 duty ratio) or less and CN1–0 is 10, the first line shifts to the last displayed line.

Partial Smooth Scroll Display Examples

Table 25 Data Setting to the CGRAM

CGRAM Address	CGRAM Data
000 to 07F	
080 to 0FF	
100 to 17F	
180 to 1FF	
200 to 27F	
280 to 2FF	
300 to 37F	
380 to 3FF	
400 to 47F	
480 to 4FF	

i) Initial Screen Display
• PS1–0 = 10: Fixed-displays the first and second lines
• CN1–0 = 10: Moves the first line to the bottom edge
• SN3–0 = 0010: Starts display from the third line
• SL2–0 = 000

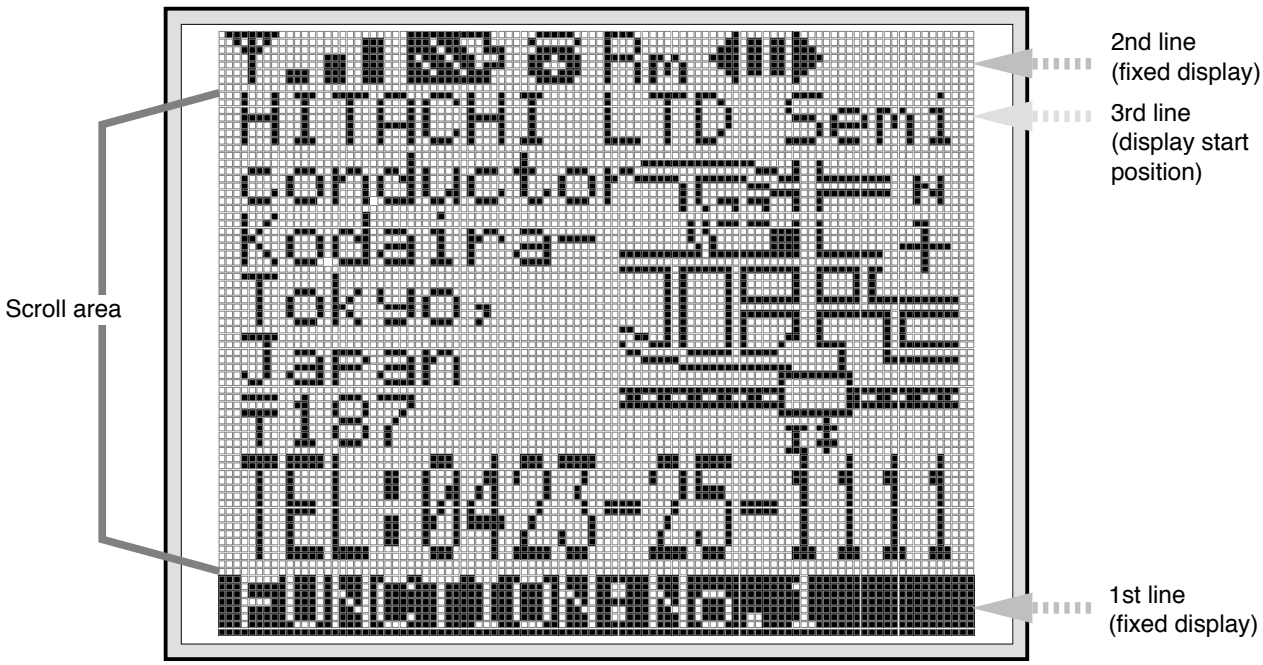


Figure 37 Example of Initial Screen in the Partial Smooth Scroll Mode

ii) 4-dot Partial Scroll Up
• PS1–0 = 10: Fixed-displays the first and second lines
• CN1–0 = 10: Moves the first line to the bottom edge
• SN3–0 = 0010: Starts display from the third line
• SL2–0 = 100: Shifts up by 4 dots

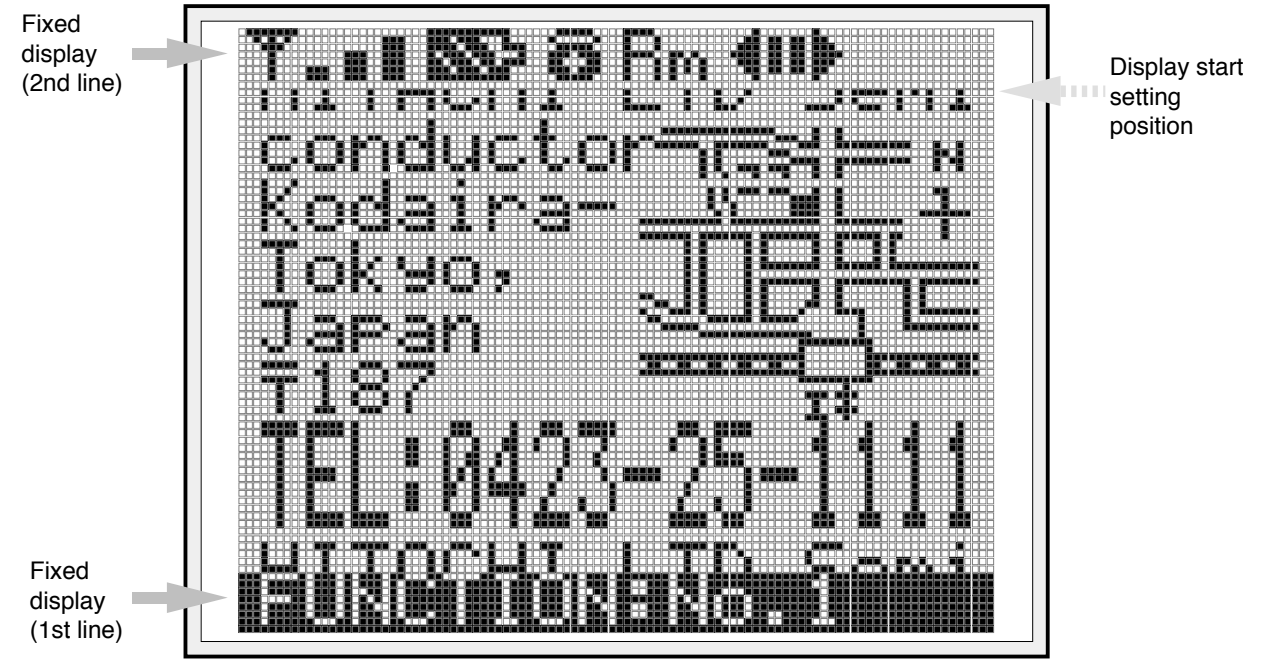


Figure 38 Example of Display Screen in the Partial Smooth Scroll Mode (1)

iii) 8-dot Partial Scroll Up
• PS1–0 = 10: Fixed-displays the first and second lines
• CN1–0 = 10: Moves the first line to the bottom edge
• SN3–0 = 0011: Starts display from the fourth line
• SL2–0 = 000

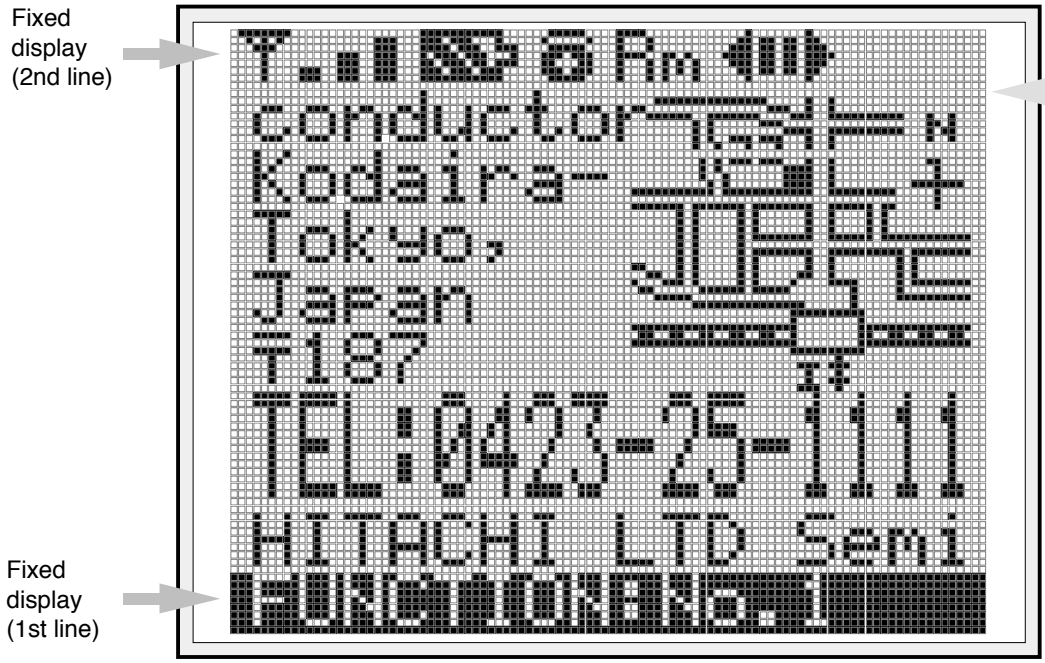


Figure 39 Example of Display Screen in the Partial Smooth Scroll Mode (2)

Reversed Display Function

The HD66741 can display graphics display sections by black-and-white reversal. Black-and-white reversal can be easily displayed when REV is set to 1.

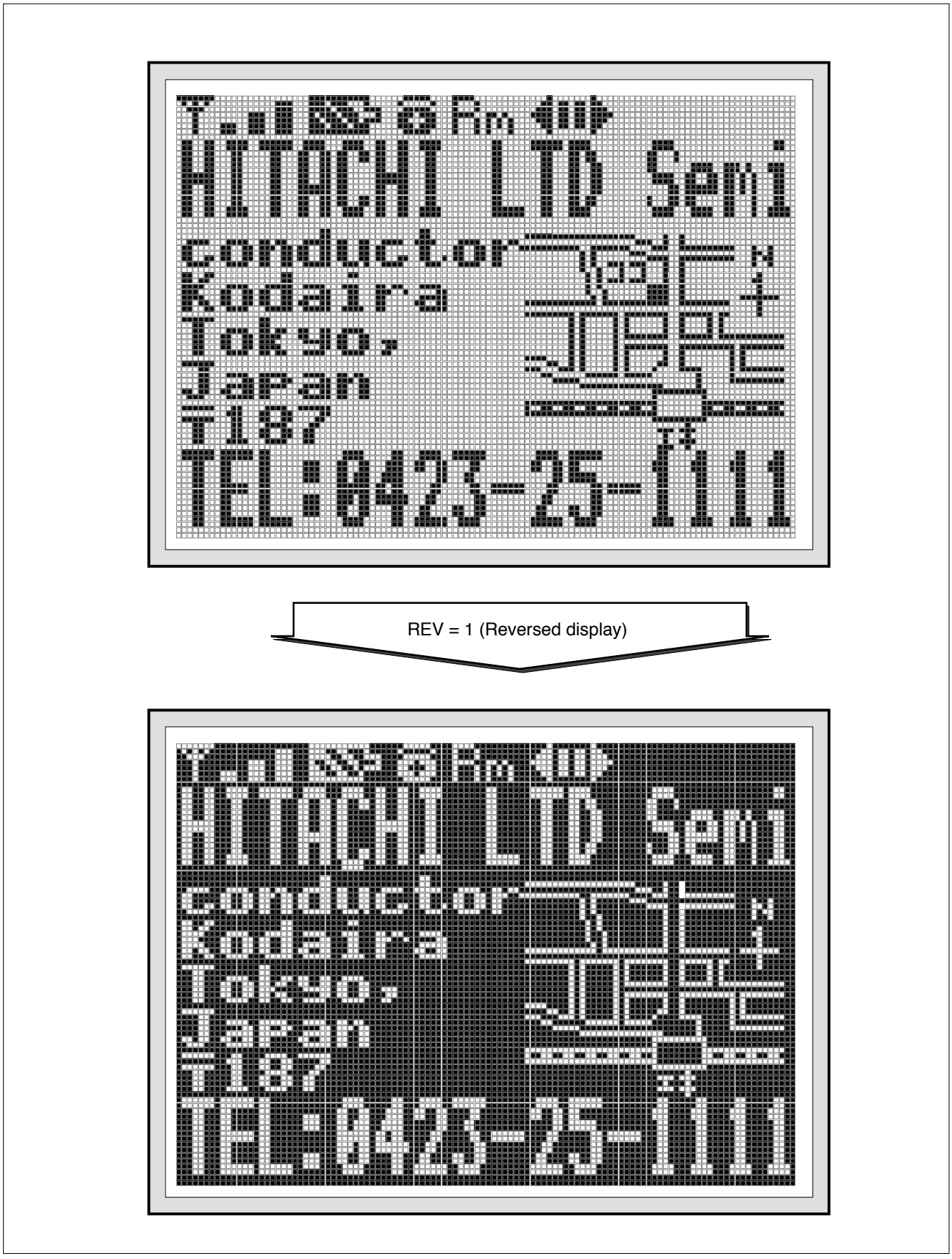


Figure 40 Reversed Display

Partial-display-on Function

The HD66741 can program the liquid crystal display drive duty ratio setting (NL3-0 bits), liquid crystal display drive bias value selection (BS2-0 bits), boost output level selection (BT1/0 bit) and contrast adjustment (CT5-0 bits). For example, in the 10-line display mode (1/80 duty ratio), the HD66741 can selectively drive only the center of the screen or only the top or bottom of the screen by combining these register functions and the centering display (CN1–0 bit) function. This is called partial-display-on. Lowering the liquid crystal display drive duty ratio as required saves the liquid crystal display drive voltage, thus reducing internal current consumption. This is suitable for four-line display of a calendar or time, or the display of only graphics icons (pictograms) at the top or bottom of the screen, which needs to be continuous in the system standby state with minimal current consumption. Here, the non-displayed lines are constantly driven by the unselected level voltage, thus turning off the LCD for the lines.

In general, lowering the liquid crystal display drive duty ratio decreases the optimum liquid crystal display drive voltage and liquid crystal display drive bias value. This reduces output multiplying factors in the booster and greatly controls consumption current.

Table 26 Partial-display-on Function (10-line Display)

Item	Normal 10-line Display	Partial-on Display (Limited 4-line Display)	
LCD screen	10th line displayed	Only four lines on the center of the screen (from the 3rd to 6th lines)	Only four lines at the top and bottom of the screen (from the 1st to 3rd and 10th lines)
LCD drive position shift	Not necessary (CN1–0 = 00)	Necessary (CN1–0 = 01)	Necessary (CN1–0 = 01)
LCD drive duty ratio	1/80 (NL3–0 = 1001)	1/32 (NL3–0 = 0011)	1/32 (NL3–0 = 0011)
LCD drive bias value (optimum)	1/10 (BS2-0 = 000)	1/6 (BS2-0 = 101)	1/6 (BS2-0 = 101)
LCD drive voltage*	12 V to 15 V (adjustable using CT5–0)	6 V to 8 V (adjustable using CT5–0)	6 V to 8 V (adjustable using CT5–0)
Boosting output multiplying factor	Five times (BT1–0 = 10)	Triple (BT1–0 = 00)	Triple (BT1–0 = 00)
Frame frequency (fosc = 90 kHz)	70 Hz	88 Hz	88 Hz

Note: The LCD drive voltage depends on the LCD materials which are actually used. Since the LCD drive voltage is high when the LCD drive duty ratio is high, a low duty ratio is suitable for low-power consumption.

• **1/32-duty Drive at the Top and Bottom of the Screen**

Figure 41 Partial-on Display (Date and Time Indicated) (1)

• **1/32-duty Drive on the Center of the Screen**

Figure 42 Partial-on Display (Date and Time Indicated) (2)

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66741 in the sleep mode, where the device stops all internal display operations, thus reducing current consumption. Specifically, LCD drive is completely halted. Here, all the SEG (SEG1 to SEG128) and COM (COM1 to COM80) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

Table 27 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
LCD control	Turned off	Turned off
R-C oscillation circuit	Operates normally	Halted

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66741 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, character and segment displays, which are controlled by the multiplexing drive method, are completely halted. Here, all the SEG (SEG1 to SEG128) and COM (COM1 to COM80) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than the start-oscillation instruction and the port control instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

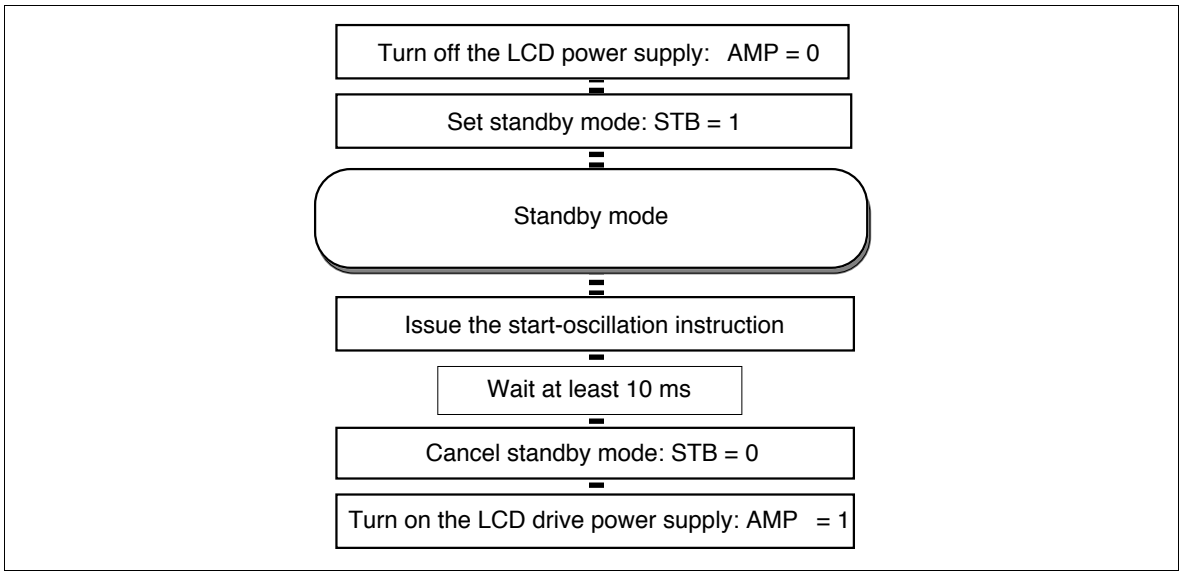


Figure 43 Procedure for Setting and Canceling Standby Mode

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1, 2
Power supply voltage (2)	V_{LCD} – GND	V	–0.3 to +17.0	1, 3
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	1, 4
Storage temperature	Tstg	°C	–55 to +110	1, 5

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. VCC > GND must be maintained.
3. VLCD > GND must be maintained.
4. For bare die and wafer products, specified up to 85˚C.
5. This temperature specifications apply to the TCP package.

DC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[1])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		2, 3
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 1.8 to 2.7 V	2, 3
		–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V	2, 3
Output high voltage (1) (SDA, DB0-7 pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	2, 4
Output low voltage (1) (SDA, DB0-7 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 1.8 to 2.7 V, I_{OL} = 0.1 mA	2
		—	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V, I_{OL} = 0.1 mA	2
Output high voltage (2) (PORT0-2 pins)	V_{OH2}	0.75 V_{CC}	—	—	V	$-I_{OH}$ = 0.1 mA	2
Output low voltage (2) (PORT0-2 pins)	V_{OL2}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1 mA	2
Driver ON resistance (COM pins)	R_{COM}	—	3	20	kΩ	±Id = 0.05 mA, V_{LCD} = 10 V	5
Driver ON resistance (SEG pins)	R_{SEG}	—	3	30	kΩ	±Id = 0.05 mA, V_{LCD} = 10 V	5
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	6
Pull-up MOS current (SDA pin)	$-I_p$	1	10	40	µA	V_{CC} = 3 V, Vin = 0 V	2
Current consumption during normal operation (V_{CC}–GND)	I_{OP}	—	32 (T.B.D.)	55 (T.B.D.)	µA	R-C oscillation, V_{CC} = 3 V, Ta = 25 °C, f_{OSC} = 86 kHz (1/72 duty)	7, 8
Current consumption during sleep mode (V_{CC}–GND)	I_{SL}	—	11	—	µA	R-C oscillation, V_{CC} = 3 V, Ta = 25 °C, f_{OSC} = 86 kHz (1/72 duty)	7, 8
Current consumption during standby mode (V_{CC}–GND)	I_{ST}	—	0.1	5	µA	V_{CC} = 3 V, Ta = 25°C	7, 8
LCD drive power supply current (V_{LCD}–GND)	I_{LCD}	—	18 (T.B.D.)	35 (T.B.D.)	µA	V_{LCD} = 12 V, 1/9 bias, Ta = 25 °C, f_{OSC} = 86 kHz, VTEST3 = Vcc	8
LCD drive voltage (V_{LCD} – GND)	V_{LCD}	4.5	—	15.0	V		9

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Triple-boost output voltage (VLOUT pin)	V_{UP3}	8.5	8.9	9.0	V	V_{CC} = Vci = 3.0 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 86 kHz, Ta = 25°C	12
Quadruple-boost output voltage (VLOUT pin)	V_{UP4}	11.5	11.8	12.0	V	V_{CC} = Vci = 3.0 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 86 kHz, Ta = 25°C	12
Five-times-boost output voltage (VLOUT pin)	V_{UP5}	14.5	14.8	15.0	V	V_{CC} = Vci = 3.0 V, I_O = 30 µA, C = 1 µF, f_{OSC} = 86 kHz, Ta = 25°C	12
Use range of boost output voltages	V_{UP3}, V_{UP4}, V_{UP5}	Vcc	—	15.0	V	For triple to five-times boost	12

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	50	75	150	kHz		10
External clock duty ratio	Duty	45	50	55	%		10
External clock rise time	trcp	—	—	0.2	µs		10
External clock fall time	tfcp	—	—	0.2	µs		10
R-C oscillation clock	f_{OSC}	69	86	103	kHz	Rf = 330 kΩ, V_{CC} = 3 V	11

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	600 (T.B.D.)	—	—	ns	Figure 50
	Read	t_{CYCE}	800 (T.B.D.)	—	—		
Enable high-level pulse width	Write	PW_{EH}	120	—	—	ns	Figure 50
	Read	PW_{EH}	350	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 50
	Read	PW_{EL}	300	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 50
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 50
Address hold time		t_{AHE}	20	—	—	ns	Figure 50
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 50
Write data hold time		t_{HE}	20	—	—	ns	Figure 50
Read data delay time		t_{DDRE}	—	—	300	ns	Figure 50
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 50

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	380 (T.B.D.)	—	—	ns	Figure 50
	Read	t_{CYCE}	500 (T.B.D.)	—	—		
Enable high-level pulse width	Write	PW_{EH}	70	—	—	ns	Figure 50
	Read	PW_{EH}	250	—	—		
Enable low-level pulse width	Write	PW_{EL}	150	—	—	ns	Figure 50
	Read	PW_{EL}	150	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 50
Setup time (RS, R/W to E, CS*)		t_{ASE}	50	—	—	ns	Figure 50
Address hold time		t_{AHE}	20	—	—	ns	Figure 50
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 50
Write data hold time		t_{HE}	20	—	—	ns	Figure 50
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 50
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 50

80-system Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	600 (T.B.D.)	—	—	ns	Figure 51
	Read	t_{CYCR}	800 (T.B.D.)	—	—	ns	Figure 51
Write low-level pulse width		PW_{LW}	120	—	—	ns	Figure 51
Read low-level pulse width		PW_{LR}	350	—	—	ns	Figure 51
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 51
Read high-level pulse width		PW_{HR}	300	—	—	ns	Figure 51
Write/Read rise/fall time		t_{WRr} , $_{WRf}$	—	—	25	ns	Figure 51
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 51
Address hold time		t_{AH}	20	—	—	ns	Figure 51
Write data setup time		t_{DSW}	60	—	—	ns	Figure 51
Write data hold time		t_{H}	20	—	—	ns	Figure 51
Read data delay time		t_{DDR}	—	—	300	ns	Figure 51
Read data hold time		t_{DHR}	5	—	—	ns	Figure 51

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	380 (T.B.D.)	—	—	ns	Figure 51
	Read	t_{CYCR}	500 (T.B.D.)	—	—	ns	Figure 51
Write low-level pulse width		PW_{LW}	70	—	—	ns	Figure 51
Read low-level pulse width		PW_{LR}	250	—	—	ns	Figure 51
Write high-level pulse width		PW_{HW}	150	—	—	ns	Figure 51
Read high-level pulse width		PW_{HR}	150	—	—	ns	Figure 51
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 51
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 51
Address hold time		t_{AH}	20	—	—	ns	Figure 51
Write data setup time		t_{DSW}	60	—	—	ns	Figure 51
Write data hold time		t_{H}	20	—	—	ns	Figure 51
Read data delay time		t_{DDR}	—	—	200	ns	Figure 51
Read data hold time		t_{DHR}	5	—	—	ns	Figure 51

Clock-synchronized Serial Interface Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

(V_{CC} = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t_{SCYC}	0.5	—	20	µs	Figure 52
	At read (send)	t_{SCYC}	1	—	20	µs	Figure 52
Serial clock high-level width	At write (receive)	t_{SCH}	230	—	—	ns	Figure 52
	At read (send)	t_{SCH}	480	—	—	ns	Figure 52
Serial clock low-level width	At write (receive)	t_{SCL}	230	—	—	ns	Figure 52
	At read (send)	t_{SCL}	480	—	—	ns	Figure 52
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 52
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 52
Chip select hold time		t_{CH}	200	—	—	ns	Figure 52
Serial input data setup time		t_{SISU}	100	—	—	ns	Figure 52
Serial input data hold time		t_{SIH}	100	—	—	ns	Figure 52
Serial output data delay time		t_{SOD}	—	—	400	ns	Figure 52
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 52

(V_{CC} = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	At write (receive)	t_{SCYC}	0.2	—	20	µs	Figure 52
	At read (send)	t_{SCYC}	0.5	—	20	µs	Figure 52
Serial clock high-level width	At write (receive)	t_{SCH}	80	—	—	ns	Figure 52
	At read (send)	t_{SCH}	230	—	—	ns	Figure 52
Serial clock low-level width	At write (receive)	t_{SCL}	80	—	—	ns	Figure 52
	At read (send)	t_{SCL}	230	—	—	ns	Figure 52
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 52
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 52
Chip select hold time		t_{CH}	200	—	—	ns	Figure 52
Serial input data setup time		t_{SISU}	40	—	—	ns	Figure 52
Serial input data hold time		t_{SIH}	40	—	—	ns	Figure 52
Serial output data delay time		t_{SOD}	—	—	200	ns	Figure 52
Serial output data hold time		t_{SOH}	5	—	—	ns	Figure 52

Reset Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 53

Electrical Characteristics Notes

1. For bare die products, specified up to 85˚C.
2. The following three circuits are I/O pin configurations (figure 44).

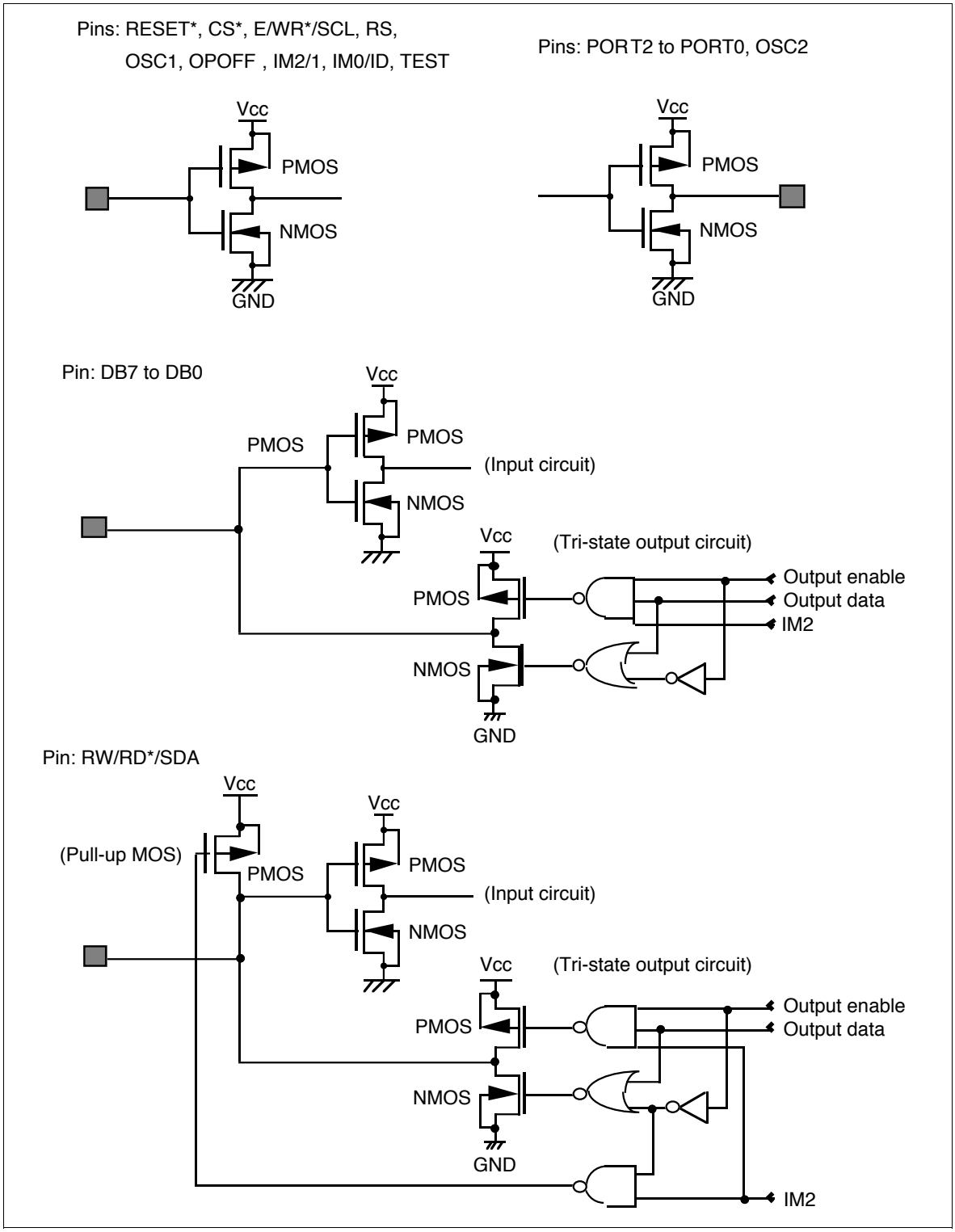


Figure 44 I/O Pin Configuration

3. The TEST pin must be grounded and the IM2/1, IM0/ID, and OPOFF pins must be grounded or connected to Vcc.
4. Corresponds to the high output for clock-synchronized serial interface.
5. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins, and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins.
6. This excludes the current flowing through pull-up MOSs and output drive MOSs.
7. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
8. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 45).

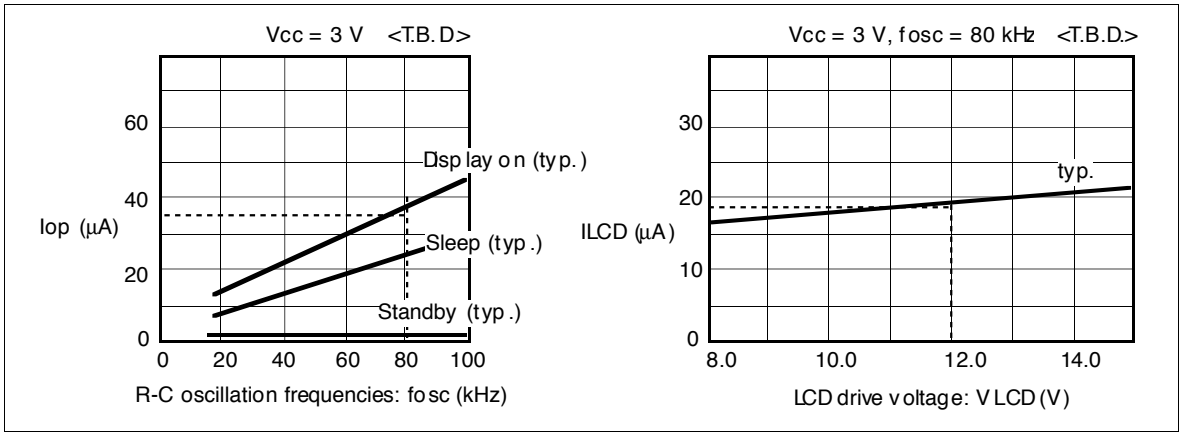


Figure 45 Relationship between the Operation Frequency and Current Consumption

9. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.
10. Applies to the external clock input (figure 46).

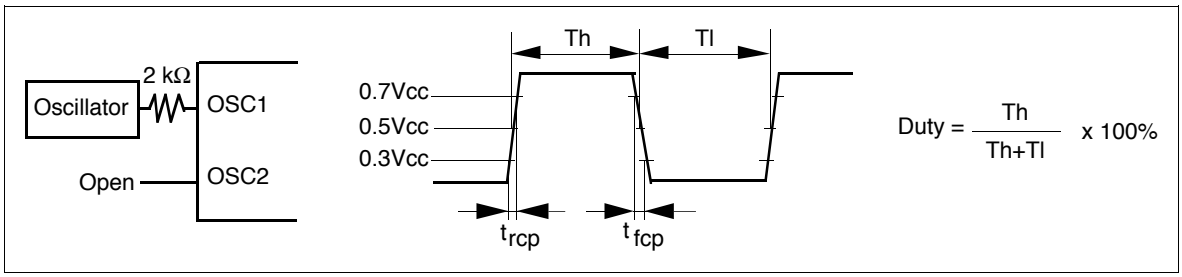
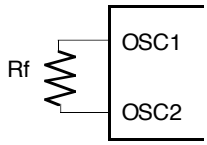


Figure 46 External Clock Supply

11. Applies to the internal oscillator operations using external oscillation resistor Rf (figure 47 and table 28).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Figure 47 Internal Oscillation

Table 28 External Resistance Value and R-C Oscillation Frequency (Referential Data)

External Resistance (Rf)	R-C Oscillation Frequency: fosc <T.B.D.>				
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 4.0 V	Vcc = 5.0 V
200 kΩ			130 kHz		
270 kΩ			100 kHz		
300 kΩ			93 kHz		
330 kΩ	61 kHz	74 kHz	86 kHz	91 kHz	95 kHz
360 kΩ	57 kHz	69 kHz	79 kHz	84 kHz	88 kHz
390 kΩ			74 kHz		
430 kΩ			67 kHz		
470 kΩ			63 kHz		

12. Booster characteristics test circuits are shown in figure 48.

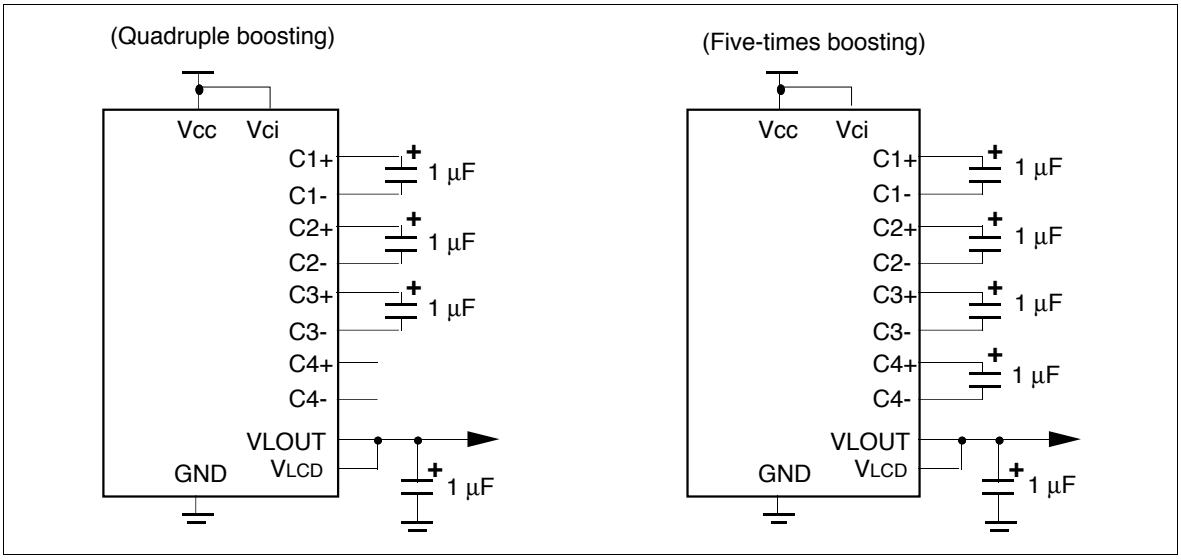
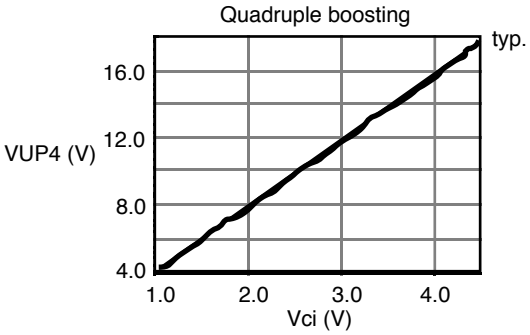


Figure 48 Booster

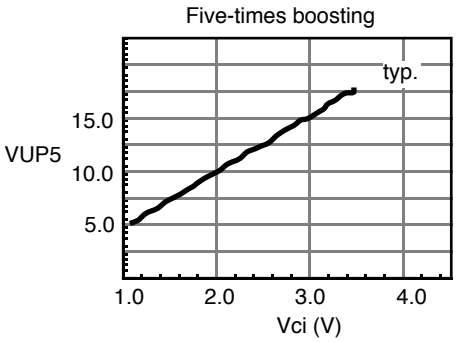
Referential data

VUP4 = VLCD – GND; VUP5 = VLCD – GND

(i) Relation between the obtained voltage and input voltage

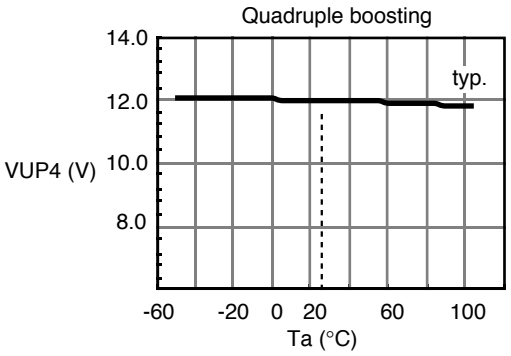


Vci = Vcc, fosc = 80 kHz, Ta = 25°C

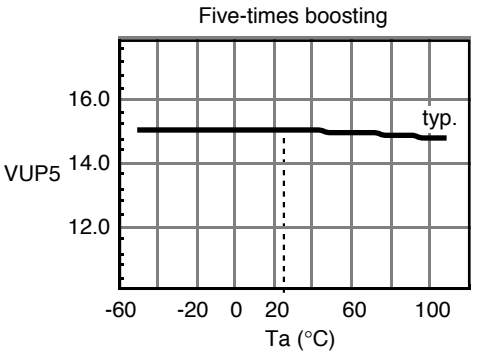


Vci = Vcc, fosc = 80 kHz, Ta = 25°C

(ii) Relation between the obtained voltage and temperature

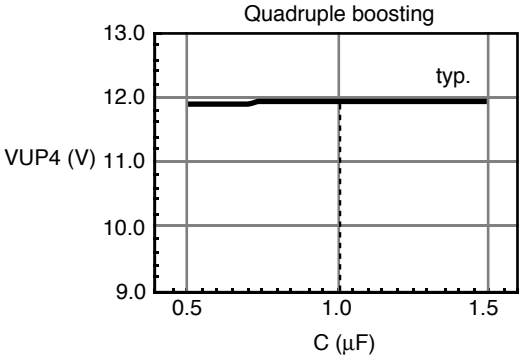


Vci = Vcc = 3 V, fosc = 80 kHz, Io = 30µA

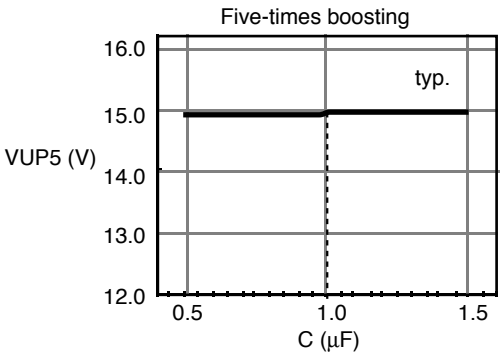


Vci = Vcc = 3 V, fosc = 80 kHz, Io = 30µA

(iii) Relation between the obtained voltage and capacity



Vci = Vcc = 3.0 V, fosc = 80 kHz, Io = 30 µA



Vci = Vcc = 3.0 V, fosc = 80 kHz, Io = 30 µA

Figure 48 Booster (cont)

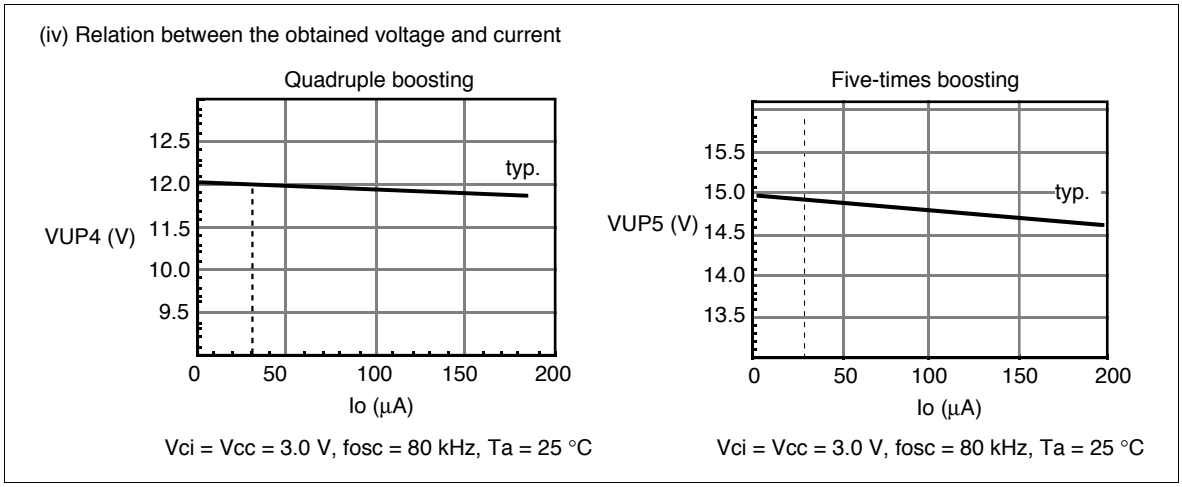


Figure 48 Booster (cont)

Load Circuits

AC Characteristics Test Load Circuits

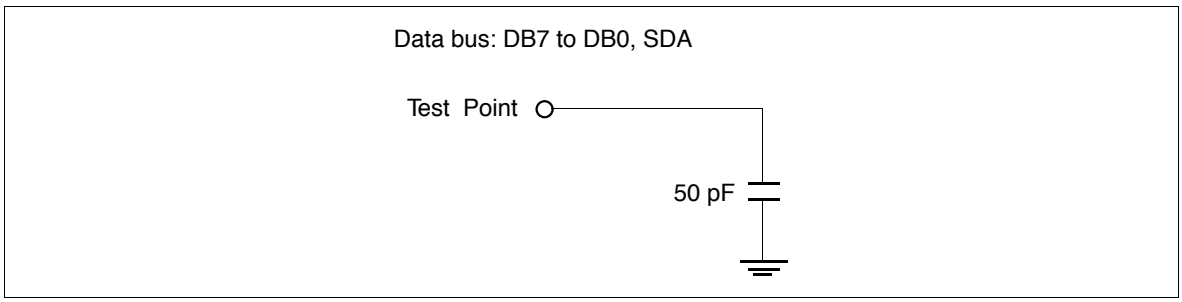
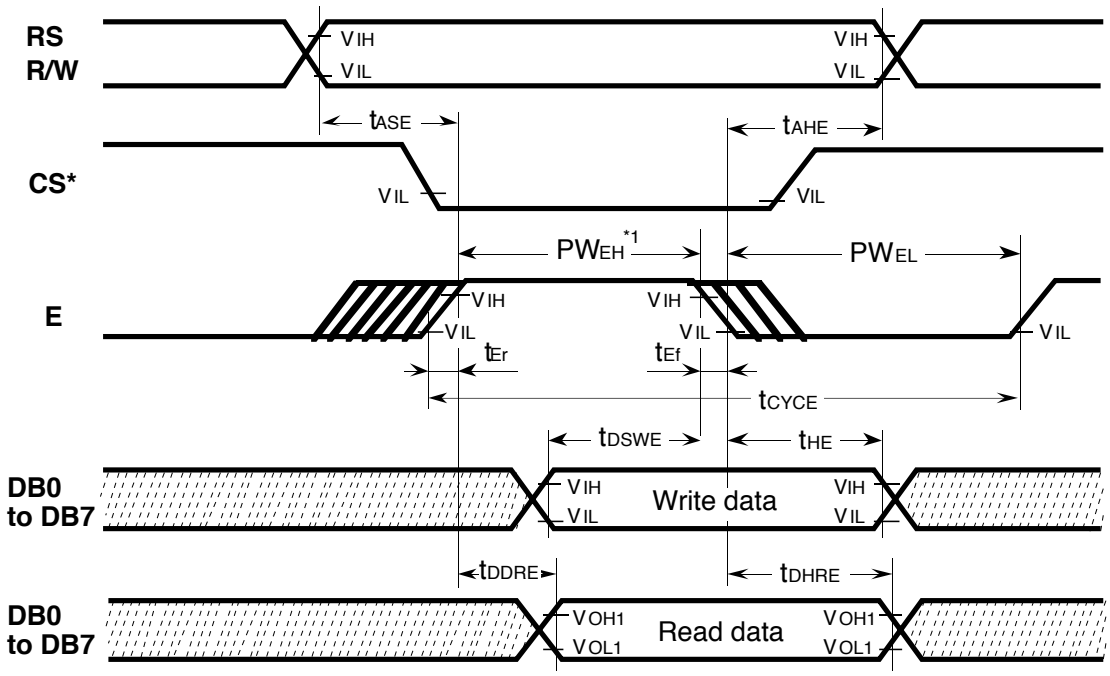


Figure 49 Load Circuit

Timing Characteristics

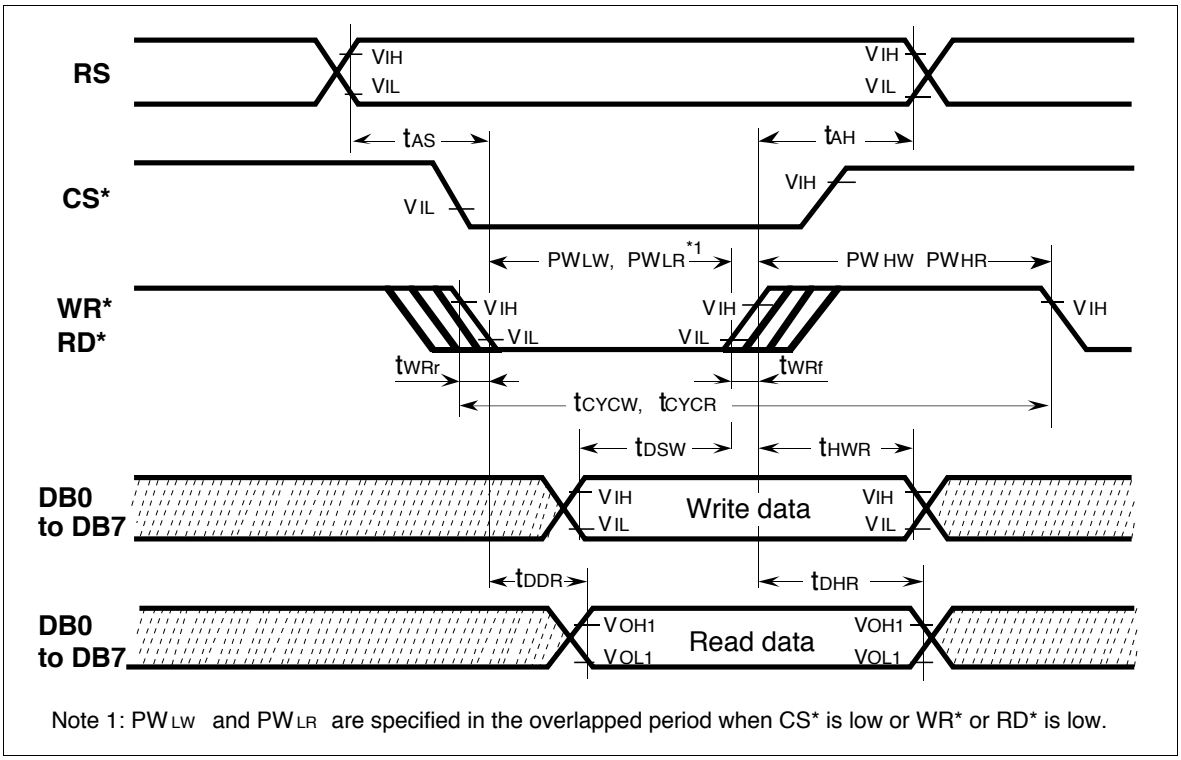
68-system Bus Operation



Note 1: PW_{EH} is specified in the overlapped period when CS* is low or E is high.

Figure 50 68-system Bus Timing

80-system Bus Operation



Note 1: PW_{LW} and PW_{LR} are specified in the overlapped period when CS* is low or WR* or RD* is low.

Figure 51 80-system Bus Timing

Clock-synchronized Serial Operation

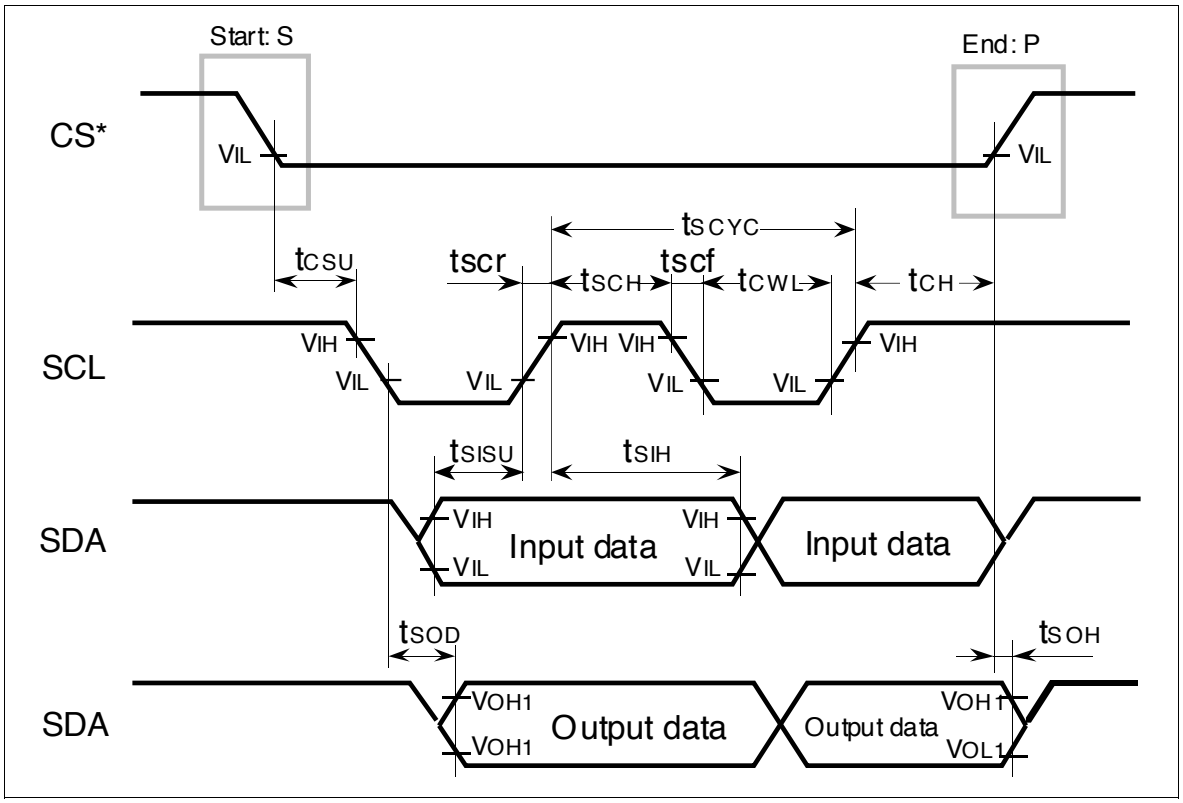


Figure 52 Clock-synchronized Serial Interface Timing

Reset Operation

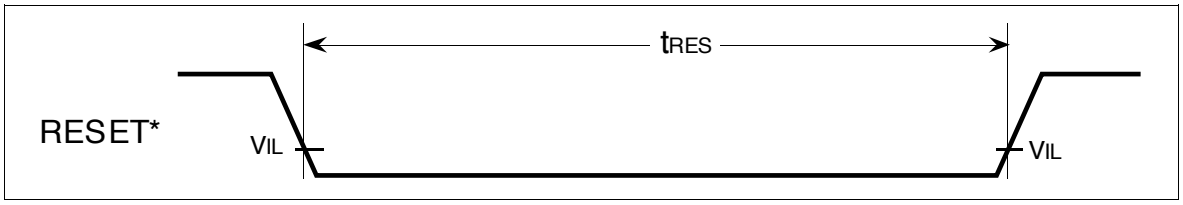
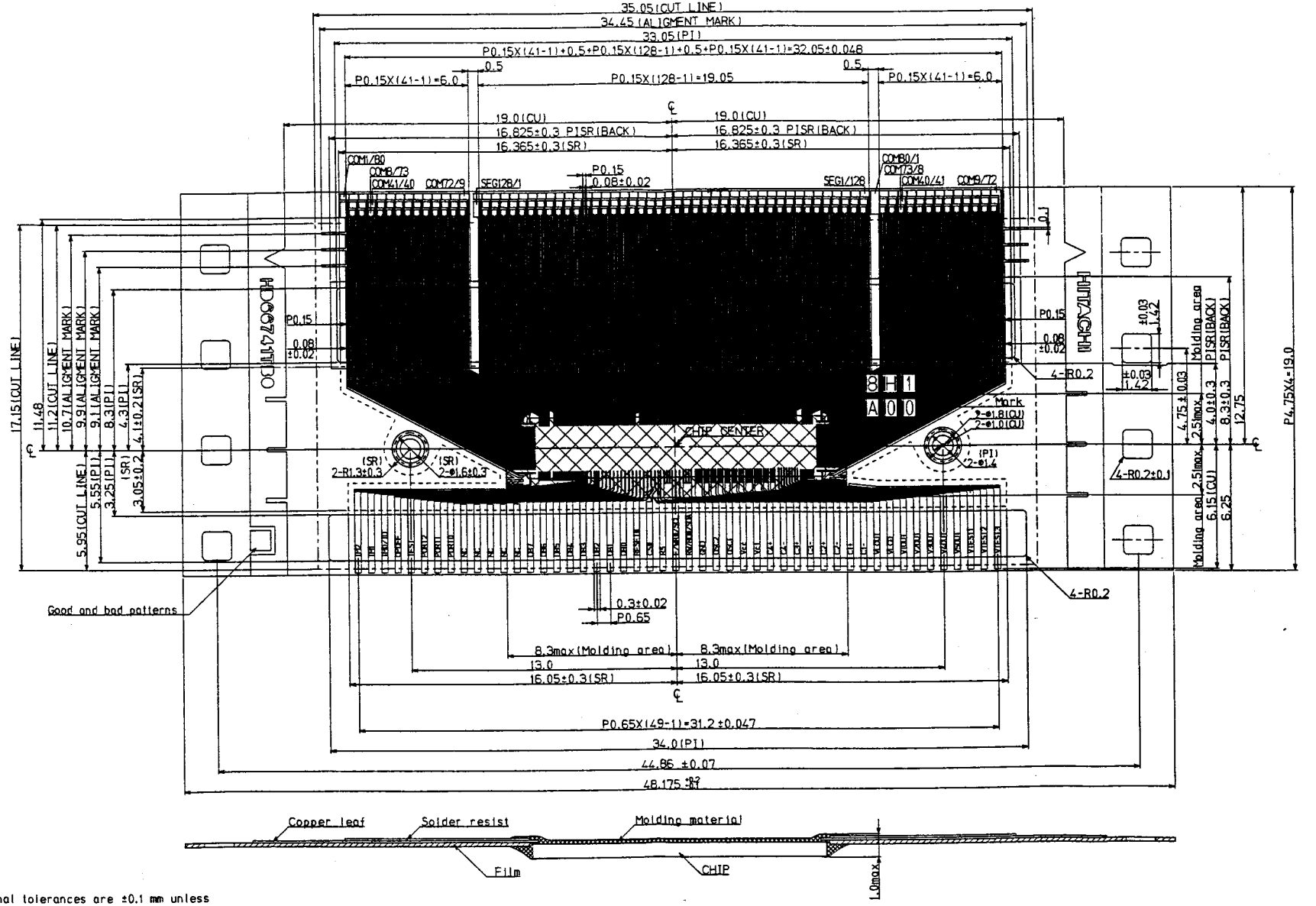


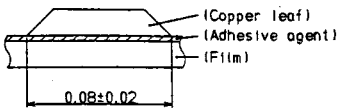
Figure 53 Reset Timing

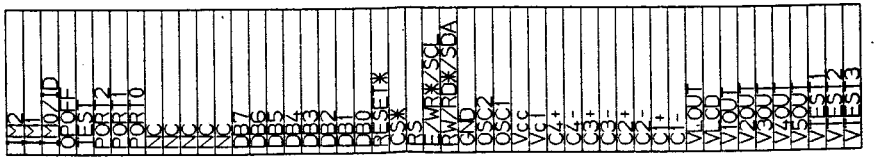


Notes: 1.Dimensional tolerances are ±0.1 mm unless otherwise noted.

2.See "Mark Description" regarding Mark Code.

3.The figure below shows a cross sectional view of the outer lead bonding area.





When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All right reserved: No one is permitted to reproduce or duplicated, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party of Hitachi, Ltd.
6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.