

# SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS040C – DECEMBER 1982 – REVISED FEBRUARY 1998

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Both Shift and Storage Registers
- High-Current Outputs Can Drive Up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

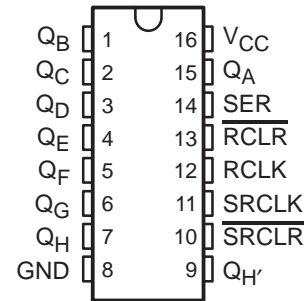
The 'HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ( $\overline{RCLR}$ ,  $\overline{SRCLR}$ ) inputs are provided on both the shift and storage registers. A serial ( $Q_{H'}$ ) output is provided for cascading purposes.

Both the shift register ( $RCLK$ ) and storage register ( $SRCLK$ ) clocks are positive edge triggered. If both clocks are connected together, the shift register is always one count pulse ahead of the storage register.

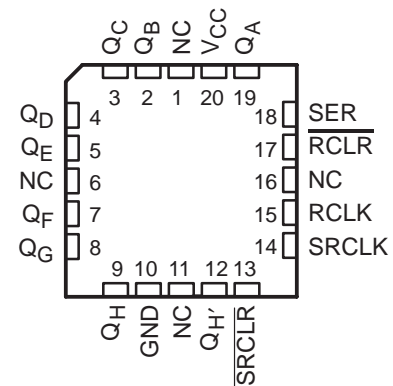
The parallel ( $Q_A$ – $Q_H$ ) outputs have high-current capability.  $Q_{H'}$  is a standard output.

The SN54HC594 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC594 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54HC594 . . . J OR W PACKAGE  
SN74HC594 . . . D, DB, OR N PACKAGE  
(TOP VIEW)



SN54HC594 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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 **TEXAS  
INSTRUMENTS**

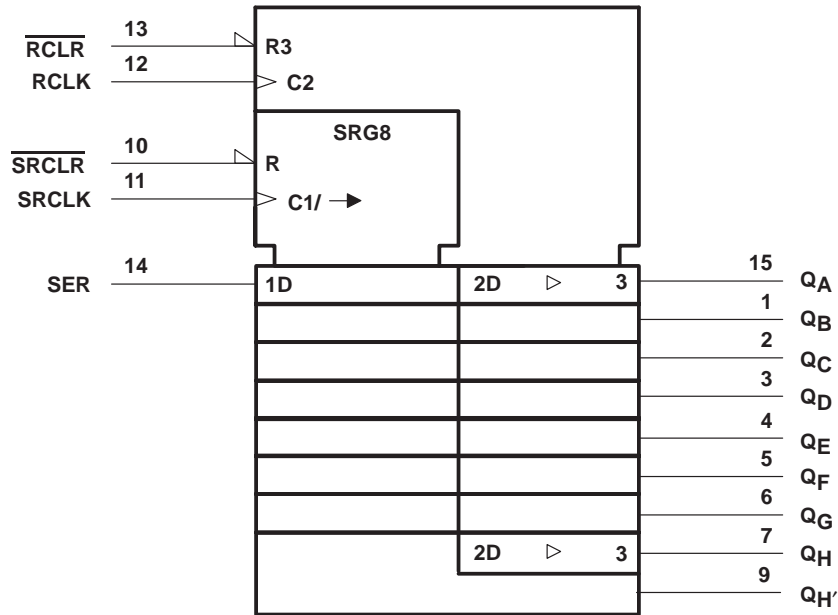
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# SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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## logic symbol†

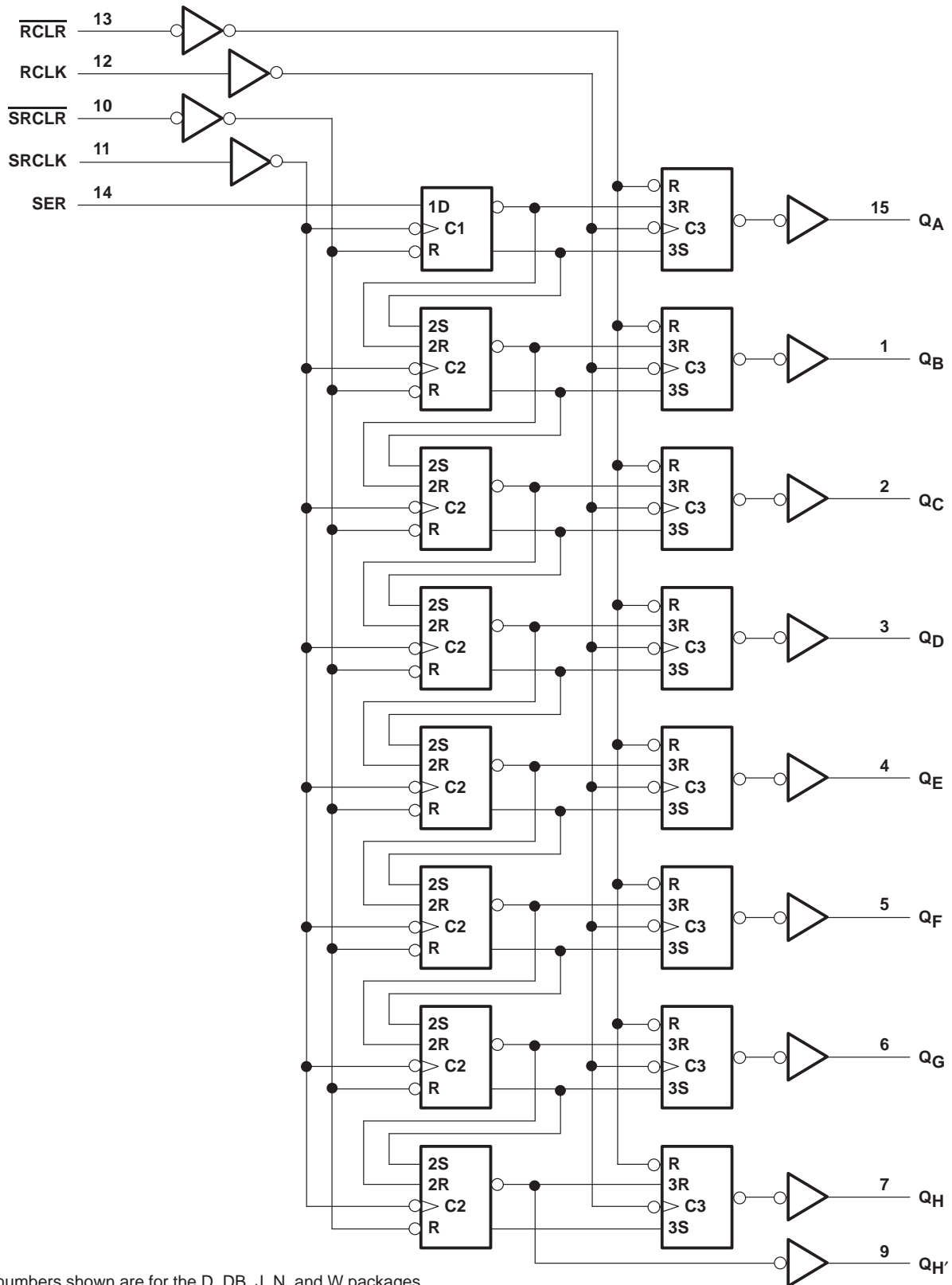


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, and W packages.

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## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and W packages.



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# SN54HC594, SN74HC594

## 8-BIT SHIFT REGISTERS

### WITH OUTPUT REGISTERS

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#### absolute maximum ratings over operating free-air temperature†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	113°C/W
DB package	131°C/W
N package	78°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

#### recommended operating conditions (see Note 3)

		SN54HC594			SN74HC594			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0	0.5	0	0.5	V
		$V_{CC} = 4.5$ V		0	1.35	0	1.35	
		$V_{CC} = 6$ V		0	1.8	0	1.8	
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V		0	1000	0	1000	ns
		$V_{CC} = 4.5$ V		0	500	0	500	
		$V_{CC} = 6$ V		0	400	0	400	
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54HC594, SN74HC594  
8-BIT SHIFT REGISTERS  
WITH OUTPUT REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		4.5 V	Q <sub>H'</sub> , I <sub>OH</sub> = -4 mA	3.98	4.3		3.7		3.84		
			Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -6 mA	3.98	4.3		3.7		3.84		
			Q <sub>H'</sub> , I <sub>OH</sub> = -5.2 mA	5.48	5.8		5.2		5.34		
6 V	Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OH</sub> = -7.8 mA	5.48	5.8		5.2		5.34				
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		4.5 V	Q <sub>H'</sub> , I <sub>OL</sub> = 4 mA		0.17	0.26		0.4		0.33	
			Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 6 mA		0.17	0.26		0.4		0.33	
			Q <sub>H'</sub> , I <sub>OL</sub> = 5.2 mA		0.15	0.26		0.4		0.33	
6 V	Q <sub>A</sub> -Q <sub>H</sub> , I <sub>OL</sub> = 7.8 mA		0.15	0.26		0.4		0.33			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0		6 V		±0.01	±0.5		±10		±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC594		SN74HC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	5		3.3		4		MHz
		4.5 V	25		17		20		
		6 V	29		20		24		
t <sub>w</sub>	SRCLK or RCLK high or low	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
	SRCLR or RCLR low	2 V	100		150		125		
		4.5 V	20		30		25		
		6 V	17		25		21		
t <sub>su</sub>	SER before SRCLK↑	2 V	90		135		110		ns
		4.5 V	18		27		22		
		6 V	15		23		19		
	SRCLK↑ before RCLK↑†	2 V	90		135		110		
		4.5 V	18		27		22		
		6 V	15		23		19		
	SRCLR low before RCLK↑	2 V	50		75		63		
		4.5 V	10		15		13		
		6 V	9		13		11		
	SRCLR high (inactive) before SRCLK↑	2 V	20		20		20		
		4.5 V	10		10		10		
		6 V	10		10		10		
	RCLR high (inactive) before SRCLK↑	2 V	5		5		5		
		4.5 V	5		5		5		
		6 V	5		5		5		
t <sub>h</sub>	Hold time, SER after SRCLK↑	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

† This setup time ensures the output register sees stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

# SN54HC594, SN74HC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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**switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			2 V	5	8		3.3		4	MHz	
			4.5 V	25	35		17		20		
			6 V	29	40		20		24		
$t_{pd}$	SRCLK	$Q_H'$	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
	RCLK	$Q_A-Q_H$	2 V		50	150		225		185	
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
$t_{PHL}$	$\overline{\text{SRCLR}}$	$Q_H'$	2 V		50	150		225		185	ns
			4.5 V		20	30		45		37	
			6 V		15	25		38		31	
	$\overline{\text{RCLR}}$	$Q_A-Q_H$	2 V		50	125		185		155	
			4.5 V		20	25		37		31	
			6 V		15	21		31		26	
$t_t$		$Q_H'$	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	
		$Q_A-Q_H$	2 V		38	60		90		75	
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

**switching characteristics over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC594		SN74HC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	RCLK	$Q_A-Q_H$	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
$t_{PHL}$	$\overline{\text{RCLR}}$	$Q_A-Q_H$	2 V		90	200		300		250	ns
			4.5 V		23	40		60		50	
			6 V		19	34		51		43	
$t_t$		$Q_A-Q_H$	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load	395	pF

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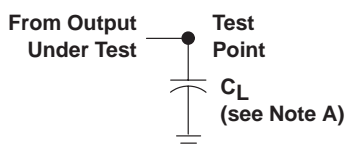


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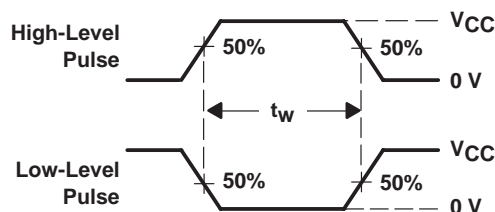
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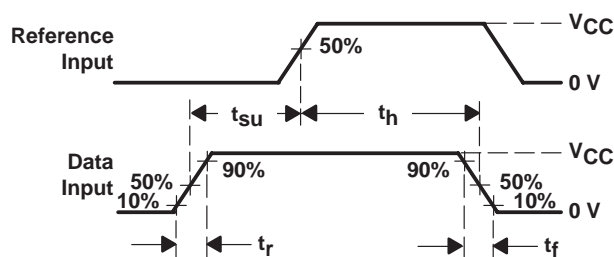
## PARAMETER MEASUREMENT INFORMATION



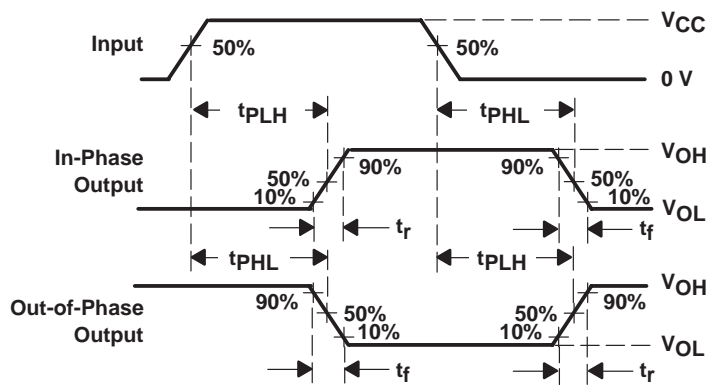
LOAD CIRCUIT



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - $t_f$  and  $t_r$  are the same as  $t_t$ .

Figure 1. Load Circuit and Voltage Waveforms

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## SN74HC594, 8-Bit Shift Registers With Output Registers

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74HC594
Voltage Nodes (V)	6, 5, 2
Vcc range (V)	2.0 to 6.0
Input Level	CMOS
Output Level	CMOS
Output Drive (mA)	-4/4
Output	2S
Clear	Async

### FEATURES

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- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
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- Independent Clocks for Both Shift and Storage Registers
- High-Current Outputs Can Drive Up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

### DESCRIPTION

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The 'HC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (RCLR\, SRCLR\) inputs are provided on both the shift and storage registers. A serial ( $Q_H$ ) output is provided for cascading purposes.

Both the shift register (RCLK) and storage register (SRCLK) clocks are positive edge triggered. If both clocks are connected together, the shift register is always one count pulse ahead of the storage register.

The parallel ( $Q_A - Q_H$ ) outputs have high-current capability.  $Q_H$  is a standard output.

The SN54HC594 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC594 is characterized for operation from -40°C to 85°C.

#### **TECHNICAL DOCUMENTS**

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#### **DATASHEET**

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Full datasheet in Zipped PostScript: [scls040c.psz](#) (151 KB)

#### **APPLICATION NOTES**

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- [Designing With Logic](#) (SDYA009C - Updated: 06/01/1997)
- [HCMOS Design Considerations](#) (SCLA007 - Updated: 04/01/1996)
- [Implications of Slow or Floating CMOS Inputs](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [SN54/74HCT CMOS Logic Family Applications And Restrictions](#) (SCLA011 - Updated: 05/01/1996)
- [Using High Speed CMOS and Advanced CMOS In Systems With Multiple Vcc](#) (SCLA008 - Updated: 04/01/1996)

#### **RELATED DOCUMENTS**

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- [Documentation Rules \(SAP\) And Ordering Information](#) (SZZU001B, 4 KB - Updated: 05/06/1999)
- [Logic Selection Guide Second Half 2000](#) (SDYU001N, 5035 KB - Updated: 04/17/2000)
- [MicroStar Junior BGA Design Summary](#) (SCET004, 167 KB - Updated: 07/28/2000)
- [More Power In Less Space - Technical Article](#) (SCAU001A, 850 KB - Updated: 03/01/1996)

#### **PRICING/AVAILABILITY**

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<u>ORDERABLE DEVICE</u>	<u>PACKAGE</u>	<u>PINS</u>	<u>TEMP (°C)</u>	<u>STATUS</u>	<u>BUDGETARY PRICE US\$/UNIT QTY=1000+</u>	<u>PACK QTY</u>	<u>PRICING/AVAILABILITY</u>
SN74HC594DR	<u>D</u>	16		ACTIVE	1.97	2500	<a href="#">Check stock or order</a>
SN74HC594DW	<u>DW</u>	16	-40 TO 85	ACTIVE	1.97	40	<a href="#">Check stock or order</a>
SN74HC594DWR	<u>DW</u>	16	-40 TO 85	ACTIVE	2.04	2000	<a href="#">Check stock or order</a>
SN74HC594N	<u>N</u>	16	-40 TO 85	ACTIVE	1.97	25	<a href="#">Check stock or order</a>

**Table Data Updated on: 11/16/2000**

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