Philips Components–Signetics

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Memory Products	

100149B
1K-bit ECL bipolar PROM

DESCRIPTION

The 100149B is field programmable, meaning that custom patterns are immediately available by following the Signetics Generic IV Programming procedure. The device is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the TiW link matrix.

The 100149B is suitable for use in high-performance ECL systems. The outputs are capable of driving 50Ω loads.

A Chip Enable input is provided for ease of memory expansion.

Ordering information can be found on the following page.

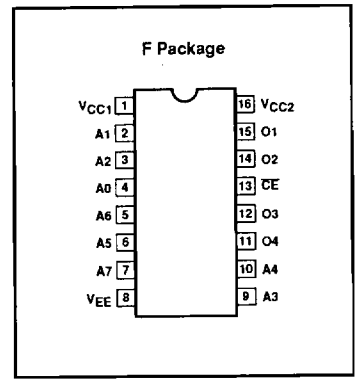
FEATURES

- Address access time: 5ns max
- Power dissipation: 0.66mW/bit typ
- High-impedance inputs (50KΩ pulldown)
- One Chip Enable input
- Open Emitter outputs (50Ω drive)
- On-chip address decoding
- No separate fusing pins
- Fully compatible with ECL 100K series

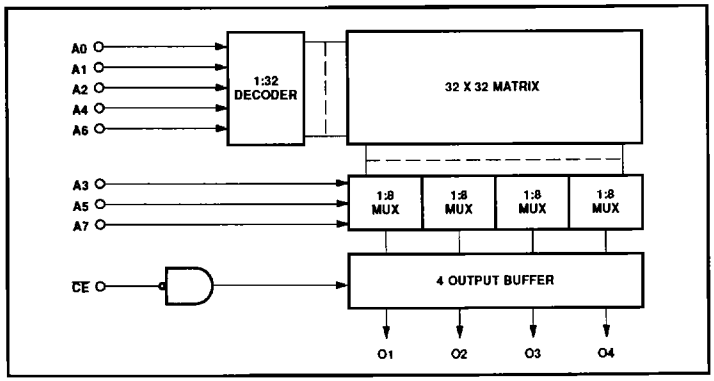
APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



LOGIC DIAGRAM



1K-bit ECL bipolar PROM (256 × 4) 100149B

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic Dual-In-Line 300mil-wide	100149B F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage (V_{CC} = 0)	-8	V_{DC}
V_{IN}	Input voltage (V_{CC} = 0)	0 to -3	V_{DC}
I_O	Output source current	40	mA_{DC}
T_{amb}	Operating temperature range	-0 to +75	°C
T_{stg}	Storage temperature range	-55 to +165	°C

DC ELECTRICAL CHARACTERISTICS

0°C ≤ T_{amb} ≤ +75°C, -4.275V ≤ V_{EE} ≤ -4.725V

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			MIN	TYP[4]	MAX	
Input voltage						
V_{IL}	Low		-1.810			V
V_{IH}	High				-0.880	V
V_{ILA}	Threshold Low				-1.475	V
V_{IHA}	Threshold High		-1.165			V
Output voltage						
V_{OL}	Low	V_{IL} = Min	-1.810		-1.620	V
V_{OH}	High	V_{IH} = Max	-1.025		-0.880	V
V_{OLA}	Threshold Low	V_{IL} = Max			-1.610	V
V_{OHA}	Threshold High	V_{IH} = Min	-1.035			V
Input current[5]						
I_{IL}	Low	V_{IL} = Min	0.5			µA
I_{IH}	High	V_{IH} = Max			220	µA
Supply current						
I_{EE}		V_{EE} = -4.5V		150	160	mA

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Each ECL 100K series device has been designed to meet the DC specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to -2V.
3. For current measurements, maximum is defined as the maximum absolute value.
4. Typical values are at V_{EE} = -4.5V, T_{amb} = +25°C.
5. Unused inputs must have 10KΩ minimum to V_{EE} or be connected to $-2V_{DC}$.

1K-bit ECL bipolar PROM (256 × 4) 100149B

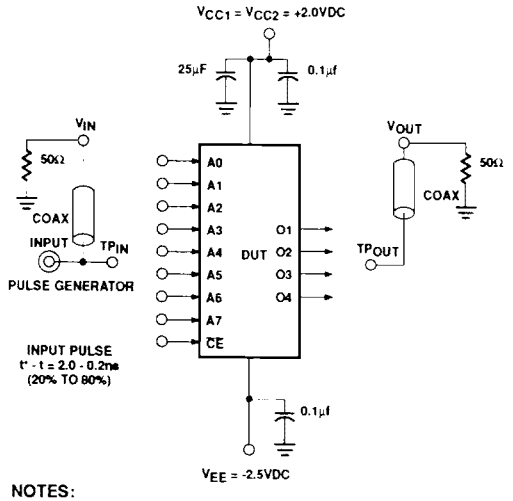
AC ELECTRICAL CHARACTERISTICS

$R_1 = 50\Omega$, $0°C \leq T_{amb} \leq +75°C$, $-4.275V \leq V_{EE} \leq -4.725V$

SYMBOL	PARAMETER	TO	FROM	LIMITS MIN	LIMITS TYP[1]	LIMITS MAX	UNIT
Access time							
t_{AA}		Output	Address			5	ns
t_{CE}		Output	Chip Enable		2	3	ns
Disable time							
t_{CD}		Output	Chip Disable		2	3	ns
Rise and fall time							
t^+	Rise time (20-80%)				2.0		ns
t^-	Fall time (80-20%)				2.0		ns

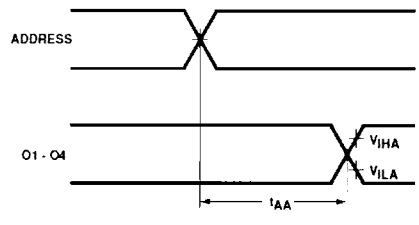
NOTES:
1. Typical values are at $V_{EE} = -4.5V$, $T_{amb} = +25°C$.

TEST LOAD CIRCUIT

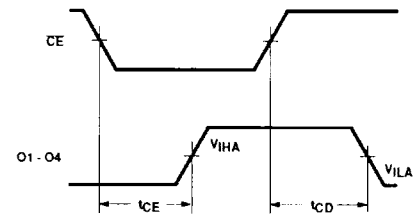


NOTES:
1. For AC tests, all input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin. A 50Ω termination to ground is located in each scope input. Unused outputs are connected to a 50Ω resistor to ground.
2. Test procedures are shown for only one input or set of input conditions. Other inputs are tested in the same manner.
3. Normal practice in test fixtures layout should be followed. Lead lengths, particularly to the power supply, should be as short as posstble. A 10µF capacitor between V_{CC1} and V_{CC2} terminals, located as close to the device as possible, is recommended to reduce ringing.

VOLTAGE WAVEFORMS



Address Access Time



Chip Enable/Disable Propagation Delays