NEC
NEC Electronics Inc.

μPD7003
8-BIT CMOS HIGH-SPEED A/D CONVERTER

Description

The μPD7003 is a high speed, high performance, low power, 8-bit analog-to-digital Converter designed to be easily interfaced to the 8080 and 8086, 8- and 16-bit microprocessors. Using the parallel conversion technique, the μPD7003 features a conversion speed of 4 μs and eliminates the need of sample and hold circuits in most applications. The μPD7003 is also capable of running under DMA control using a DMA controller such as the μPD8257. Available in a 24-pin ceramic/plastic DIP, the μPD7003 is the ideal converter for high speed 8-bit designs.

Features

- High speed conversion (250 k samples/sec. max.)
- Input consists of 255/1 matched autozeroed comparators
- No missing codes over temperature range
- Linearity ±1.25 LSB max.
- Three-state outputs
- Overrange output
- Operates from single −5 V supply
- Low power consumption (50 mW)

Ordering Information

Part Number	Package	Operating Temperature Range
μPD7003C	Plastic DIP	−20°C to −70°C
μPD7003D	Ceramic DIP	−20°C to −80°C

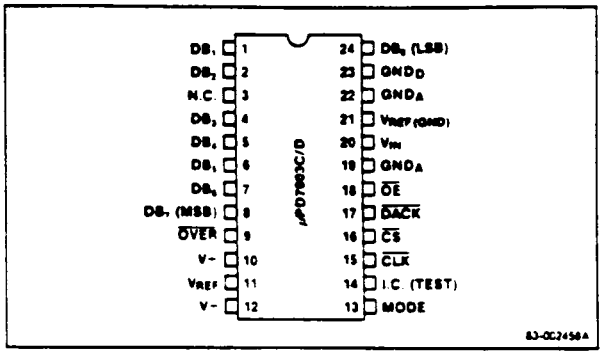
Absolute Maximum Ratings

T_A = 25°C

Operating Temperature, C Package	−20 to −70°C
Operating Temperature, D Package	−20 to −70°C
Storage Temperature	−65 to −125°C
All Input Voltages	−0.3 to V− +0.3 V
Power Supply	−0.3 to −7 V
Power Dissipation	300 mW
Analog GND Voltage	±0.3 V

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Pin Identification

Pin	Name	Function
1	DB_1	7th bit output
2	DB_2	6th bit output
3	NC	Non connection
4	DB_3	5th bit output
5	DB_4	4th bit output
6	DB_5	3th bit output
7	DB_6	2th bit output
8	DB_7	MSB output
9	$\overline{OVER}$	Overrange output
10	V−	Power supply (−5 V)
11	V_{REF}	Reference voltage input (positive)
12	V−	Power supply (−5 V)
13	MODE	MODE control (note 1)
14	TEST	Low: Device test (used for inspecting the device) High: Conversion
15	$\overline{CLK}$	Low: Previous data output High: Quantizing
16	$\overline{CS}$	Chip select
17	$\overline{DACK}$	DMA Acknowledge
18	$\overline{OE}$	Low: Data output High: High impedance
19	AGND	Analog ground
20	V_{IN}	Voltage input
21	$V_{REF(GND)}$	GND for V_{REF}
22	AGND	Analog ground
23	GND	Digital ground
24	DB_0 (LSB)	LSB

Pin Identification (Cont.)

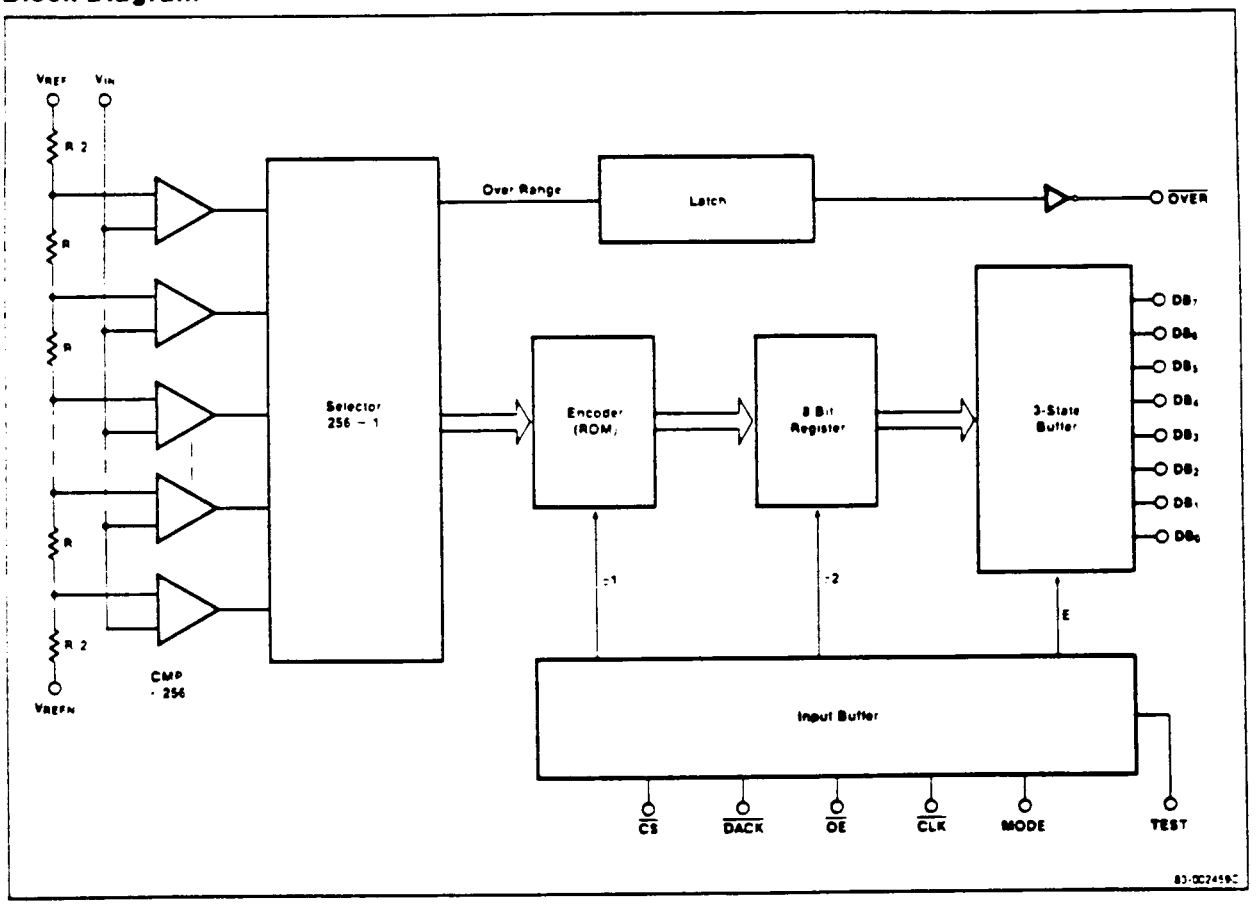
Pin	Name	Function
19	GND_A	Analog ground
20	V_{SIN}	Analog input
21	V_{REFN}	Reference voltage input (negative) (Note 2)
22	GND_A	Analog ground
23	GND_D	Digital Ground
24	DB0	LSB output

Notes: 1.

Inputs		8-Bit Register
Mode	$\overline{OE}$	
1	1	Data refreshed with every $\overline{CONV}$ ↓
	0	
0	1	
	0	No change

2. Tie to the analog ground unless external zero adjustment required.

Block Diagram



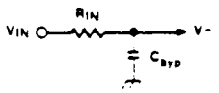
DC Characteristics

$T_A = +25°C$, $V- = V_{REF} = 5.0 \pm 0.25$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Power Supply Current	I_{CC}		6.0	18.0	mA	$t_{CY} = 4.0\ \mu s$, $t_{WLC} = 2.0\ \mu s$ Note 1
High Level Output Voltage	V_{OH}	2.8			V	$I_O = -2.0$ mA
Low Level Output Voltage	V_{OL}			0.4	V	$I_O = -1.0$ mA
Digital Input Leakage Current	I_{ILK}		1	10	μA	$0\ V \le V_{IN} \le V-$
Digital Output Leakage Current	I_{OLK}		1	10	μA	$0\ V \le V_O \le V-$
Reference Input Current	I_{REF}	1.19	1.79	3.57	mA	$\overline{CLK}$ = H or L Note 1
Analog Input Resistance	R_{IN}	1	35		kΩ	$V_{EN} = 2.5$ V, $t_{CY} = 4\ \mu s$, $t_{WLC} = 2\ \mu s$ Note 2
Reference Input Capacitance	C_{REF}		100		pF	$f_{clk} = 1$ MHz; unmeasured pins returned to Ground
Analog Input Capacitance	C_{IN}		100		pF	$f_{clk} = 1$ MHz; unmeasured pins returned to Ground
Power Dissipation	P_D			50	mW	$t_{CY} = 4.0\ \mu s$, $t_{WLC} = 2.0\ \mu s$

Notes: 1. This means DC current. Tie the bypass capacitors (electrolytic capacitor ≥ 10 μF, ceramic capacitor ≈ 0.01 μF) to V− and V_{REF} pins, in order to absorb rush current (≈ 10 mA).

2. DC input equivalent circuit is shown below.



Tie the bypass capacitor (> 0.01 μF) to the analog input pin. 3 mA peak current flows into this pin.

AC Characteristics

$T_A = 25 \pm 2°C$, $V- = 5.0$ V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Output Delay Time	t_{DEO}		100	350	ns	$\overline{OE}$ ↓ — DO
	t_{DCO}		150	450	ns	$\overline{CONV}$ ↓ — DO
	t_{DSO}		100	350	ns	$\overline{CS}$ ↓ — DO
	t_{DCOVR}		100	350	ns	$\overline{CONV}$ ↑ — $\overline{OVER}$
Delay Time to Floating	t_{FEO}		70	200	ns	$\overline{OE}$ ↑ — DO
	t_{FSO}		150	450	ns	$\overline{CS}$ ↑ — DO

Conversion Characteristics

$T_A = 25 \pm 2°C$, $V- = V_{REF} = 5.0$ V;
$t_{CY} = 4.0\ \mu s$; $t_{WLC} = 2.0\ \mu s$

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Resolution	RES	8	8	8	Bits	−20°C to +80°C
Nonlinearity	NL			±1.25	LSB	
Full Scale Error				±1.00	LSB	
Full Scale Error Temperature Coefficient			20		ppm/°C	
Zero Scale Error		−0.75		+0.75	LSB	
Zero Scale Error Temperature Coefficient			20		ppm/°C	

Note: μPD7003C $T_A = 0°C$ to $+70°C$.

Recommended Operating Conditions

T_A = 0°C to 70°C: μPD7003C,
T_A = −20°C to +80°C: μPD7003D

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Supply Voltage	V−	4.75	5.0	5.25	V	
Reference Input Voltage	V_{REF}	4.0	V−	V−	V	
Analog Input Voltage	V_{IN}	−0.1		V− +0.1	V	
High Level Logic Input	V_{IH}	2.4		V−	V	
Low Level Logic Input	V_{IL}	−0.1		0.8	V	
Sampling Rate		10		250k	times/s	
Conversion Cycle Time	t_{CY}	4.0		100	μs	
$\overline{CONV}$ High Level Width	t_{WHC}	2.0			μs	
$\overline{CONV}$ Low Level Width	t_{WLC}	2.0			μs	
$\overline{CONV}$ Setup Time	t_{SCE}	0		Note 1	ns	$\overline{CONV}$ ↓ − $\overline{OE}$ ↓
$\overline{CS}$ Setup Time	t_{SSE}	100			ns	$\overline{CS}$ ↓ − $\overline{OE}$ ↓
$\overline{CS}$ Hold Time	t_{HES}	0			ns	$\overline{OE}$ ↑ − $\overline{CS}$ ↑
$\overline{OE}$ Setup Time	t_{SEC}	600			ns	$\overline{OE}$ ↓ − $\overline{CONV}$ ↓
$\overline{OE}$ Hold Time	t_{HCE}	400			ns	$\overline{CONV}$ ↑ − $\overline{OE}$ ↓
$\overline{OE}$ Low Level Width	t_{WLE}	400		Note 2	ns	
Digital Input Rise and Fall Time	t_r, t_f			50	ns	

Notes: 1 t_{SCE} (ns) ≤ t_{CY} (ns) − t_{WLE} (ns) − 100 (ns).
2 t_{WLE} (ns) ≤ t_{CY} (ns) − t_{SCE} (ns) − 100 (ns)

Converter Operation

Referring to the block diagram, the reference voltage is set externally to some desired level which references the individual internal components such that V_{REF} is divided equally by 256 resistors in a ladder/divider configuration. The applied voltage to V_{IN} is then compared to the reference level and the individual samples are sent to the selector section where the individual signals are multiplexed to form an address data word. The data word is then further encoded to form the final 8-bit data byte by the encoder ROM, and stored in the 8-bit register until the Output Enable Command. Then the data is sent to the data bus via a three-state buffer.

Mode Select

There are two modes of operation for the μPD7003. Figure 1 shows the timing diagram for mode "0" where the converter is operating in continuous output mode. The analog input is sampled when the clock is in the "low" state. When the clock is in the "high" state the conversion from analog-to-digital takes place and the resultant data is output on the next falling edge of the clock pulse and the cycle is repeated.

The second mode (Mode 1) is shown in figure 2. In this mode of operation, one conversion takes place while the clock is in the "low" state and the resultant data is held as long as output enable and Chip Select ($\overline{CS}$) or DMA Acknowledge ($\overline{DACK}$) are "low." Data refresh is inhibited until $\overline{CS}$ and $\overline{DACK}$ are recycled.

MODE = "HIGH"

Data is refreshed on the falling edge of $\overline{CLK}$, loaded during the "low" clock state, and converted and output during the "high" clock state.

MODE = "LOW"

Data is loaded and converted when Output Enable is "low" and refreshed only when $\overline{OE}$ makes the transition from high to low again.

Note that in either case data will only be accepted and output when $\overline{OE}$ and $\overline{CS}$ or $\overline{DACK}$ are active ("low"). Output enable should not be changed during the intervals shown in figure 3. The timing for output enable change versus clock transition is 600 ns before and 500 ns after the rising or falling edge of $\overline{CLK}$ any attempt to change $\overline{OE}$ during these periods will be inhibited.

Timing Waveforms

Figure 1. (MODE;0)

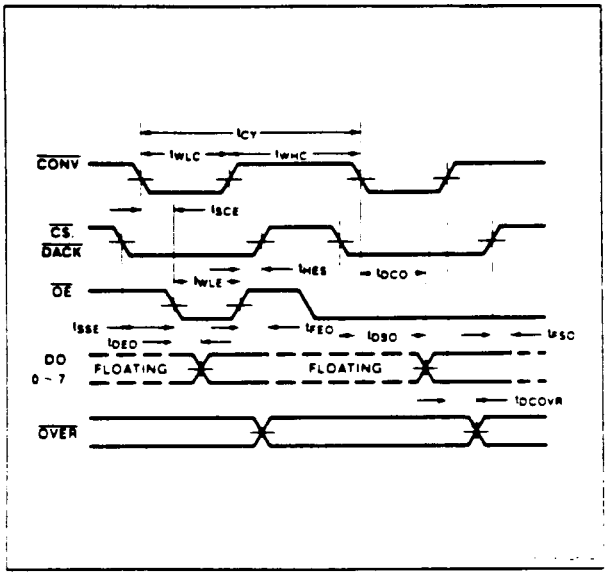


Figure 2. (MODE;1)

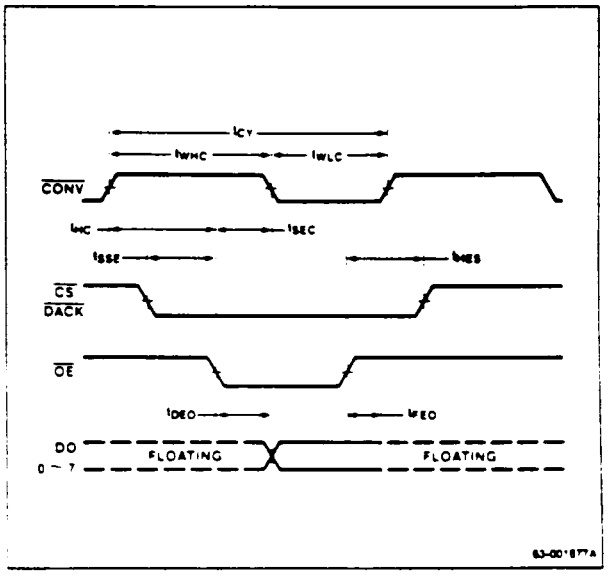


Figure 3. Timing Chart