

**33 x 32 1.25 GBIT/S DIFFERENTIAL CROSSPOINT SWITCH** **S2028**

**FEATURES**

- 33 x 32 differential crosspoint switch
- Full broadcast switching capability
- Differential 10K PECL data path
- Configurable differential output driver controls
- Up to 1.25 Gbit/s NRZ data rate
- TTL configuration controls
- Reconfigurable without disturbing operation
- Single cycle broadcast configuration
- High-speed multicast and fast unicast configuration (100 MHz)
- “Break” feature to disable previous multicast configuration
- 224-pin LDCC package

**APPLICATIONS**

- Internet Switches
- Datacom or telecom switching
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Digital video

**GENERAL DESCRIPTION**

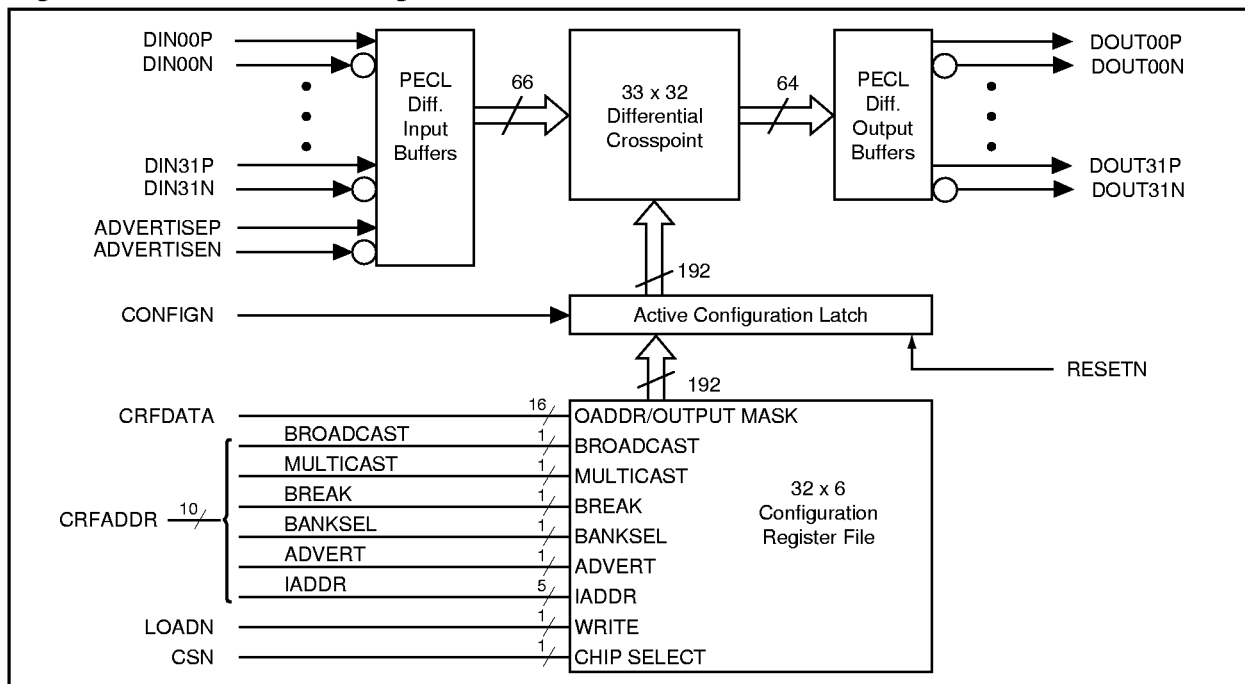
The S2028 is a very high-speed 33 x 32 differential crosspoint switch with fast multicast and broadcast capabilities. It consists of 32 differential PECL input signal pairs that can be connected to any or all of its 32 differential PECL output signal pairs. In addition, the differential output drivers can be individually configured to gate in an additional broadcast channel. This channel can be used as a default advertise channel, or to supply a signal such as a clock to simplify interface design.

Along with a single cycle reconfiguration of the entire 33 x 32 crosspoint switch, the S2028 features single cycle broadcast and fast two cycle multicast configuration. A “break” feature allows fast unicast or multicast disable of the previous configuration.

The S2028 contains a unique memory map, which provides full support of the broadcast, multicast, and unicast modes.

The differential 10K PECL logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure, to minimize data distortion and to handle NRZ data rates up to 1.25 gigabits per second.

**Figure 1. Functional Block Diagram**



TTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2028 can be completely reconfigured in only 10 ns without disturbing switch operations.

The configuration register can also be put into transparent mode, reconfiguring all addressed outputs within 10ns after the LOADN signal goes low.

### Data Transfer

For each configured connection between a differential input pair and an enabled output pair, any data appearing at the input pair and switching at up to 1.25 Gb/s will be passed immediately through to the output pair.

### Configuration

The S2028 can be selectively reconfigured one output channel at a time in unicast mode, 16 output channels at a time in multicast mode, and all 32 output channels simultaneously in broadcast mode. Any number of output channels can be reconfigured simultaneously using the CONFIGN control. Configuration data is stored in all 32 registers, one register for each output channel. As shown in Figure 1, the configuration data is passed in parallel from all 32 registers to a bank of latches which hold the active switch configuration. This two-state arrangement allows any number of output channels to be reconfigured simultaneously.

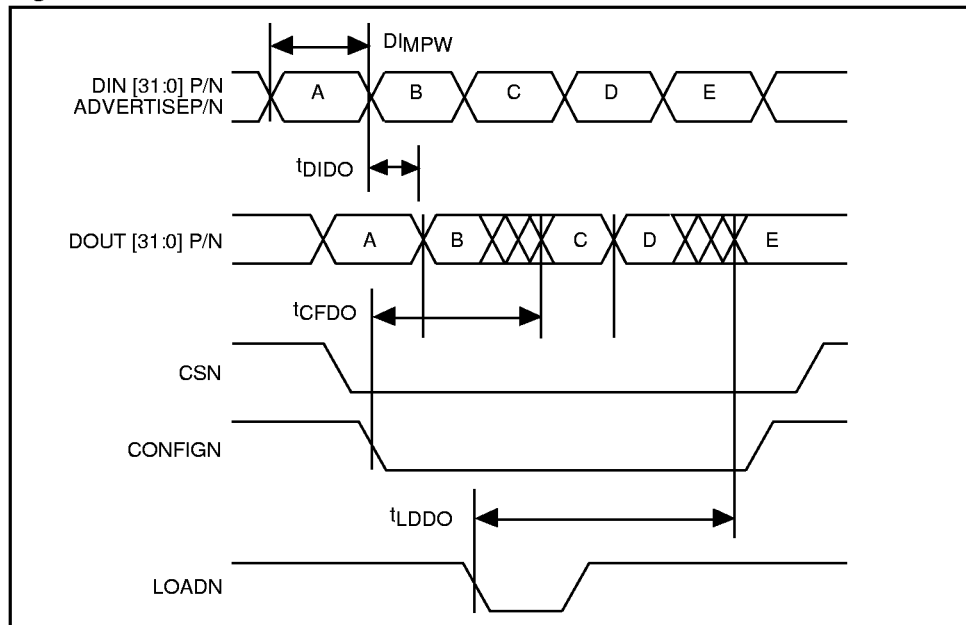
Each output configuration register holds 6 bits. Five bits are used to select which input channel will be connected to the output channel, and one bit is used to override the input address and instead channel the ADVERTISEP/N input to that output.

The S2028A 33 X 32 Crosspoint Switch interface is designed to connect directly to a microprocessor's address and data bus and R/W signal. A CS input (CSN) is provided to simplify interfacing to the microprocessor's address bus. Most of the device's functions can be programmed by a single instruction in firmware. See the memory map in Figure 3. The memory map depends on the hardware interface, and can be mapped to any 1024 byte address range. In general, the address bus will specify the crosspoint switch input channel, and the data bus will specify the crosspoint switch output channel. The microprocessor or host hardware presents the address and data to the S2028A, the decoder logic enables CSN, and then the microprocessor strobes the Read/Write\* signal (LOADN). (See Figure 2.)

### Broadcast Mode

Writing to any address in the Broadcast Address Space (512-1023) will broadcast the input channel specified on the address bus (IADDR) to all 32 output channels. If the ADVERT bit is set to a 1, IADDR is ignored and the ADVERTISE input is broadcast to all 32 output channels. Broadcasting is a single cycle operation, and does not require strobing of CONFIGN.

**Figure 2. Data Transfer Waveforms**



### Multicast Mode

In Multicast Mode, a group of 16 output channels can be configured to connect to one input channel in a single cycle. There are two output channel groups, so all 32 output channels can be configured in two cycles. Each group has its own address range. Group 0 configures output channels 0-15 while Group 1 configures output channels 16-31. Each bit of the 16 bit data bus (CRFDATA) specifies which of the 16 output channels in the group are to be configured to connect to the input channel.

The address bus IADDR specifies the input channel, and the ADVERT input specifies whether to override that input channel with the ADVERTISEP/N input. The BANKSEL bit specifies which of the two sets of 16 output channels is being addressed. For example, if the address bus contains "0101011001" and the data bus contains "01000110 10101100", then output channels 18, 19, 21, 23, 25, 26 and 30 are configured for connection to input channel 25. If the address bus contains "0101111001" and the data bus is unchanged, then output channels 18, 19, 21, 23, 25, 26 and 30 are configured for connection to the ADVERTISEP/N input.

The Multicast Address Range is from 256-511. Writing to address range 256-383 will maintain the prior configuration for a particular channel, if that channel's output mask bit is set to a "0". The address range 384-511 activates the "break" feature of the S2028A 33X32 Crosspoint Switch. In this mode, for each output channel whose mask bit is set to 0, if the prior configured input channel matches the new requested input channel, the prior configuration is broken and the ADVERTISE input is connected to that output.

### Unicast Mode

Writing to the Unicast Address Range (0-255) will configure the input channel specified on the address bus (IADDR) to connect to the output channel specified on the lower 5 bits of the data bus (OADDR). However, if the ADVERT bit is set to a 1, IADDR is ignored and the output channel OADDR is configured to connect to the ADVERTISEP/N input.

Writing to Address Range 0-127 will maintain the prior configuration for a particular channel, if that channel's output mask bit is set to a "0". The address range 128-255 activates the "break" feature. In this mode, for each output channel whose mask bit is set to 0, if the prior configured input channel matches the new requested input channel, the prior configuration is broken and the ADVERTISE input is connected to that output.

### Reconfiguration

When the differential switch is to be reconfigured, the S2028A minimizes the time required through the use of an active configuration latch. While the switch is operational, and prior to the time at which it must be reconfigured, a new configuration can be loaded into the output pair configuration registers. Once the 32 output pair configuration registers contain the desired connection and output pair driver control information, the contents of the registers are transferred in parallel to the active configuration latch by the CONFIGN strobe. This allows multiple connections to be simultaneously changed. Broadcast mode is a single cycle operation and does not require strobing CONFIGN.

The configuration latch can be made transparent by tying the CONFIGN input to a logic 0. When this is done, changes strobed into the output pair configuration registers by the LOADN input will be passed immediately to the switch.

### Reset Behavior

When the RESETN input is asserted, the S2028A assumes a configuration where the ADVERTISEP/N channel is broadcast to all of the differential output drivers. Individual output drivers then remain in this state after RESETN is deasserted, until they are explicitly reconfigured to a new input address.



**Table 1. Pin Assignment and Descriptions**

Pin Name	Level	I/O	Pin #	Description
DIN31P	Diff. PECL	Input Pairs	54	Input data. Differential. Can be used as single-ended input pairs with $V_{BB}$ tied to one side of each differential pair.
DIN31N			55	
DIN30P			115	
DIN30N			114	
DIN29P			51	
DIN29N			52	
DIN28P			118	
DIN28N			117	
DIN27P			47	
DIN27N			49	
DIN26P			122	
DIN26N			120	
DIN25P			46	
DIN25N			48	
DIN24P			125	
DIN24N			124	
DIN23P			44	
DIN23N			45	
DIN22P			127	
DIN22N			126	
DIN21P			42	
DIN21N			43	
DIN20P			131	
DIN20N			129	
DIN19P			38	
DIN19N			41	
DIN18P			134	
DIN18N			130	
DIN17P			35	
DIN17N			36	
DIN16P			141	
DIN16N			140	
DIN15P	21			
DIN15N	22			
DIN14P	143			
DIN14N	142			
DIN13P	17			
DIN13N	19			
DIN12P	146			
DIN12N	145			
DIN11P	16			
DIN11N	15			
DIN10P	150			
DIN10N	148			
DIN9P	14			
DIN9N	13			
DIN8P	154			
DIN8N	153			

Note: Cavity up counter clockwise pin numbering orientation. (See Figure 5). **For cavity down mounting, pin numbering will have clockwise orientation.**

**Table 1. Pin Assignment and Descriptions (Continued)**

Pin Name	Level	I/O	Pin #	Description
DIN7P DIN7N DIN6P DIN6N DIN5P DIN5N DIN4P DIN4N DIN3P DIN3N DIN2P DIN2N DIN1P DIN1N DIN0P DIN0N	Diff. PECL	Input Pairs	11 12 156 155 8 10 158 157 5 6 161 159 2 3 164 163	Differential PECL input data. Differential inputs can be used as single-ended inputs with $V_{BB}$ tied to one side of each differential input pair.
ADVERTISEP ADVERTISEN	Diff. PECL	Input Pair	202 199	A 33rd input channel that can be mapped to any or all output channels. Gets mapped to selected outputs when ADVERT is high.
LOADN	TTL	I	138	Load strobe, active Low. When low, writes into the crosspoint switch memory when CSN is asserted.
CONFIGN	TTL	I	147	Configuration strobe, active Low. When low, parallel loads the contents of the configuration register file into the active configuration latch.
RESETN	TTL	I	123	Reset. Active Low. Sets all the outputs to be tied to the ADVERTISEP/N input.
CSN			139	Chip select.
PARAOUT			203	AMCC test pin. (No connect.)
DOUT31P DOUT31N DOUT30P DOUT30N DOUT29P DOUT29N DOUT28P DOUT28N DOUT27P DOUT27N DOUT26P DOUT26N	Diff. PECL	Output pairs	58 59 223 222 61 62 220 219 64 66 217 215	Output data. Differential.

Note: Cavity up counter clockwise pin numbering orientation. (See Figure 5). **For cavity down mounting, pin numbering will have clockwise orientation.**

**Table 1. Pin Assignment and Descriptions (Continued)**

Pin Name	Level	I/O	Pin #	Description
DOUT25P	Diff. PECL	Output Pairs	67	Output data. Differential.
DOUT25N			68	
DOUT24P			216	
DOUT24N			213	
DOUT23P			69	
DOUT23N			71	
DOUT22P			214	
DOUT22N			212	
DOUT21P			70	
DOUT21N			74	
DOUT20P			211	
DOUT20N			210	
DOUT19P			72	
DOUT19N			75	
DOUT18P			209	
DOUT18N			206	
DOUT17P			77	
DOUT17N			78	
DOUT16P			207	
DOUT16N			204	
DOUT15P			91	
DOUT15N			89	
DOUT14P			190	
DOUT14N			193	
DOUT13P			92	
DOUT13N			94	
DOUT12P			189	
DOUT12N			187	
DOUT11P			97	
DOUT11N			98	
DOUT10P			184	
DOUT10N			183	
DOUT9P	99			
DOUT9N	100			
DOUT8P	182			
DOUT8N	181			
DOUT7P	101			
DOUT7N	102			
DOUT6P	180			
DOUT6N	179			
DOUT5P	103			
DOUT5N	105			
DOUT4P	178			
DOUT4N	176			
DOUT3P	107			
DOUT3N	108			
DOUT2P	174			
DOUT2N	173			
DOUT1P	110			
DOUT1N	111			
DOUT0P	171			
DOUT0N	170			

Note: Cavity up counter clockwise pin numbering orientation. (See Figure 5). **For cavity down mounting, pin numbering will have clockwise orientation.**

**Table 1. Pin Assignment and Descriptions (Continued)**

Pin Name	Level	I/O	Pin #	Description
CRFDAT0 CRFDAT1 CRFDAT2 CRFDAT3 CRFDAT4 CRFDAT5 CRFDAT6 CRFDAT7 CRFDAT8 CRFDAT9 CRFDAT10 CRFDAT11 CRFDAT12 CRFDAT13 CRFDAT14 CRFDAT15	TTL	I	136 137 135 133 191 194 195 196 198 87 86 85 83 82 80 79	16-Bit Data Bus used to specify the output channel(s) and direct the ADVERTISE INPUT.
CRFADDR0 CRFADDR1 CRFADDR2 CRFADDR3 CRFADDR4 CRFADDR5 CRFADDR6 CRFADDR7 CRFADDR8 CRFADDR9	TTL	I	23 24 26 27 28 29 30 31 33 34	10-Bit Address Bus used to memory map the various operating functions of the device, including Broadcast, Multicast, Break, and Unicast modes.

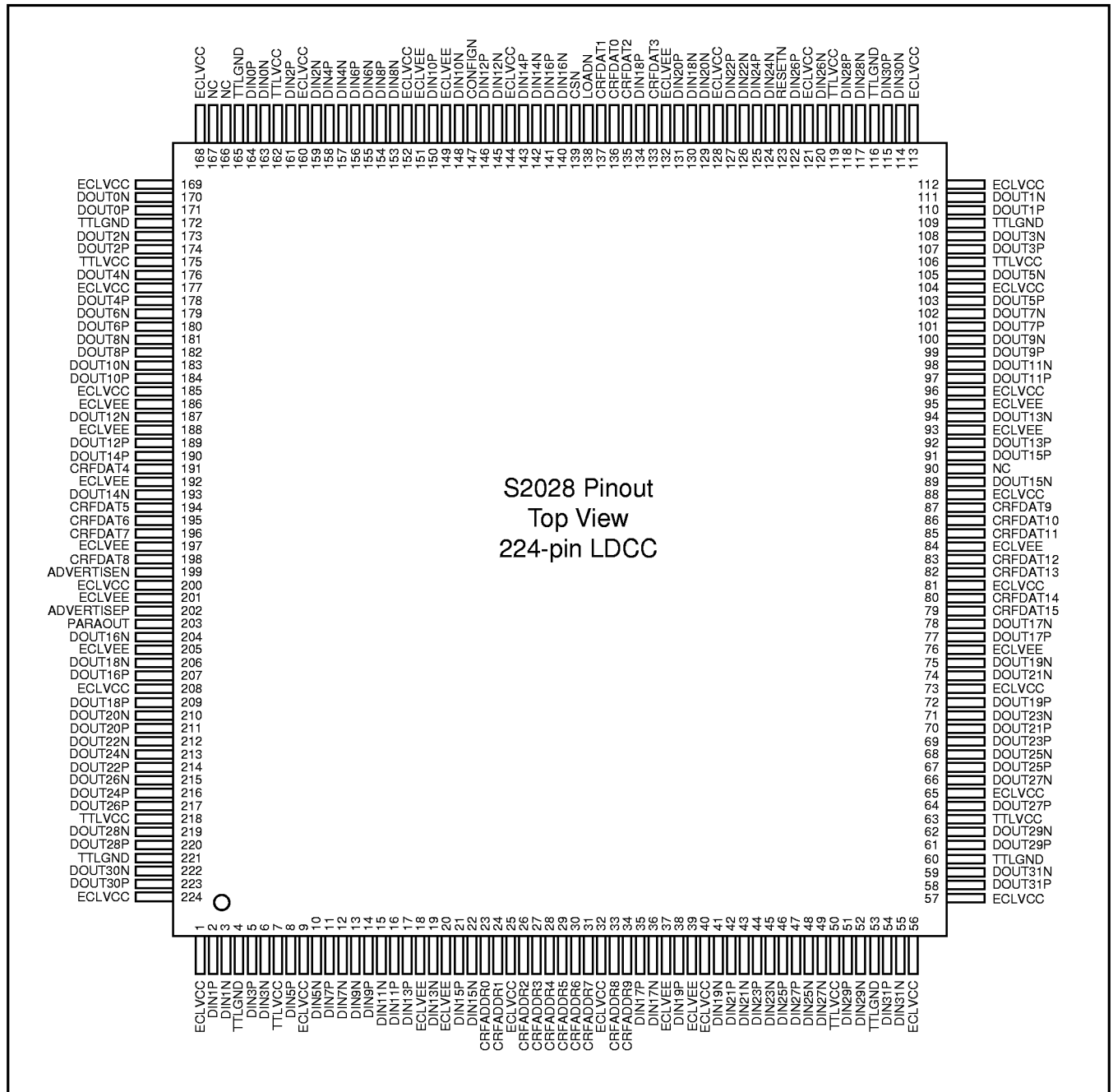
Note: Cavity up counter clockwise pin numbering orientation. (See Figure 5). **For cavity down mounting, pin numbering will have clockwise orientation.**

**Table 1. Pin Assignment and Descriptions (Continued)**

Pin Name	Level	I/O	Pin #	Description
ECLVCC	+5V		1, 9, 25, 32, 40, 56, 57, 65, 73, 81, 88, 96, 104, 112, 113, 121, 128, 144, 152, 160, 168, 169, 177, 185, 200, 208, 224	ECL Power Supply
TTLGND	GND		4, 53, 60, 109, 116, 165, 172, 221	TTL Ground
TTLVCC	+5V		7, 50, 63, 106, 119, 162, 175, 218	TTL Power Supply
ECLVEE	GND		18, 20, 37, 39, 76, 84, 93, 95, 132, 149, 151, 186, 188, 192, 197, 201, 205	ECL Ground
NC			90, 166, 167	No Connect

Note: Cavity up counter clockwise pin numbering orientation. (See Figure 5). **For cavity down mounting, pin numbering will have clockwise orientation.**

Figure 4. S2028 Pinout



**Figure 5. 224-Pin LDCC Package**

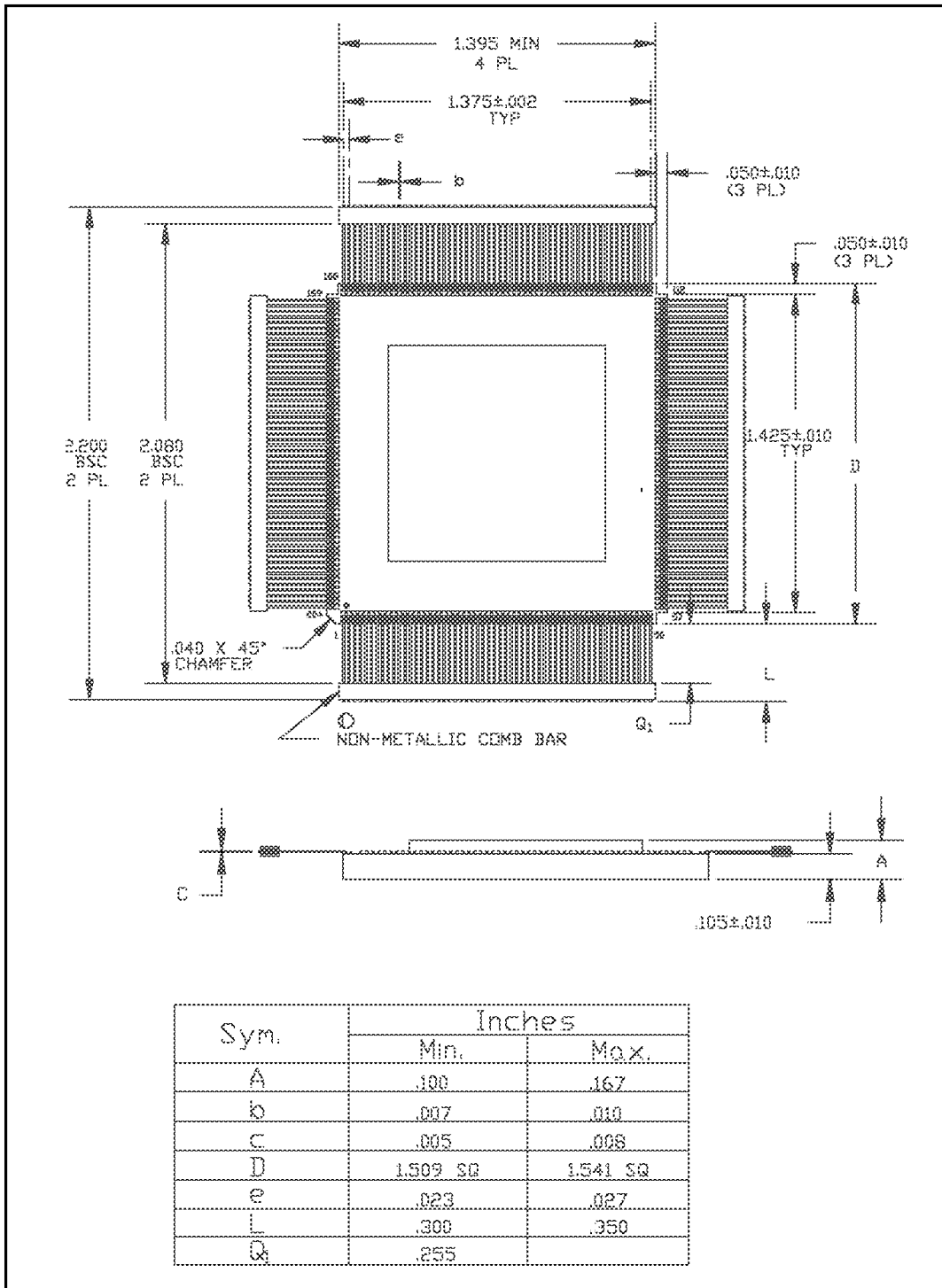
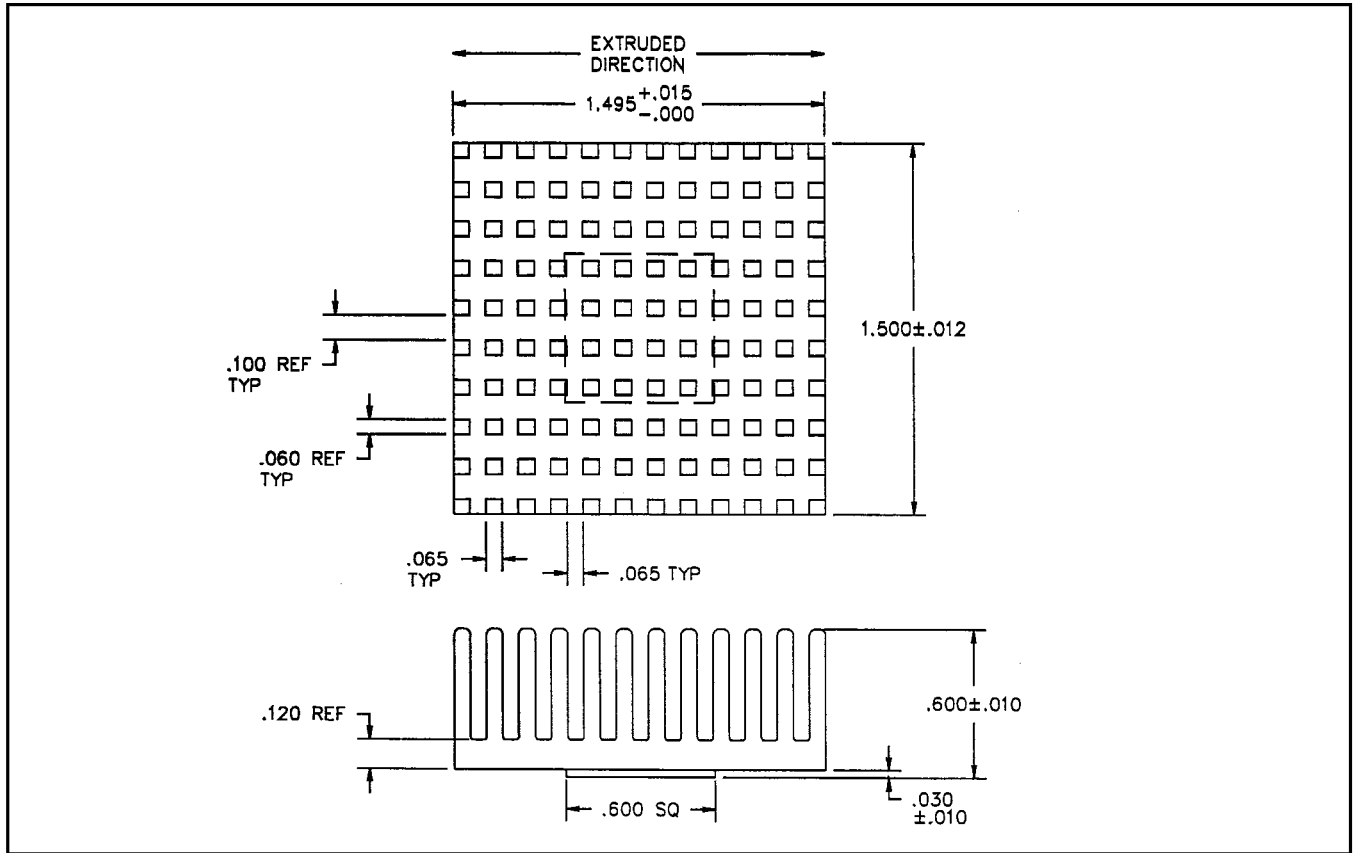


Figure 6. AMCC Heat Sink 45-18



### Thermal Management

The S2028A device requires sufficient thermal management for proper functionality and reliability. It is recommended that the user investigate, define, and implement correct techniques in managing the power of this product. Techniques to consider include: headspreading through metal layers within your PCB in addition to heatsinking with mounted heatsink and moving; fluid controlled thermal management.

Table 2. S2028 Thermal Data

<p>AMCC Recommended:  <math>T_{Jmax} = 130^{\circ}C</math>          Temperature Range (0 to <math>70^{\circ}C</math>)  <math>P_d = 16W</math>          224 pin LDCC: <math>T_{ja} = 19^{\circ}C/W</math>, <math>T_{jc} = 1.8^{\circ}C/W</math></p>	<p>Calculation of required <math>T_{ja}</math> for S2028:  <math>T_{ja} = (130-70)/16 = 3.75^{\circ}C/W</math>          Since: <math>T_{ja} = T_{jc} + T_{ca}</math>          Heatsink must meet:  <math>T_{ca} = 3.75-1.8 = 1.95^{\circ}C/W</math></p>
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Note: The best heatsink currently available at AMCC is rated  $2.1^{\circ}C/W$  with 1000 LFPM airflow. (See Figure 6).

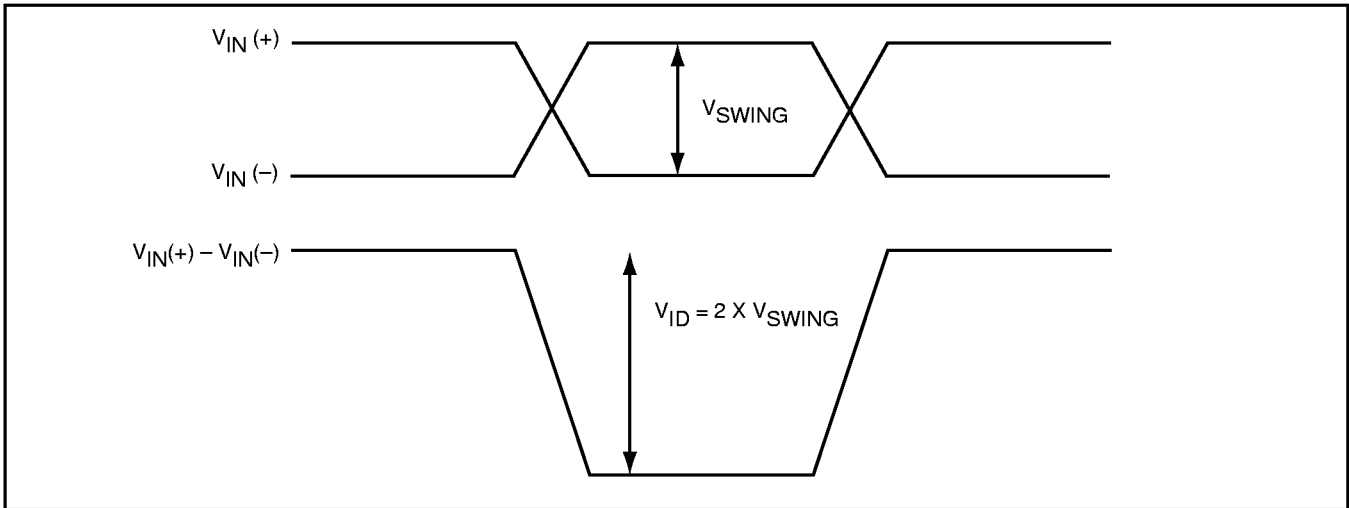
**Table 3. Absolute Maximum Ratings**

Supply Voltage $V_{CC}$	7.0V
PECL Input Voltage	$V_{CC} - 2.5V$ to $V_{CC}$
PECL Output Source Current (continuous)	-50mA DC
TTL Input Voltage	5.5V
Operating Junction Temperature $T_J$	+150°C
Storage Temperature	-65° to +150°C

**Table 4. Recommended Operating Conditions**

Parameter	Min	Nom	Max	Units
Supply Voltage $V_{CC}$	4.75	5.0	5.25	V
Ambient Temperature	0		70	°C
Junction Temperature			130	°C
$I_{CC}$		3.5	4.50	A

Figure 7. Differential Input Voltage



Note:  $V_{IN(+)} - V_{IN(-)}$  is the algebraic difference of the input signals.

Table 5. PECL DC Characteristics<sup>3</sup>

Symbol	Min	Typ	Max	Units
$V_{IH}^2$	$V_{CC} - 1145$		$V_{CC} - 600$	mV
$V_{IL}^2$	$V_{CC} - 2000$		$V_{CC} - 1450$	mV
$V_{BIAS}^{1,2}$		$V_{CC} - 1300$		mV
$I_{IH}^2$			30	$\mu A$
$I_{IL}^2$			-0.5	$\mu A$

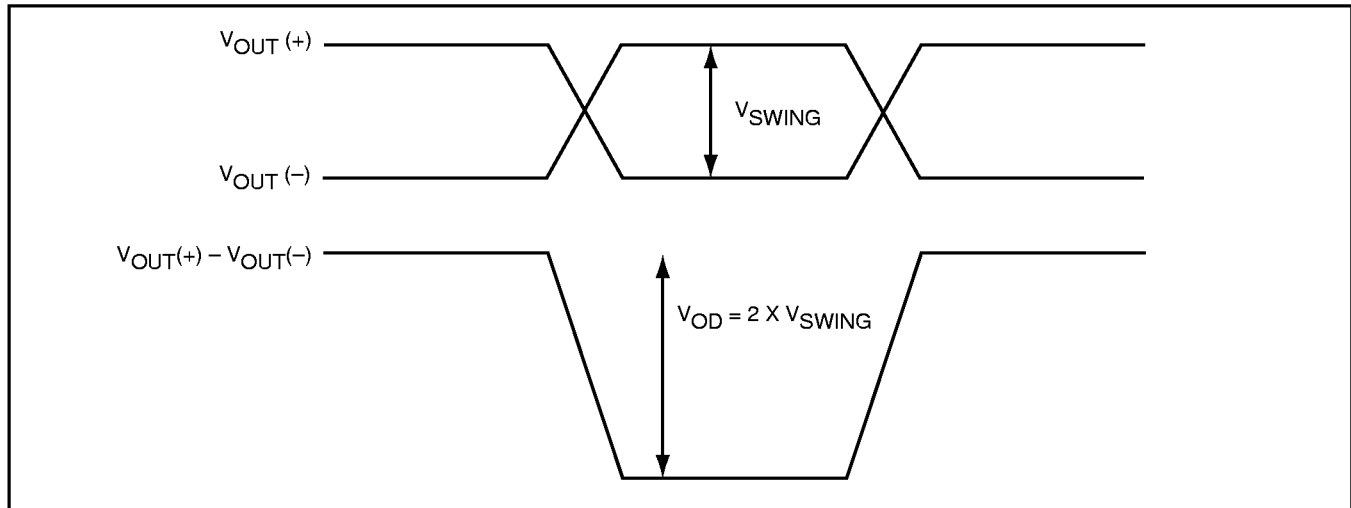
1. Internal bias point.
2. Single-ended connection.
3. DC is considered to be an input signal between 0Hz and 1KHz.

Table 6. Differential PECL Characteristics

Symbol	Min	Typ	Max	Units
$V_{ID}^1$	500		2800	mV

1. Differential input voltage - algebraic difference.

**Figure 8. Differential Output Voltage**



Note:  $V_{OUT(+)} - V_{OUT(-)}$  is the algebraic difference of the input signals.

**Table 7. PECL DC Characteristics<sup>2</sup>**

Symbol	Min	Typ	Max	Units
$V_{OH}^1$	$V_{CC} - 1095$		$V_{CC} - 695$	mV
$V_{OL}^1$	$V_{CC} - 1900$		$V_{CC} - 1365$	mV
$I_{OH}$		20		mA
$I_{OL}$		5		mA

1. All outputs are loaded with  $50\Omega$  to  $V_{CC} - 2V$ .
2. DC is considered to be an output signal between 0Hz and 1KHz.

**Table 8. Differential PECL Characteristics**

Symbol	Min	Typ	Max	Units
$V_{OD}^1$	700		2330	mV

1. Differential output voltage - algebraic difference.

**Table 9. TTL Input DC Characteristics**

Symbol	Parameter	Conditions	Commercial 0° to 70°C			Unit
			Min	Typ <sup>1</sup>	Max	
$V_{IH}^2$	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all input pairs	2.0			V
$V_{IL}^2$	Input LOW Voltage	Guaranteed Input LOW Voltage for all input pairs			0.8	V
$V_{IK}$	Input Clamp Diode Voltage	$V_{CC} = \text{MIN}, I_{IN} = -18 \text{ mA}$		-0.8	-1.2	V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$			50	$\mu\text{A}$
$I_I$	Input HIGH Current at Max.	$V_{CC} = \text{MAX}, V_{IN} = V_{CC} + 0.3\text{V}$			1	mA
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX}, V_{IN} = 0.5\text{V}$			-0.4	mA

1. Typical limits are at 25°C,  $V_{CC} = 5.0\text{V}$ .

2. These input levels provide a zero noise immunity and should only be tested in a static, noise-free environment.

**Table 10. Data Transfer Timing<sup>1</sup>**

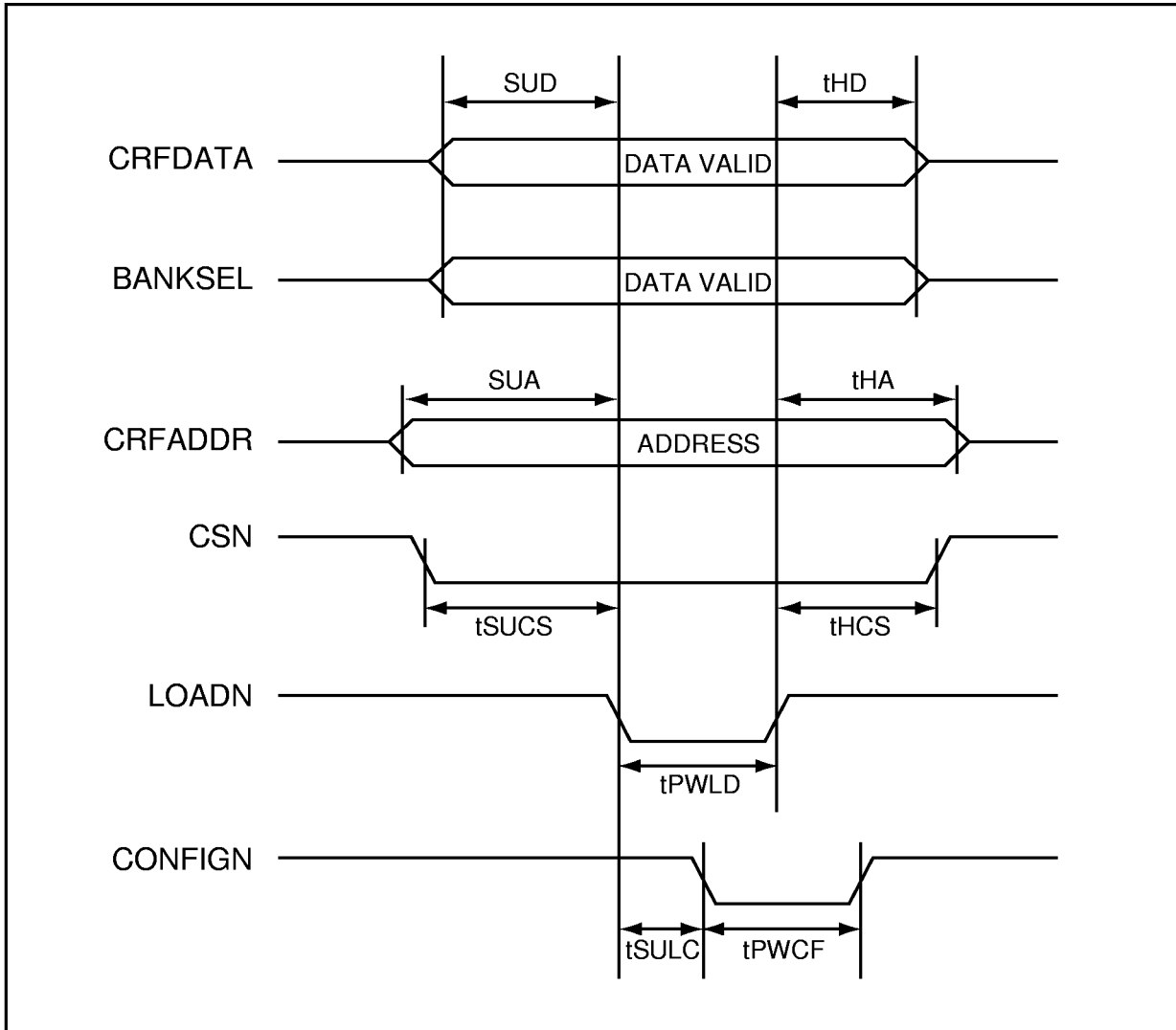
Symbol	Description	Min.	Max.	Units
$t_{DIDO}$	Propagation delay from DIN[31:0] P/N or ADVERTISEP/N to DOUT[31:0] P/N		3	ns
$t_{CFDO}$	Propagation delay from falling edge of CONFIGN to DOUT[31:0] P/N valid		6	ns
$t_{LDDO}$	Propagation delay from falling edge of LOADN to DOUT[31:0] P/N valid (When CONFIGN is held low)		8.5	ns
$D_{I\text{MPW}}$	Pulse width of DIN[31:0] P/N	0.650		ns
$F_{\text{MAX}}$	Data rate	1250	1250	Mbit/s
$t_{\text{PER}}$	Configuration cycle time	10		ns
$t_{\text{BTB}}$	Back to back cycle time	5		ns

1. All timing measured from the  $V_{CC} - 1.3\text{V}$  point on the signals.

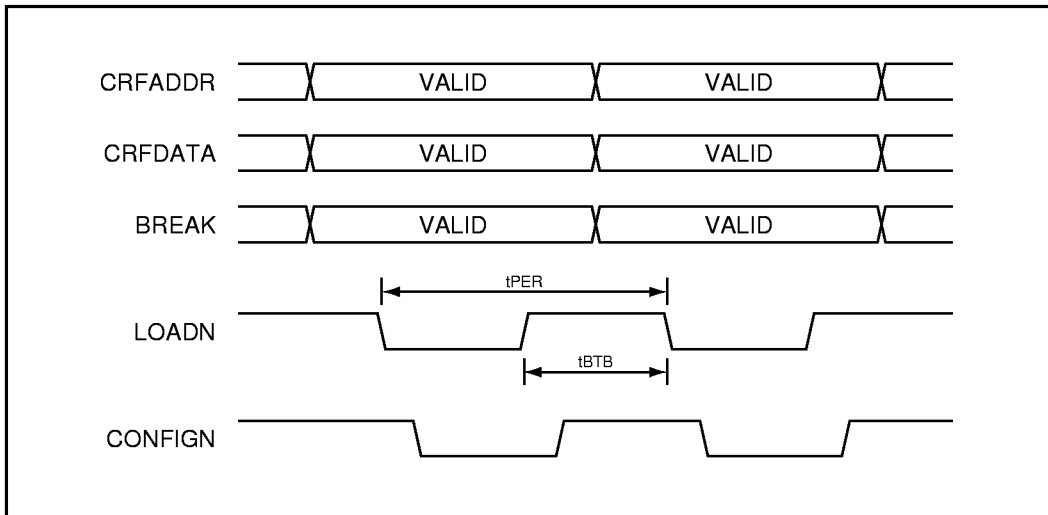
**Table 11. Reconfiguration Timing<sup>1</sup>**

<b>Symbol</b>	<b>Description</b>	<b>Min.</b>	<b>Max.</b>	<b>Units</b>
$t_{SUD}$	Setup time of CRFDATA before falling edge of LOADN	2		ns
$t_{HD}$	Hold time of CRFDATA after rising edge of LOADN	2		ns
$t_{SUA}$	Setup time of CRFADDR before falling edge of LOADN	2		ns
$t_{HA}$	Hold time of CRFADDR after rising edge of LOADN	1.5		ns
$t_{SUCS}$	Setup time of CSN before falling edge of LOADN	2		ns
$t_{HCS}$	Hold time of CSN after rising edge of LOADN	2		ns
$t_{SULC}$	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	1.5		ns
$t_{PWLD}$	Pulse width low of LOADN	2		ns
$t_{PWCF}$	Pulse width low of CONFIGN	2		ns

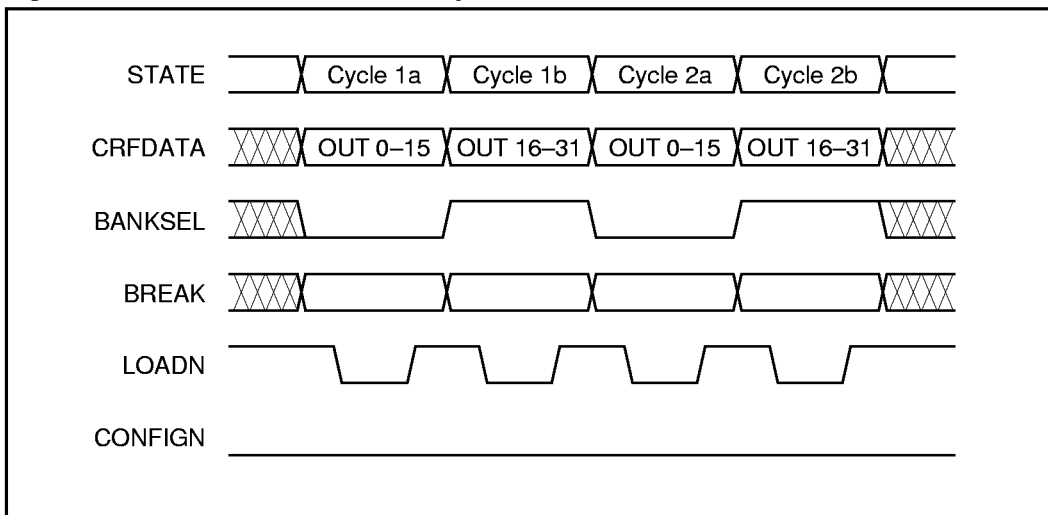
1. All timing measured from the 1.5V point on the signals.

*Figure 9. Data Transfer Timing*

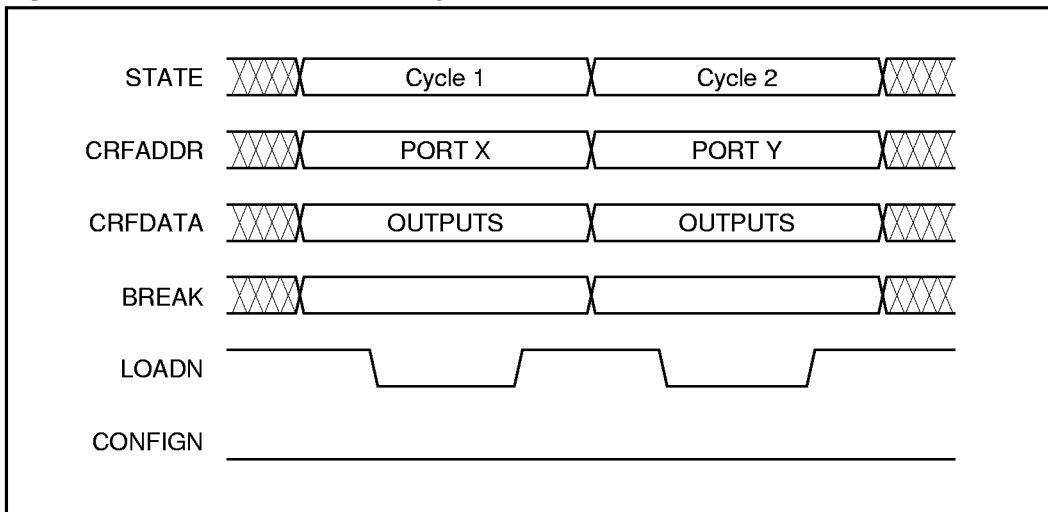
**Figure 10. Back to Back Cycles**



**Figure 11. Back to Back Multicast Cycles with CONFIG Low**

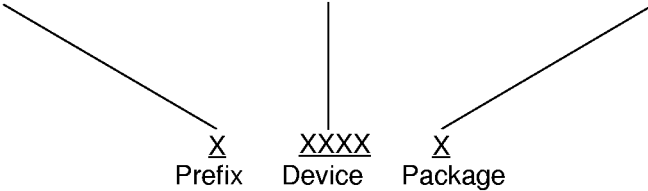


**Figure 12. Back to Back Unicast Cycles with CONFIGN Low**



**Ordering Information**

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	2028A	A – 224 LDCC with straight leads



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