

TENTATIVE

TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

8,388,608-WORD BY 64-BIT DYNAMIC RAM MODULE

## DESCRIPTION

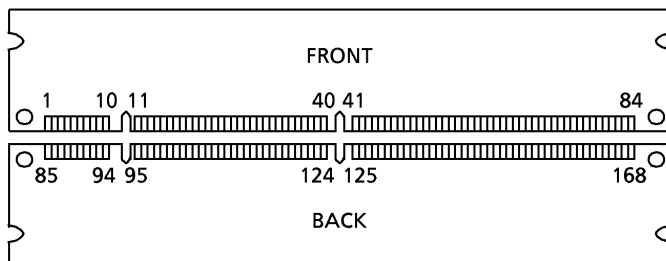
The THM65V8035BTG is a 8,388,608-word by 64-bit dynamic RAM module consisting of eight TC5164805BFT DRAMs on a printed circuit board. This module is optimized for applications which require high density and high capacity, such as computer main memory and image memory, and also for applications which require compactness.

## FEATURES

- 8,388,608-word by 64-bit organization
- Fast access and cycle times
- Single power supply of 3.3 V ± 5%
- Low power dissipation (max)
  - Operating 3332 mW (40-ns type)
  - 2776 mW (50-ns type)
  - Standby 13.9 mW (both devices)
- Read-Modify-Write, CAS-before-RAS refresh, Hidden refresh and EDO capability
- All inputs and outputs LVTTTL-compatible
- 4096 refresh cycles per 64 ms
- Package: 168-pin TSOP Gold contacts

	-4	-5
t <sub>RAC</sub> RAS Access Time	40 ns	50 ns
t <sub>AA</sub> Column Address Access Time	20 ns	25 ns
t <sub>CAC</sub> CAS Access Time	11 ns	13 ns
t <sub>RC</sub> Cycle Time	69 ns	84 ns
t <sub>HPC</sub> Hyper Page Mode Cycle Time	16 ns	20 ns

## PIN ASSIGNMENT (TOP VIEW)



1	V <sub>SS</sub>	85	V <sub>SS</sub>	29	/CAS1	113	/CAS5	57	DQ18	141	DQ50
2	DQ0	86	DQ32	30	/RAS0	114	NC	58	DQ19	142	DQ51
3	DQ1	87	DQ33	31	/OE0	115	NC	59	V <sub>CC</sub>	143	V <sub>CC</sub>
4	DQ2	88	DQ34	32	V <sub>SS</sub>	116	V <sub>SS</sub>	60	DQ20	144	DQ52
5	DQ3	89	DQ35	33	A0	117	A1	61	NC	145	NC
6	V <sub>CC</sub>	90	V <sub>CC</sub>	34	A2	118	A3	62	NC	146	NC
7	DQ4	91	DQ36	35	A4	119	A5	63	NC	147	NC
8	DQ5	92	DQ37	36	A6	120	A7	64	V <sub>SS</sub>	148	V <sub>SS</sub>
9	DQ6	93	DQ38	37	A8	121	A9	65	DQ21	149	DQ53
10	DQ7	94	DQ39	38	A10R	122	A11R	66	DQ22	150	DQ54
11	DQ8	95	DQ40	39	A12R	123	NC	67	DQ23	151	DQ55
12	V <sub>SS</sub>	96	V <sub>SS</sub>	40	V <sub>CC</sub>	124	V <sub>CC</sub>	68	V <sub>SS</sub>	152	V <sub>SS</sub>
13	DQ9	97	DQ41	41	V <sub>CC</sub>	125	NC	69	DQ24	153	DQ56
14	DQ10	98	DQ42	42	NC	126	NC	70	DQ25	154	DQ57
15	DQ11	99	DQ43	43	V <sub>SS</sub>	127	V <sub>SS</sub>	71	DQ26	155	DQ58
16	DQ12	100	DQ44	44	/OE2	128	NC	72	DQ27	156	DQ59
17	DQ13	101	DQ45	45	/RAS2	129	NC	73	V <sub>CC</sub>	157	V <sub>CC</sub>
18	V <sub>CC</sub>	102	V <sub>CC</sub>	46	/CAS2	130	/CAS6	74	DQ28	158	DQ60
19	DQ14	103	DQ46	47	/CAS3	131	/CAS7	75	DQ29	159	DQ61
20	DQ15	104	DQ47	48	/WE2	132	NC	76	DQ30	160	DQ62
21	NC	105	NC	49	V <sub>CC</sub>	133	V <sub>CC</sub>	77	DQ31	161	DQ63
22	NC	106	NC	50	NC	134	NC	78	V <sub>SS</sub>	162	V <sub>SS</sub>
23	V <sub>SS</sub>	107	V <sub>SS</sub>	51	NC	135	NC	79	NC	163	NC
24	NC	108	NC	52	NC	136	NC	80	NC	164	NC
25	NC	109	NC	53	NC	137	NC	81	NC	165	SA0
26	V <sub>CC</sub>	110	V <sub>CC</sub>	54	V <sub>SS</sub>	138	V <sub>SS</sub>	82	SDA	166	SA1
27	/WE0	111	NC	55	DQ16	139	DQ48	83	SCL	167	SA2
28	/CAS0	112	/CAS4	56	DQ17	140	DQ49	84	V <sub>CC</sub>	168	V <sub>CC</sub>

## PIN NAMES

A0 to 9, A10R to 12R	Address Inputs
DQ0 to 63	Data Inputs/Outputs
RAS0,2	Row Address Strobe
CAS0 to 7	Column Address Strobe
WE0,2	Read/Write Input
OE0,2	Output Enable
V <sub>CC</sub>	Power (+3.3V)
V <sub>SS</sub>	Ground
SCL	Presence Detect Clock
SDA	Serial Data-out
SA0 to 2	Serial PD Address
NC	No Connection

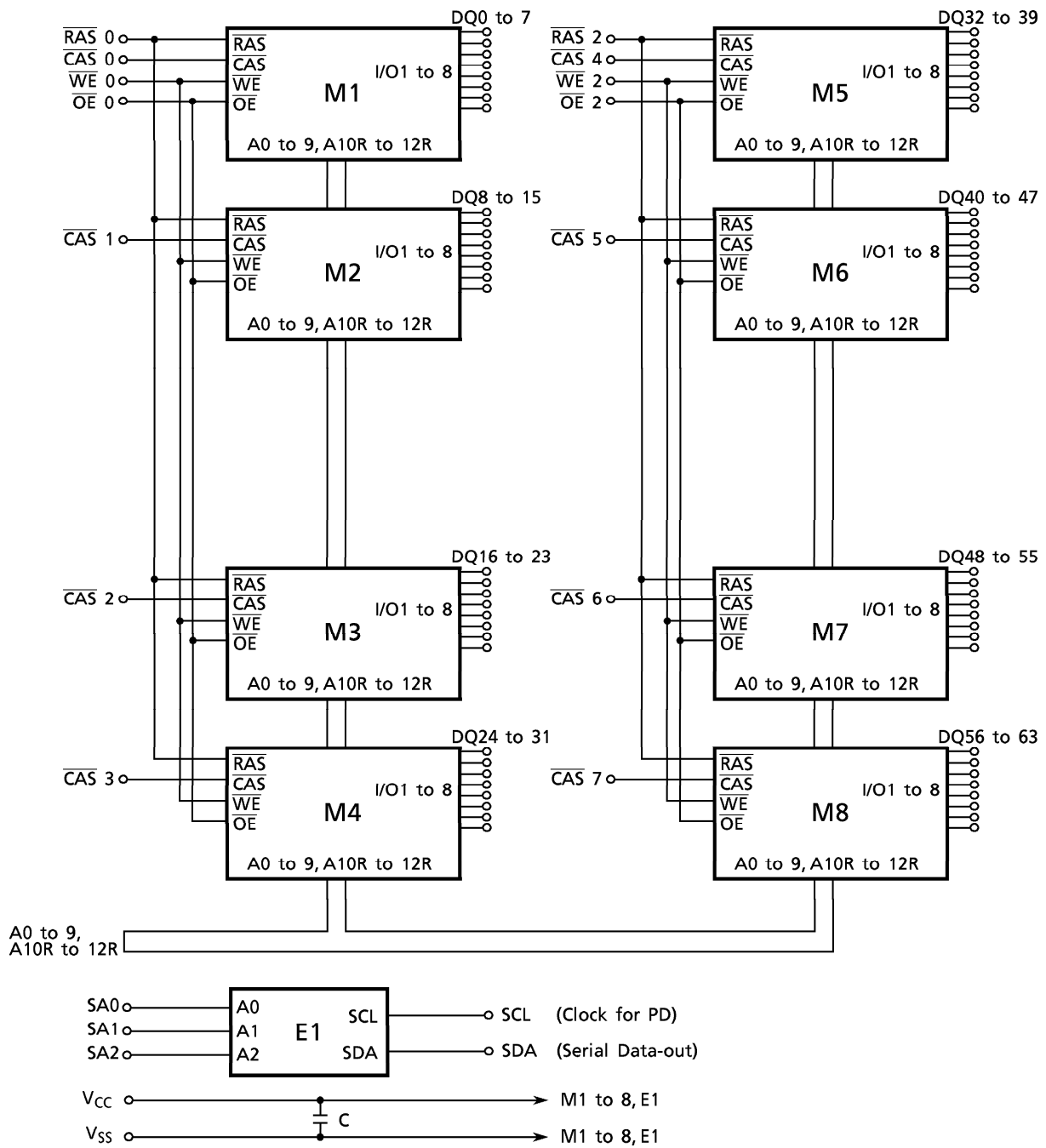
## SERIAL PRESENCE DETECT

	-4 (hex)	-5 (hex)	Notes
Byte-0	80	80	128 bytes
Byte-1	08	08	256 bytes
Byte-2	02	02	EDO
Byte-3	0D	0D	A <sub>R</sub>
Byte-4	0A	0A	A <sub>C</sub>
Byte-5	01	01	DIMM Bank
Byte-6	40	40	x64
Byte-7	00	00	—
Byte-8	01	01	LVTTTL
Byte-9	28	32	t <sub>RAC</sub>
Byte-10	0B	0D	t <sub>CAC</sub>
Byte-11	00	00	Non-parity
Byte-12	00	00	15.625 μs (Normal)
Byte-13	08	08	x8
Byte-14	00	00	Non-parity

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V <sub>IN</sub>	Input Voltage	- 0.3 to V <sub>CC</sub> + 0.3	V	1
V <sub>OUT</sub>	Output Voltage	- 0.3 to V <sub>CC</sub> + 0.3	V	1
V <sub>CC</sub>	Power Supply Voltage	- 0.3 to 4.6	V	1
T <sub>OPR</sub>	Operating Temperature	0 to 70	°C	1
T <sub>STG</sub>	Storage Temperature	- 55 to 125	°C	1
P <sub>D</sub>	Power Dissipation	3.7	W	1
I <sub>OUT</sub>	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V <sub>CC</sub>	Supply Voltage	3.13	3.3	3.47	V	2
V <sub>IH</sub>	Input High Voltage	2.0	-	V <sub>CC</sub> + 0.3*	V	2
V <sub>IL</sub>	Input Low Voltage	- 0.3**	-	0.8	V	2

\* V<sub>CC</sub> + 1.2 V at pulse width ≤ 20 ns (pulse width is measured at V<sub>CC</sub>)

\*\* - 1.2 V at pulse width ≤ 20 ns (pulse width is measured at V<sub>SS</sub>)

CAPACITANCE (V<sub>CC</sub> = 3.3 V ± 5%, f = 1 MHz, Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C <sub>I1</sub>	Input Capacitance (A0 to 9, A10R to 12R)	-	70	pF
C <sub>I2</sub>	Input Capacitance ( $\overline{WE}0,2$ )	-	41	pF
C <sub>I3</sub>	Input Capacitance ( $\overline{RAS}0,2$ )	-	43	pF
C <sub>I4</sub>	Input Capacitance ( $\overline{CAS}0$ to 7)	-	15	pF
C <sub>I5</sub>	Input Capacitance ( $\overline{OE}0,2$ )	-	45	pF
C <sub>DQ</sub>	I/O Capacitance (DQ0 to 63)	-	15	pF

**DC CHARACTERISTICS** ( $V_{CC} = 3.3\text{ V} \pm 5\%$ ,  $T_a = 0^\circ$  to  $70^\circ\text{C}$ )

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I <sub>CC1</sub>	OPERATING CURRENT Average Power Supply Operating Current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t_{RC} = t_{RC\text{ min}}$ )	THMxxxxxx-4	-	680	mA	3, 4, 5
		THMxxxxxx-5	-	560		
I <sub>CC2</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )		-	8	mA	
I <sub>CC4</sub>	HYPER PAGE MODE CURRENT Average Power Supply Current, Hyper Page Mode ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IL}$ , Address Cycling: $t_{HPC} = t_{HPC\text{ min}}$ )	THMxxxxxx-4	-	720	mA	3, 4, 5
		THMxxxxxx-5	-	600		
I <sub>CC5</sub>	STANDBY CURRENT Power Supply Standby Current ( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{ V}$ )		-	4	mA	
I <sub>CC6</sub>	CAS-BEFORE-RAS REFRESH CURRENT Average Power Supply Current, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Mode ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ Cycling: $t_{RC} = t_{RC\text{ min}}$ )	THMxxxxxx-4	-	960	mA	3, 5
		THMxxxxxx-5	-	800		
I <sub>I(L)</sub>	INPUT LEAKAGE CURRENT Input Leakage Current, Any Input ( $0\text{ V} \leq V_{IN} \leq V_{CC}$ , All Other Pins Not under Test = $0\text{ V}$ )		- 10	10	$\mu\text{A}$	
I <sub>O(L)</sub>	OUTPUT LEAKAGE CURRENT ( $D_{OUT}$ Is Disabled, $0\text{ V} \leq V_{OUT} \leq V_{CC}$ )		- 10	10	$\mu\text{A}$	
V <sub>OH</sub>	OUTPUT LEVEL Output H Level Voltage ( $I_{OUT} = -2\text{ mA}$ )		2.4	-	V	
V <sub>OL</sub>	OUTPUT LEVEL Output L Level Voltage ( $I_{OUT} = 2\text{ mA}$ )		-	0.4	V	

**AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

( $V_{CC} = 3.3\text{ V} \pm 5\%$ ,  $T_a = 0^\circ$  to  $70^\circ\text{C}$ )

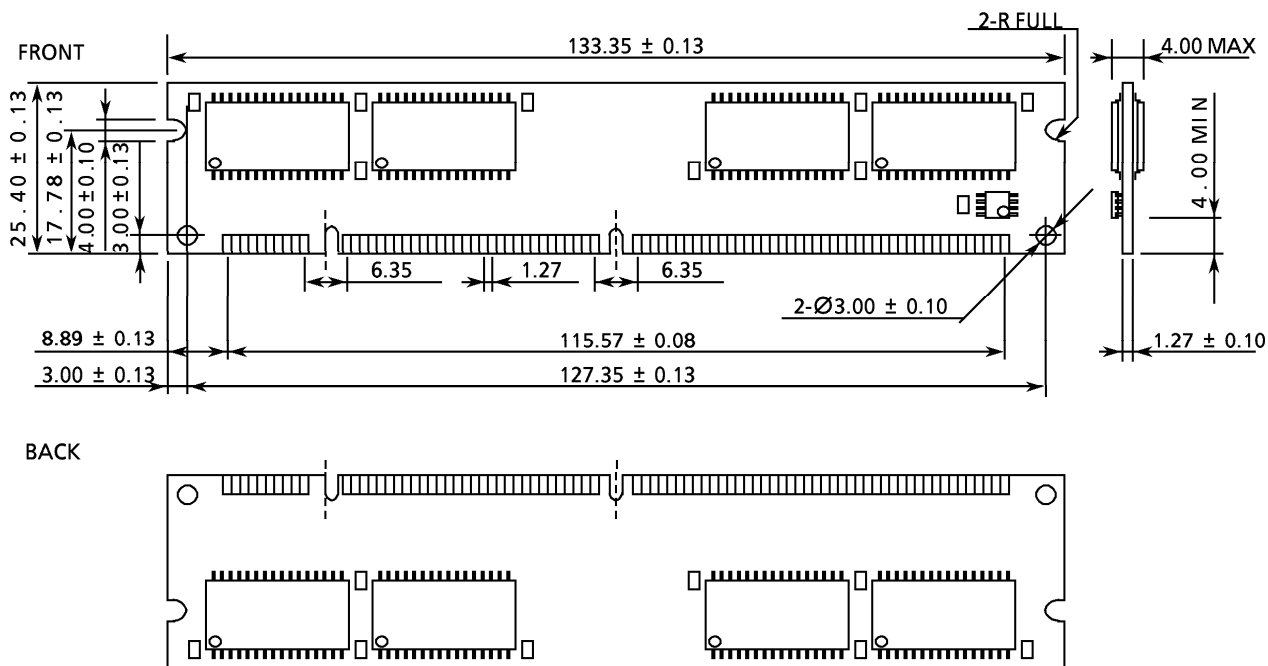
Please refer to DRAM MODULE AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No. 44

**SERIAL PRESENCE DETECT AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

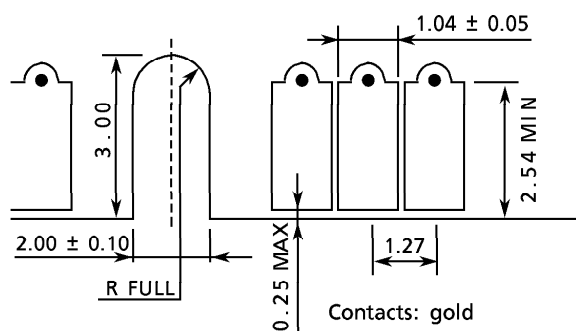
For information on SERIAL PRESENCE DETECT please refer to AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No. 100

**PACKAGE DIMENSIONS (THM65V8035BTG)**

Unit: mm



**CONTACT DIMENSIONS**



Weight: 14.4g (typ.)

# **DRAM MODULE AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No.44**

<b>TC5164405BJ/BFT/BJS/BFTS</b>	<b>USING MODULE</b>
<b>TC5165405BJ/BFT/BJS/BFTS</b>	<b>USING MODULE</b>
<b>TC5164805BJ/BFT/BJS/BFTS</b>	<b>USING MODULE</b>
<b>TC5165805BJ/BFT/BJS/BFTS</b>	<b>USING MODULE</b>
<b>TC5164165BFT/BFTS</b>	<b>USING MODULE</b>
<b>TC5165165BFT/BFTS</b>	<b>USING MODULE</b>

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**AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS**

( $V_{CC} = 3.3V \pm 0.3V$ ,  $T_a = 0$  to  $70^\circ\text{C}$ ) (Notes 6, 7, 8)

SYMBOL	PARAMETER					UNIT	NOTES
		-40		-50			
		MIN	MAX	MIN	MAX		
$t_{RC}$	Random Read or Write Cycle Time	69	-	84	-	ns	
$t_{RMW}$	Read-Modify-Write Cycle Time	92	-	111	-	ns	
$t_{RAC}$	Access Time from $\overline{RAS}$	-	40	-	50	ns	9, 14, 15
$t_{CAC}$	Access Time from $\overline{CAS}$	-	11	-	13	ns	9, 14
$t_{AA}$	Access Time from Column Address	-	20	-	25	ns	9, 15
$t_{CPA}$	Access Time from $\overline{CAS}$ Precharge	-	22	-	28	ns	9
$t_{CLZ}$	$\overline{CAS}$ to output in Low-Z	0	-	0	-	ns	
$t_{OFF}$	Output Buffer Turn-off Delay	0	11	0	13	ns	10, 16
$t_T$	Transition Time (Rise and Fall)	1	50	1	50	ns	8
$t_{RP}$	$\overline{RAS}$ Precharge Time	25	-	30	-	ns	
$t_{RAS}$	$\overline{RAS}$ Pulse Width	40	10,000	50	10,000	ns	
$t_{RASP}$	$\overline{RAS}$ Pulse Width (Hyper Page Mode)	40	100,000	50	100,000	ns	
$t_{RSH}$	$\overline{RAS}$ Hold Time	6	-	8	-	ns	
$t_{RHCP}$	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Hyper Page Mode)	22	-	28	-	ns	
$t_{CSH}$	$\overline{CAS}$ Hold Time	30	-	35	-	ns	
$t_{CAS}$	$\overline{CAS}$ Pulse Width	6	10,000	8	10,000	ns	
$t_{RCD}$	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10	29	12	37	ns	14
$t_{RAD}$	$\overline{RAS}$ to Column Address Delay Time	8	20	10	25	ns	15
$t_{CRP}$	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	
$t_{CP}$	$\overline{CAS}$ Precharge Time	6	-	8	-	ns	
$t_{ASR}$	Row Address Set-Up Time	0	-	0	-	ns	
$t_{RAH}$	Row Address Hold Time	6	-	8	-	ns	
$t_{ASC}$	Column Address Set-Up Time	0	-	0	-	ns	
$t_{CAH}$	Column Address Hold Time	6	-	8	-	ns	
$t_{RAL}$	Column Address to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
$t_{RCS}$	Read Command Set-Up Time	0	-	0	-	ns	
$t_{RCH}$	Read Command Hold Time	0	-	0	-	ns	11
$t_{RRH}$	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	11
$t_{WCH}$	Write Command Hold Time	6	-	8	-	ns	
$t_{WP}$	Write Command Pulse Width	6	-	8	-	ns	
$t_{RWL}$	Write Command to $\overline{RAS}$ Lead Time	6	-	8	-	ns	
$t_{CWL}$	Write Command to $\overline{CAS}$ Lead Time	6	-	8	-	ns	
$t_{DS}$	Data Set-Up Time	0	-	0	-	ns	12
$t_{DH}$	Data Hold Time	6	-	8	-	ns	12

**AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)**

SYMBOL	PARAMETER					UNIT	NOTES
		-40		-50			
		MIN	MAX	MIN	MAX		
t <sub>REF</sub>	Refresh Period	–	64	–	64	ms	
t <sub>REF</sub>	Refresh Period (Self Refresh)	–	128	–	128	ms	
t <sub>WCS</sub>	Write Command Set-Up Time	0	–	0	–	ns	13
t <sub>CWD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	26	–	30	–	ns	13
t <sub>RWD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	55	–	67	–	ns	13
t <sub>AWD</sub>	Column Address to $\overline{\text{WE}}$ Delay Time	35	–	42	–	ns	13
t <sub>CPWD</sub>	$\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time	37	–	45	–	ns	13
t <sub>CSR</sub>	$\overline{\text{CAS}}$ Set-Up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	5	–	5	–	ns	
t <sub>CHR</sub>	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	6	–	8	–	ns	
t <sub>RPC</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	5	–	5	–	ns	
t <sub>ROH</sub>	$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	6	–	8	–	ns	
t <sub>OEA</sub>	$\overline{\text{OE}}$ Access Time	–	11	–	13	ns	9
t <sub>OED</sub>	$\overline{\text{OE}}$ to Data Delay	11	–	13	–	ns	
t <sub>OLZ</sub>	$\overline{\text{OE}}$ to output in Low-Z	0	–	0	–	ns	
t <sub>OEZ</sub>	Output buffer turn off Delay Time from $\overline{\text{OE}}$	0	11	0	13	ns	10
t <sub>OEH</sub>	$\overline{\text{OE}}$ Command Hold Time	6	–	8	–	ns	
t <sub>ODS</sub>	Output Disable Set-Up Time	0	–	0	–	ns	
t <sub>WRP</sub>	$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	5	–	5	–	ns	
t <sub>WRH</sub>	$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle)	6	–	8	–	ns	
t <sub>RNCD</sub>	$\overline{\text{RAS}}$ to next $\overline{\text{CAS}}$ Delay Time (Hyper Page Mode)	40	–	50	–	ns	
t <sub>HPC</sub>	Hyper Page Mode Cycle Time	16	–	20	–	ns	
t <sub>HPRWC</sub>	Hyper Page Mode Read-Modify-Write Cycle Time	47	–	57	–	ns	
t <sub>COH</sub>	Output Data Hold Time	5	–	5	–	ns	
t <sub>REZ</sub>	Output Buffer Turn-off Delay from $\overline{\text{RAS}}$	0	11	0	13	ns	10, 16
t <sub>WEZ</sub>	Output Buffer Turn-off Delay from $\overline{\text{WE}}$	0	11	0	13	ns	10
t <sub>WED</sub>	$\overline{\text{WE}}$ to Data Delay	11	–	13	–	ns	
t <sub>OE</sub>	$\overline{\text{OE}}$ Pulse Width	11	–	13	–	ns	
t <sub>OEP</sub>	$\overline{\text{OE}}$ Precharge Time	6	–	8	–	ns	
t <sub>CPO</sub>	$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ Precharge Time	5	–	5	–	ns	
t <sub>OCH</sub>	$\overline{\text{CAS}}$ Hold Time referenced to $\overline{\text{OE}}$	6	–	8	–	ns	
t <sub>RASS</sub>	$\overline{\text{RAS}}$ Pulse Width ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh)	100	–	100	–	μs	
t <sub>RPS</sub>	$\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self refresh)	69	–	84	–	ns	
t <sub>CHS</sub>	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self refresh)	-50	–	-50	–	ns	

## NOTES:

1. Conditions outside the limits listed under “Absolute Maximum Ratings” may cause permanent damage to the device.
2. All voltages are referenced to  $V_{SS}$ .
3.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on the cycle rate.
4.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.
5. The address can be changed once at most while  $\overline{RAS}=V_{IL}$ . In the case of  $I_{CC4}$ , it can be changed once at most during a Hyper Page Mode cycle ( $t_{HPC}$ ).
6. An initial pause of  $200\mu s$  is required after power-up followed by a minimum of eight  $\overline{RAS}$ -Only refresh cycles before proper device operation is achieved. When using the internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles instead of eight  $\overline{RAS}$ -Only refresh cycles is required.
7. AC measurements assume  $t_T=2ns$ .
8.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between the  $V_{IH}$  and  $V_{IL}$  levels.
9. This is measured with a load equivalent to  $100pF$  at  $V_{OH} = 2.0V$  ( $I_{OUT} = -2mA$ ),  $V_{OL} = 0.8V$  ( $I_{OUT} = 2mA$ ).
10.  $t_{OFF}$  (max),  $t_{OEZ}$  (max),  $t_{REZ}$  (max) and  $t_{WEZ}$  (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a Read cycle.
12. These parameters are referenced to the leading edge of  $\overline{CAS}$  in Early Write cycles and to the leading edge of  $\overline{WE}$  in Read-Modify-Write cycles.
13.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\min)$ , the cycle is an Early Write cycle and the Data-out pin will remain open circuit (high impedance) throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\min)$ ,  $t_{CWD} \geq t_{CWD}(\min)$ ,  $t_{AWD} \geq t_{AWD}(\min)$  and  $t_{CPWD} \geq t_{CPWD}(\min)$  (Hyper Page mode), the cycle is a Read-Modify-Write cycle and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the data output (at access time) is indeterminate.
14. Operation within the  $t_{RCD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, then the access time is determined by  $t_{CAC}$ .
15. Operation within the  $t_{RAD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then the access time is determined by  $t_{AA}$ .
16. If  $\overline{RAS}$  goes high before  $\overline{CAS}$  goes high, the output goes open circuit when  $\overline{CAS}$  goes high ( $t_{OFF}$ ). If  $\overline{CAS}$  goes high before  $\overline{RAS}$  goes high, the output goes open circuit when  $\overline{RAS}$  goes high ( $t_{REZ}$ ).

DATA-OUT HI-Z CONTROL LOGIC

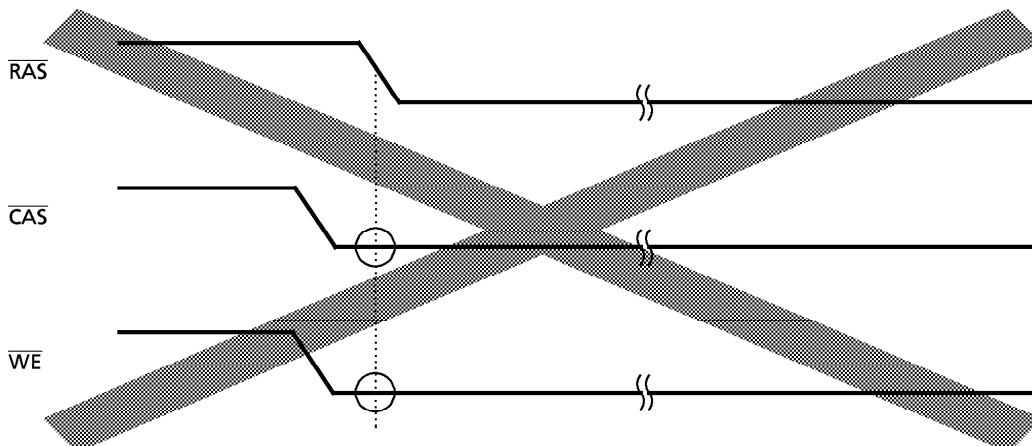
$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
H		L	H	$t_{OFF}$
	H	L	H	$t_{REZ}$
L	L		H	$t_{OEZ}$
L	H	L		$t_{WEZ}$

DATA-OUT LO-Z CONTROL LOGIC

$\overline{RAS}$	$\overline{CAS}$	$\overline{OE}$	$\overline{WE}$	Timing Specification
L		L	H	$t_{CLZ}$
L	L		H	$t_{OLZ}$
L	L		H	$t_{OLZ}$

**CAUTION**

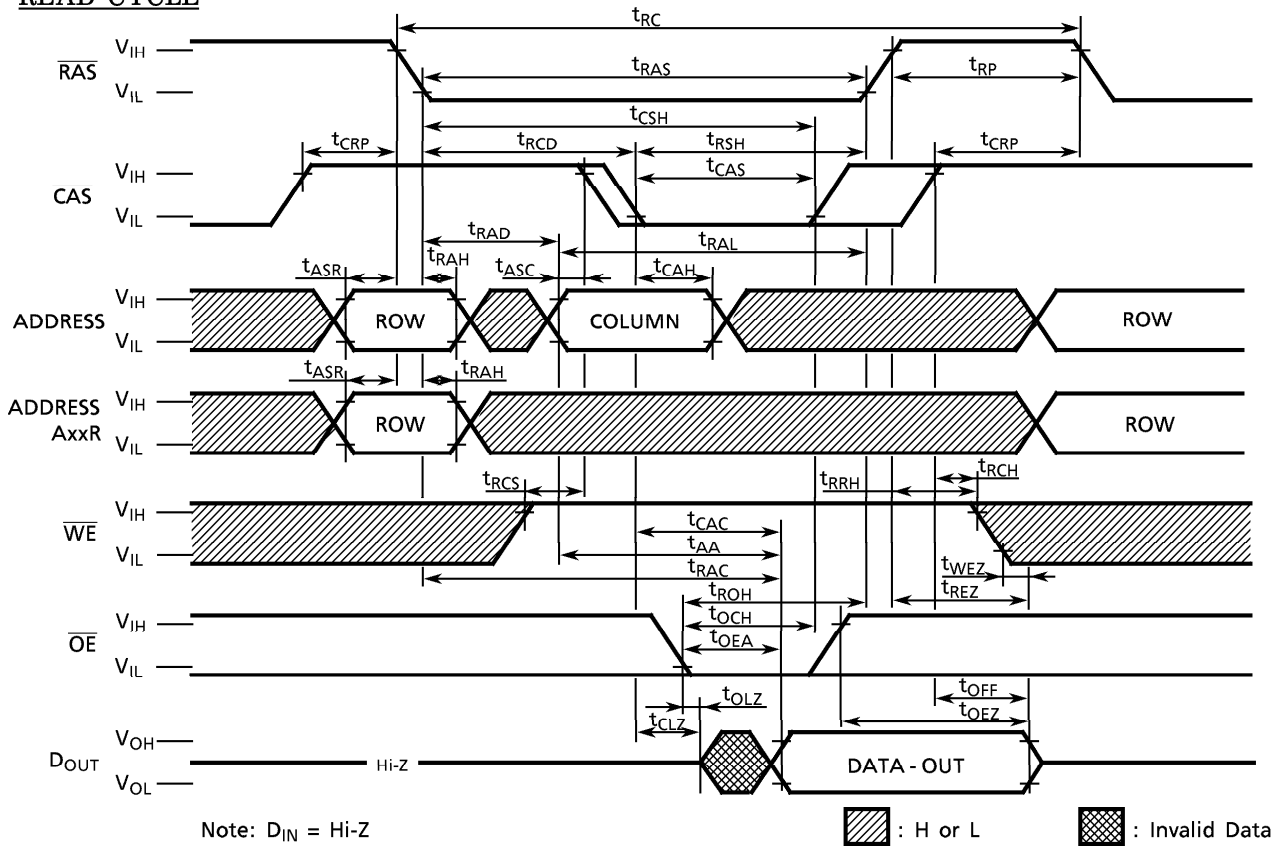
The WCBR ( $\overline{WE}$ ,  $\overline{CAS}$ -before- $\overline{RAS}$ ) timing shown below is not allowed during normal operation, such as during Read, Write and Refresh operations. When WCBR is input, a malfunction may occur due to the change in internal circuit operation status.



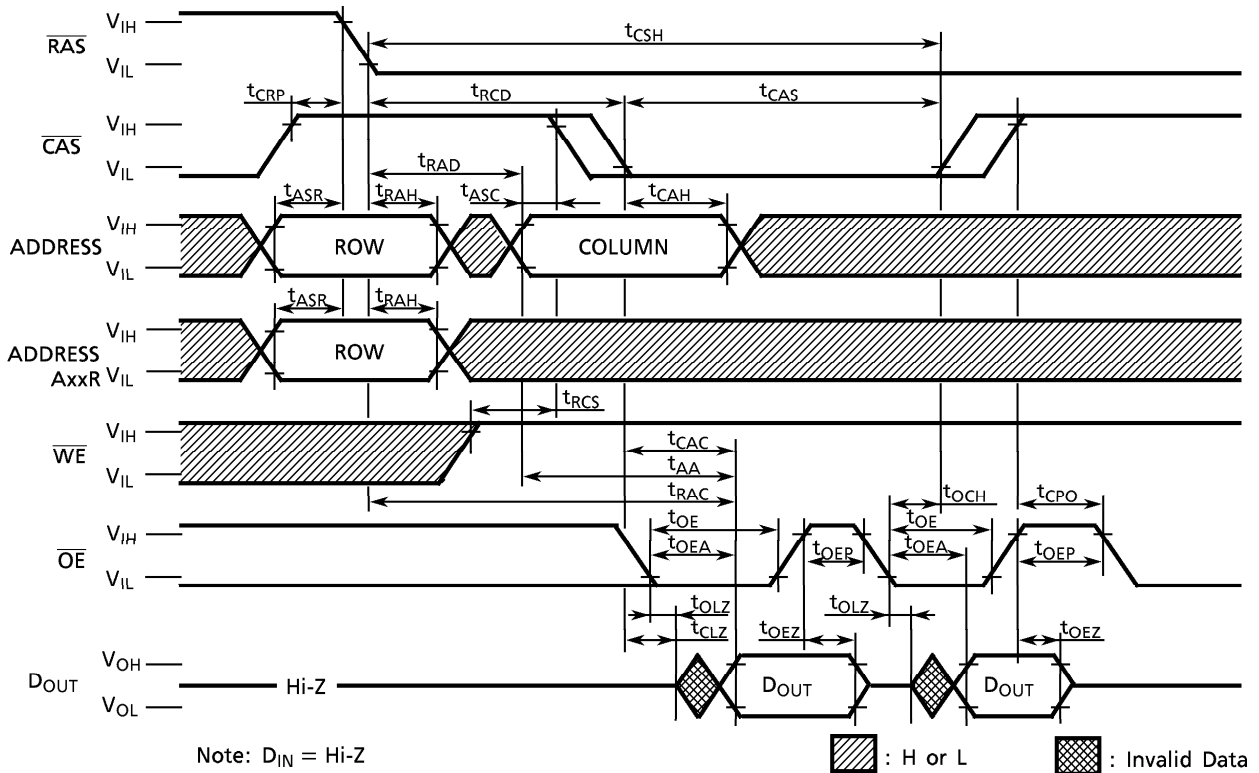
**WCBR timing**

### TIMING DIAGRAMS

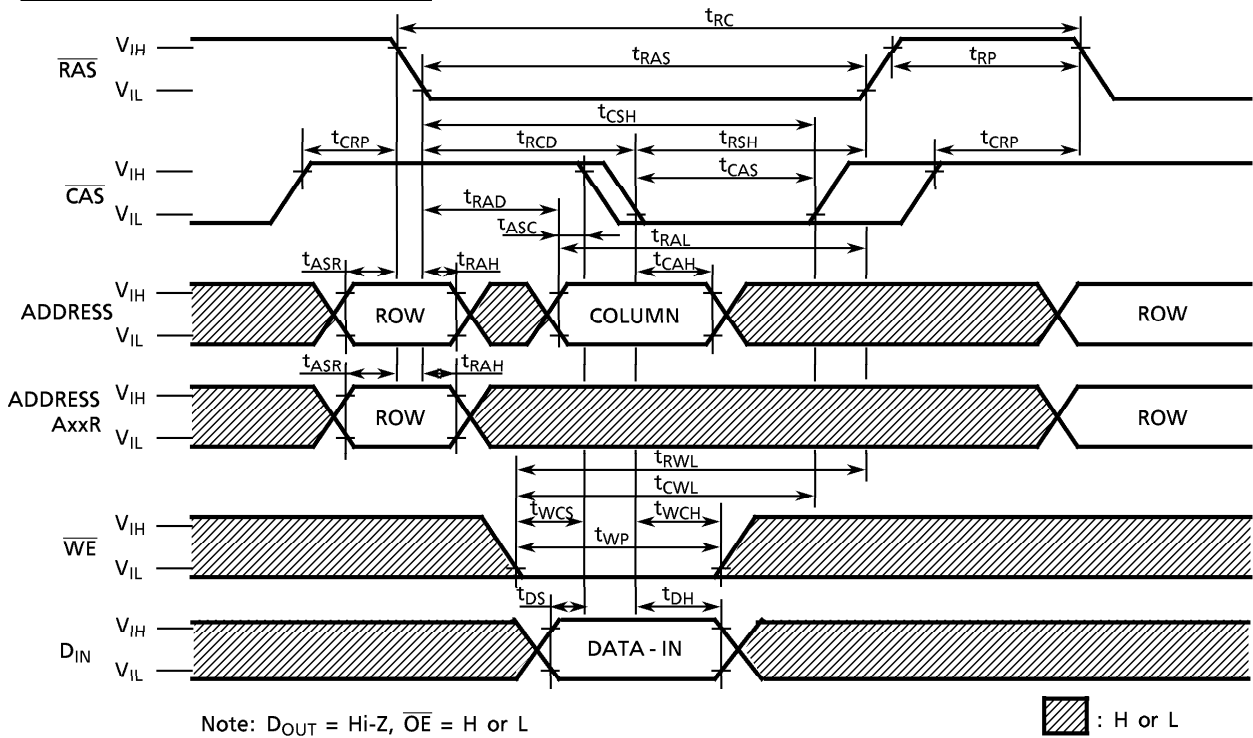
#### READ CYCLE



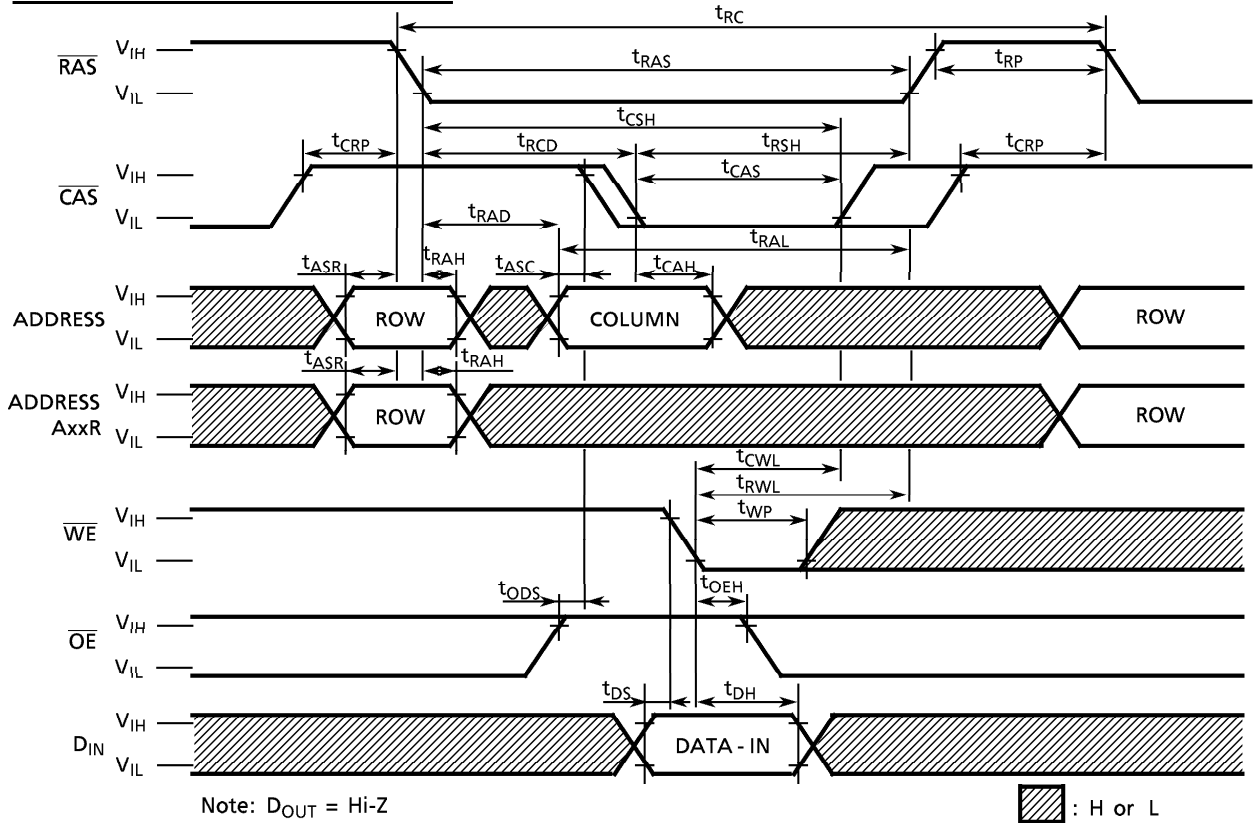
#### $\overline{\text{OE}}$ -CONTROLLED READ CYCLE



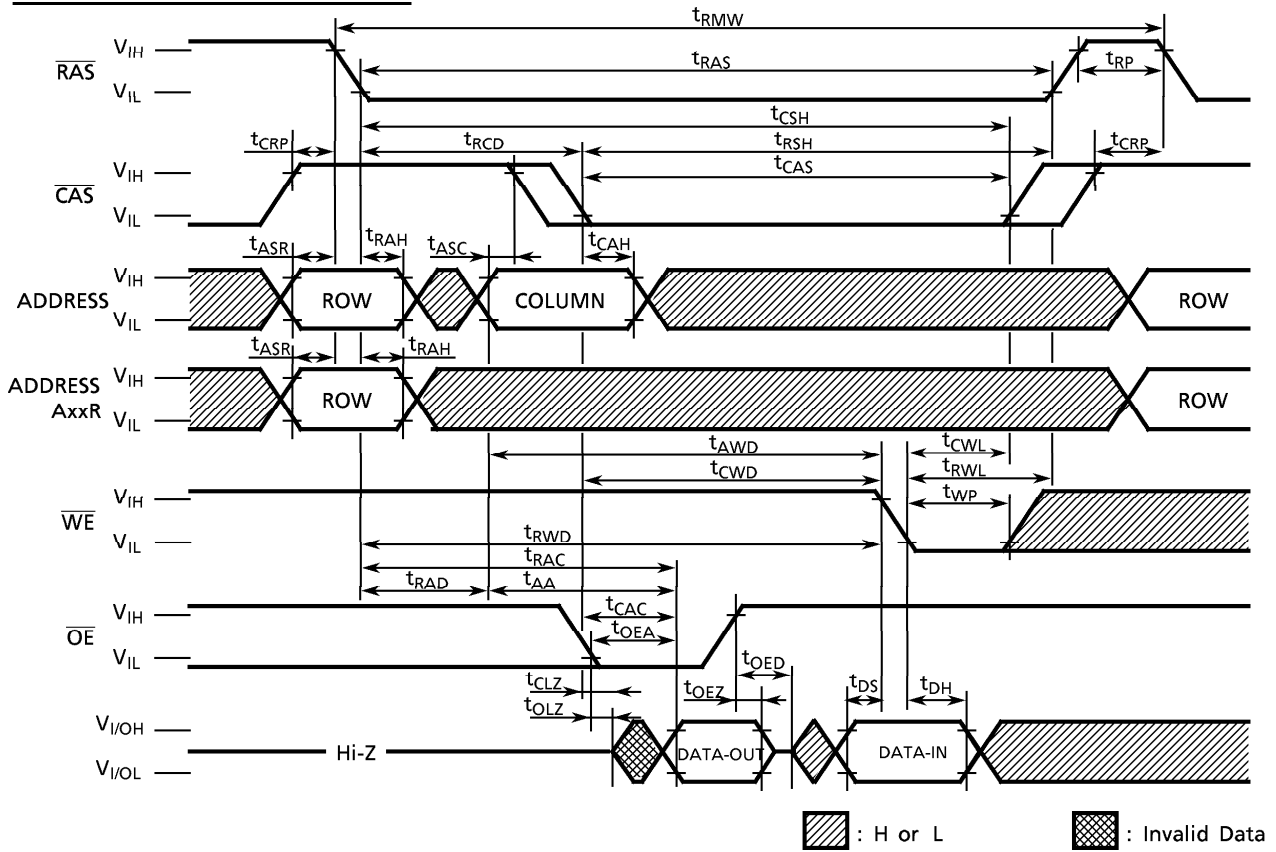
WRITE CYCLE (EARLY WRITE)



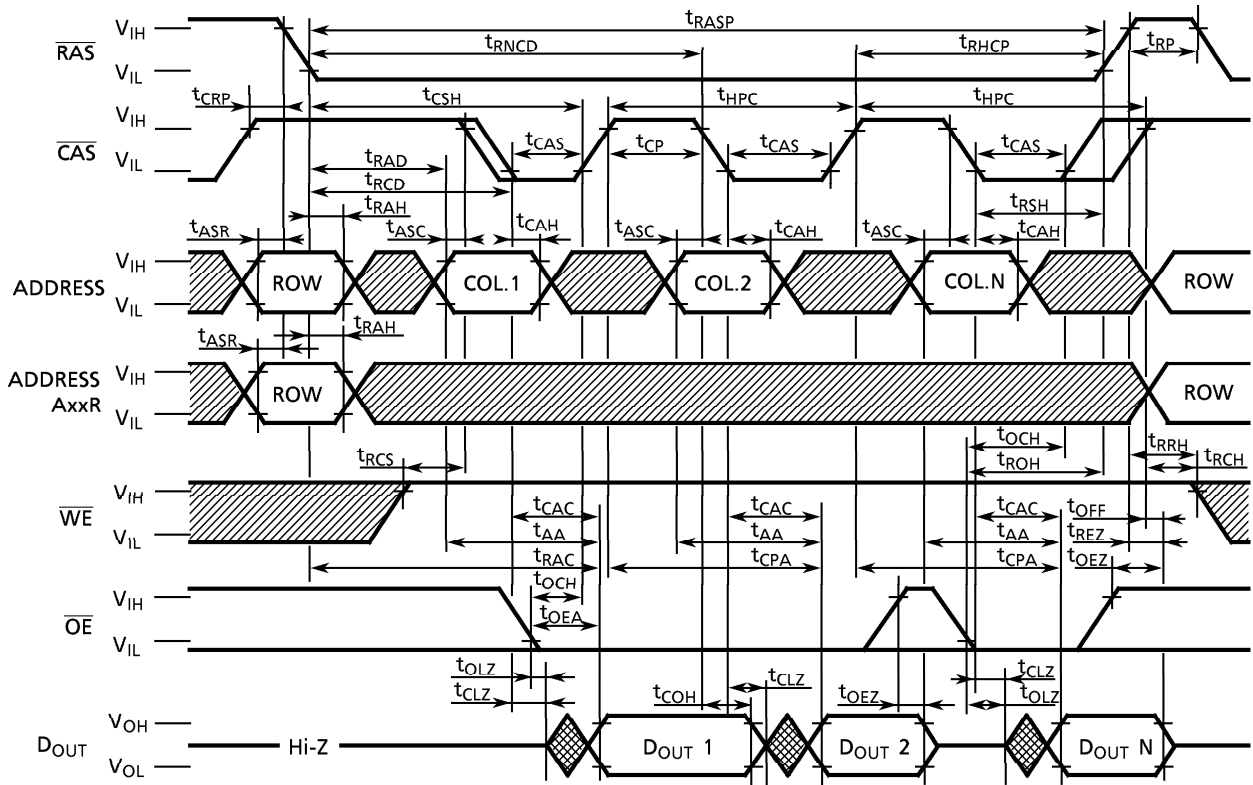
$\overline{\text{OE}}$ -CONTROLLED WRITE CYCLE



**READ-MODIFY-WRITE CYCLE**



**HYPER PAGE MODE READ CYCLE**

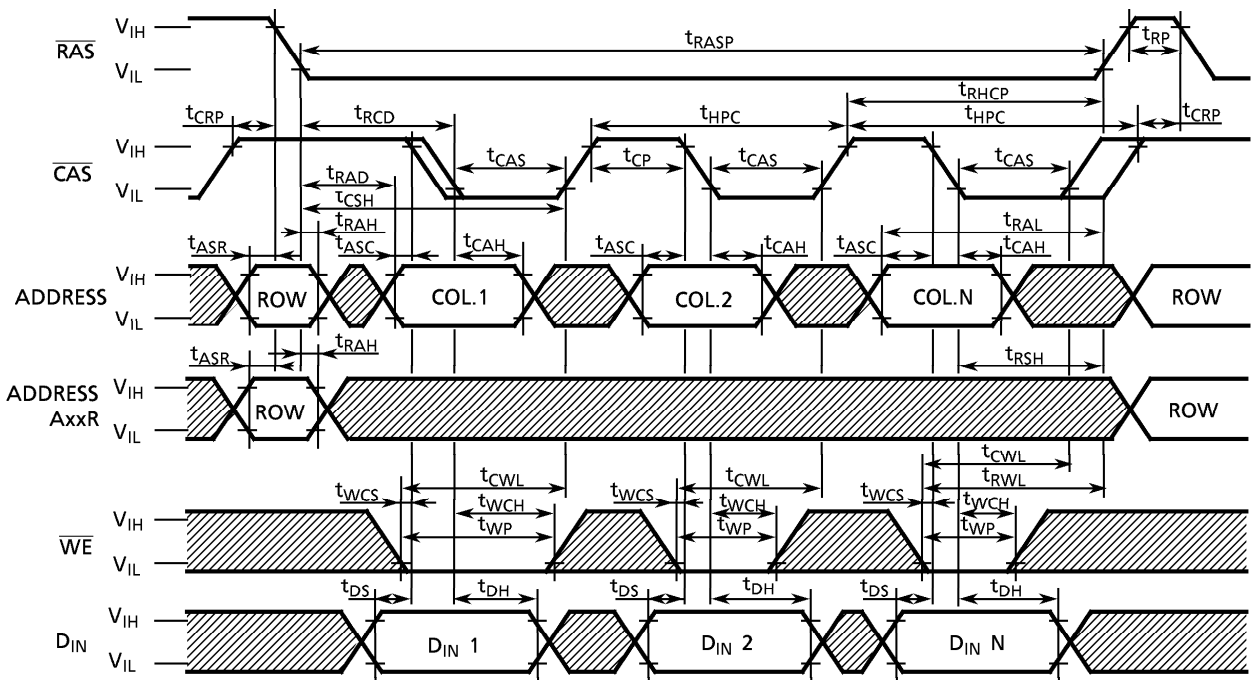


Note:  $D_{\text{IN}} = \text{Hi-Z}$

▨ : H or L

▩ : Invalid Data

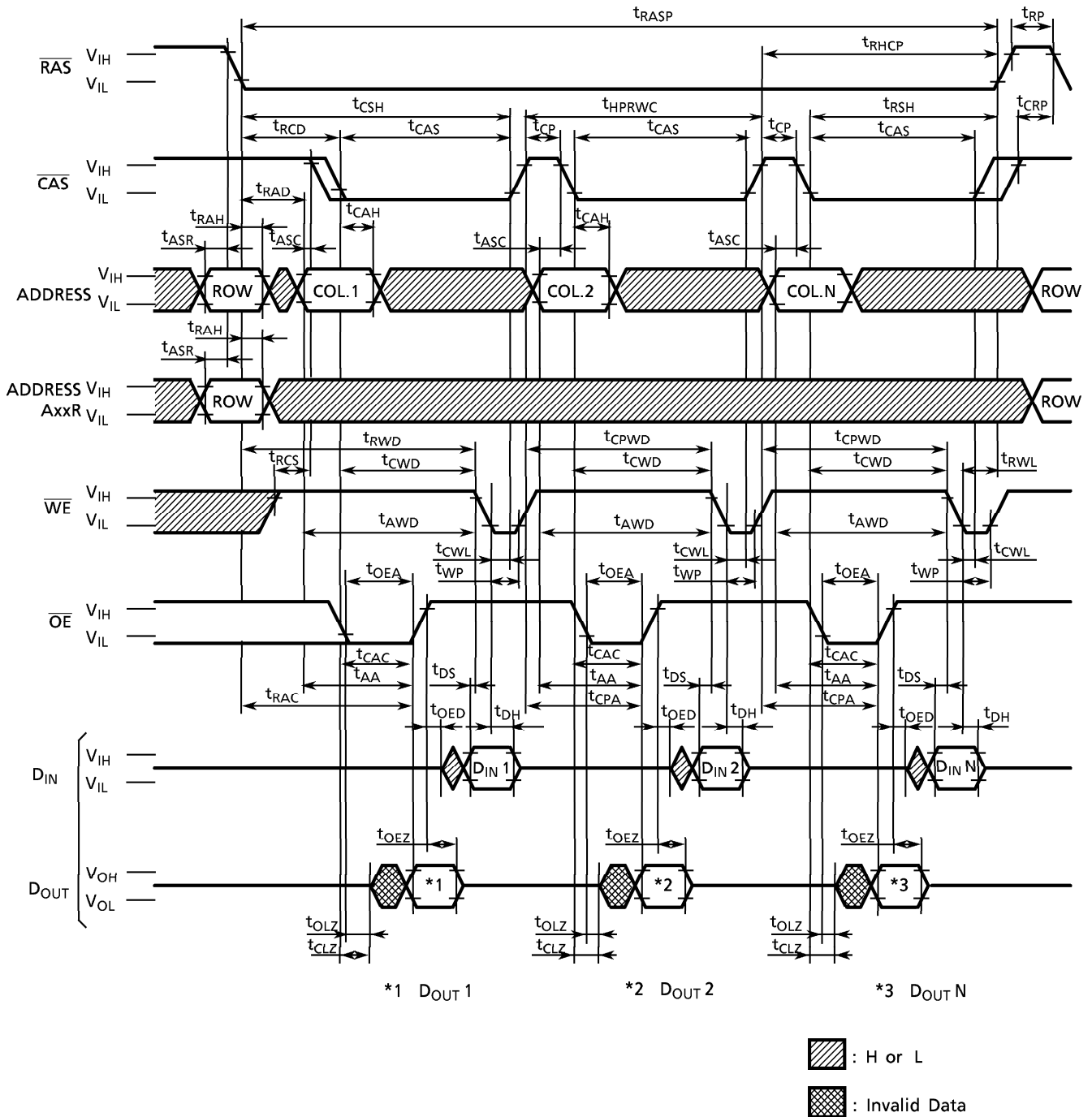
**HYPER PAGE MODE WRITE CYCLE (EARLY WRITE)**



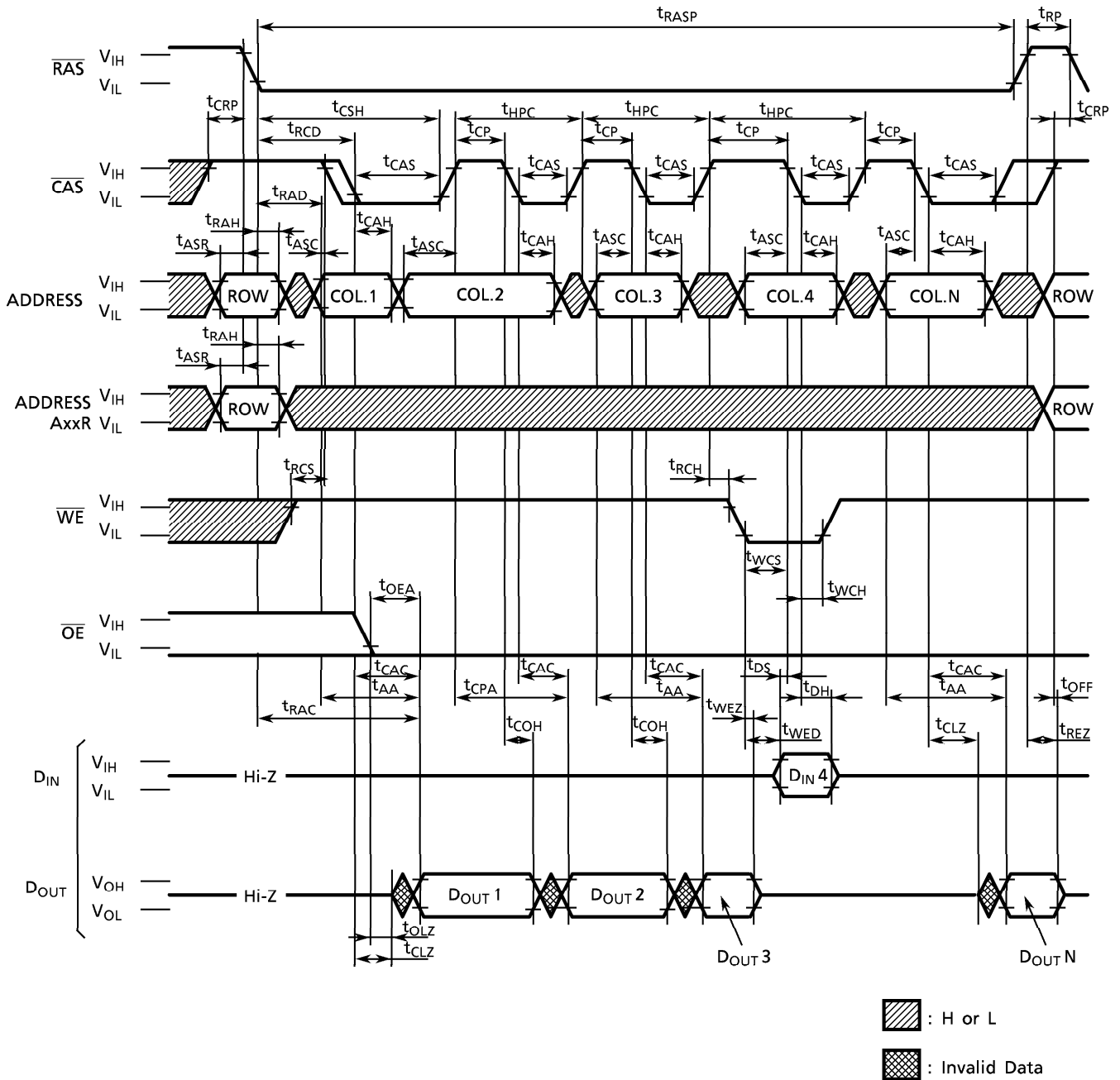
Note:  $D_{\text{OUT}} = \text{Hi-Z}$ ,  $\overline{\text{OE}} = \text{H or L}$

▨ : H or L

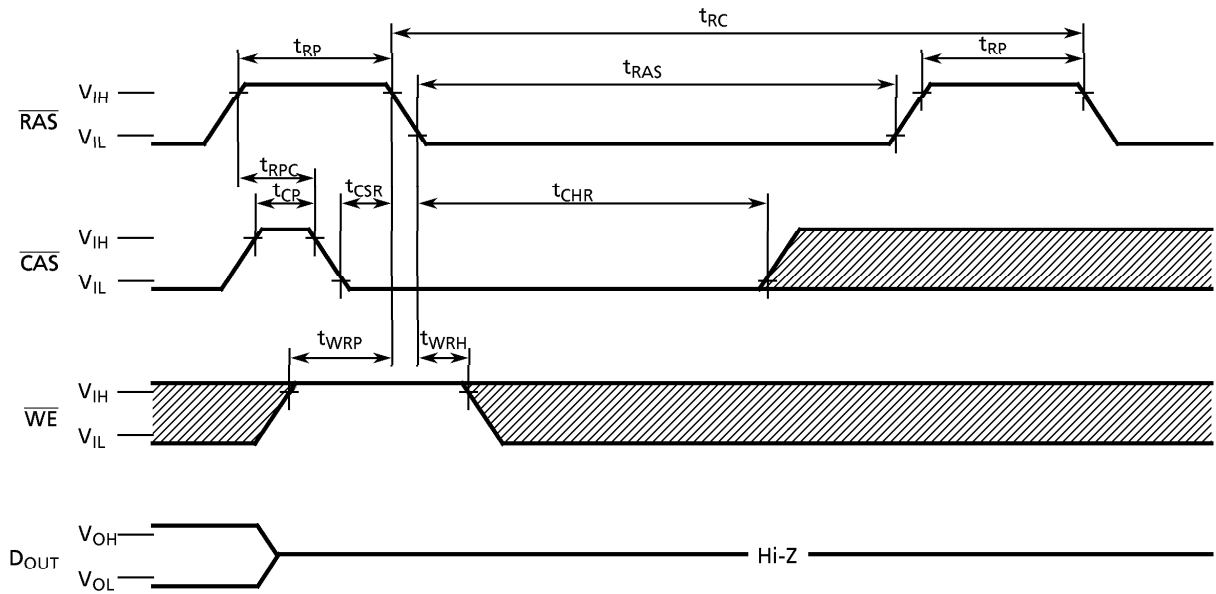
HYPER PAGE MODE READ-MODIFY-WRITE CYCLE



### HYPER PAGE MODE READ-WRITE MIXED CYCLE



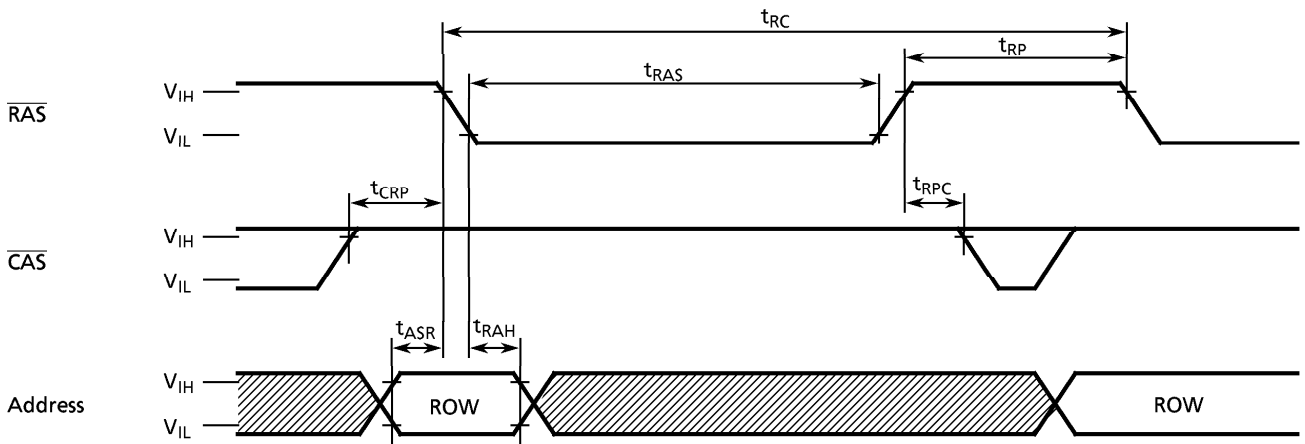
CAS-BEFORE-RAS REFRESH CYCLE



Note:  $\text{D}_{\text{IN}}$ ,  $\overline{\text{OE}}$ , ADDRESS = H or L

: H or L

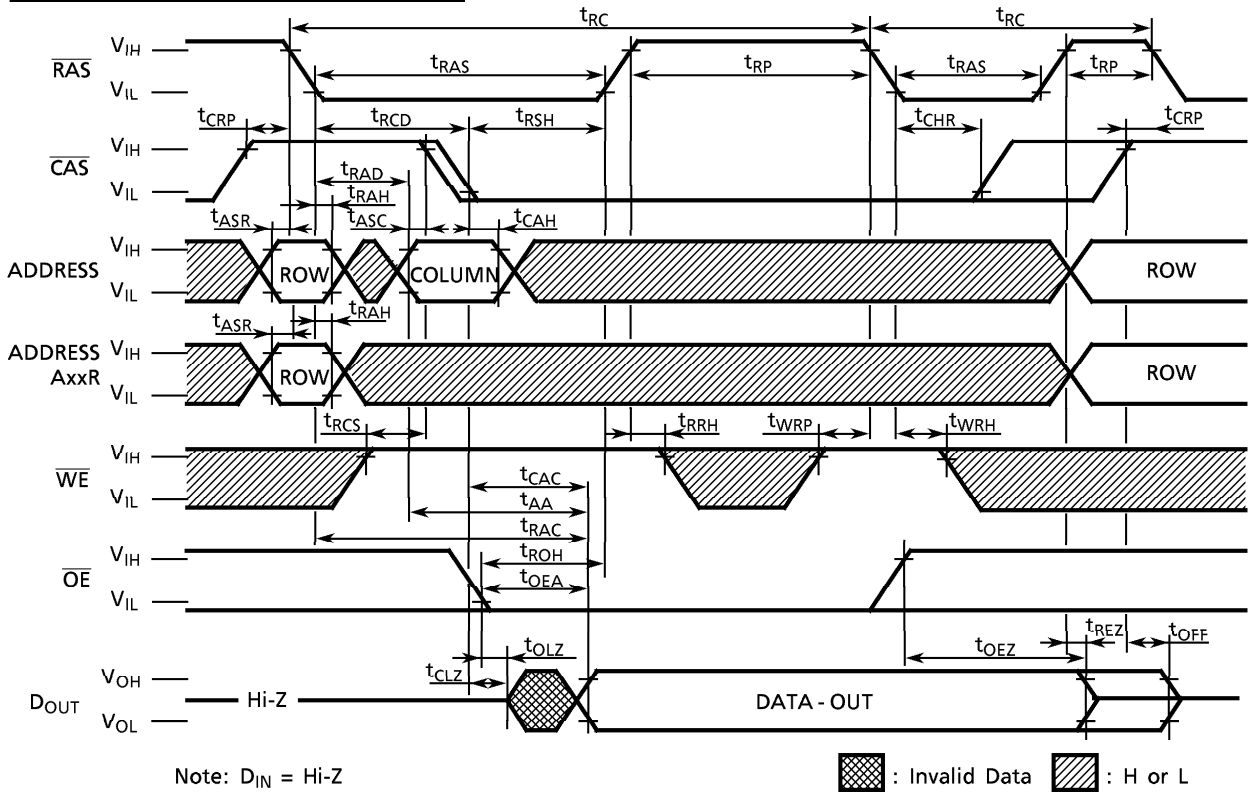
RAS-ONLY REFRESH CYCLE



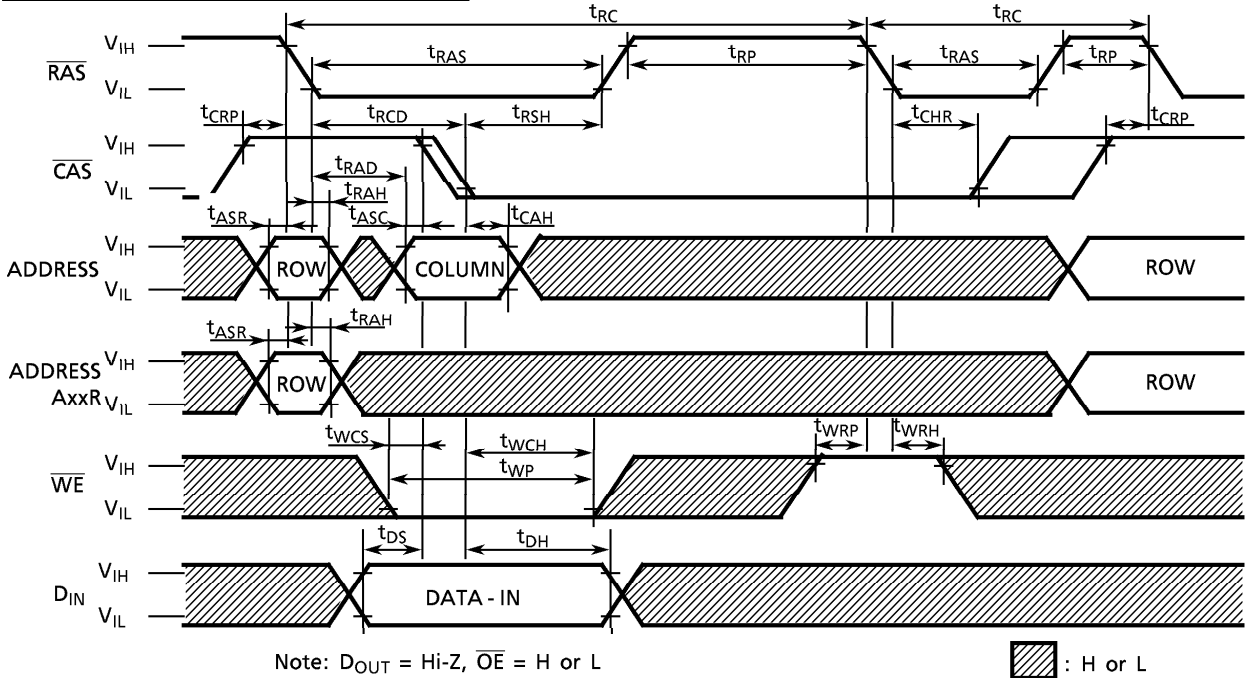
Note:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  and  $\text{D}_{\text{IN}} = \text{H or L}$

: H or L

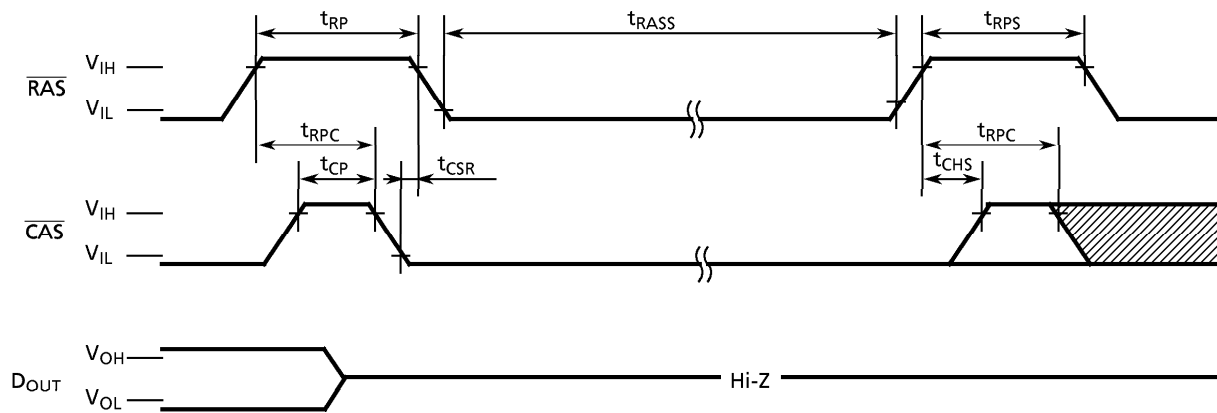
**HIDDEN REFRESH CYCLE (READ)**



**HIDDEN REFRESH CYCLE (WRITE)**



CAS-BEFORE-RAS SELF-REFRESH CYCLE (THL64VxxxxBTG-xS only)



Note:  $D_{IN}$ ,  $\overline{WE}$ ,  $\overline{OE}$ , ADDRESS = H or L

 : H or L

# **SERIAL PRESENCE DETECT AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS No.100**

961001EBA1

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DC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 3.3\text{ V} \pm 0.15\text{ V}$ )

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
$V_{IH}$	Input High Voltage	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V	
$V_{IL}$	Input Low Voltage	-0.3	$V_{CC} \times 0.3$	V	
$V_{OL}$	Output Low Voltage ( $I_{OL} = 200\ \mu\text{A}$ )	-	0.4	V	1

Note:

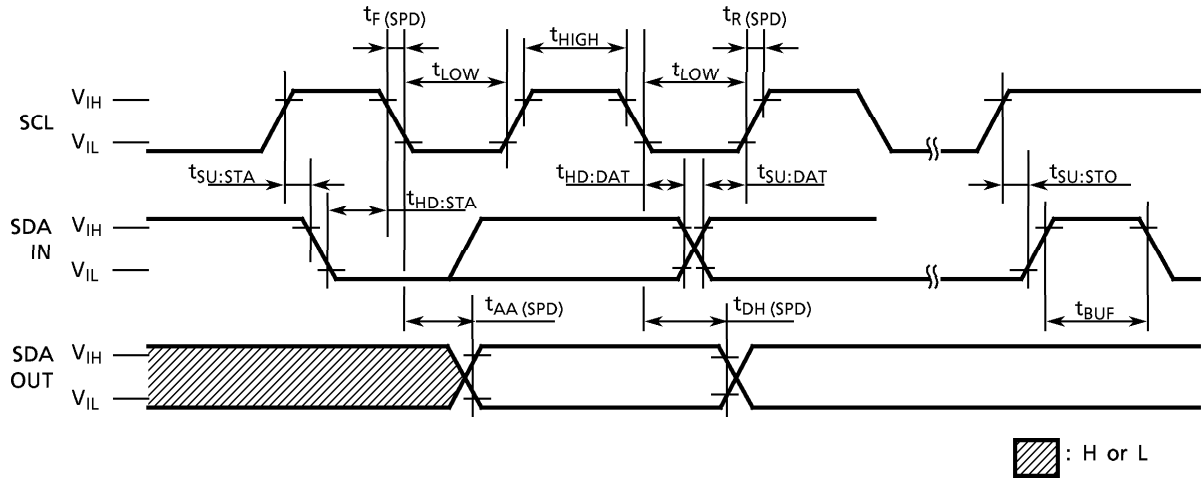
1. Output Load: 1TTL Gate and  $C_L = 100\text{ pF}$

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

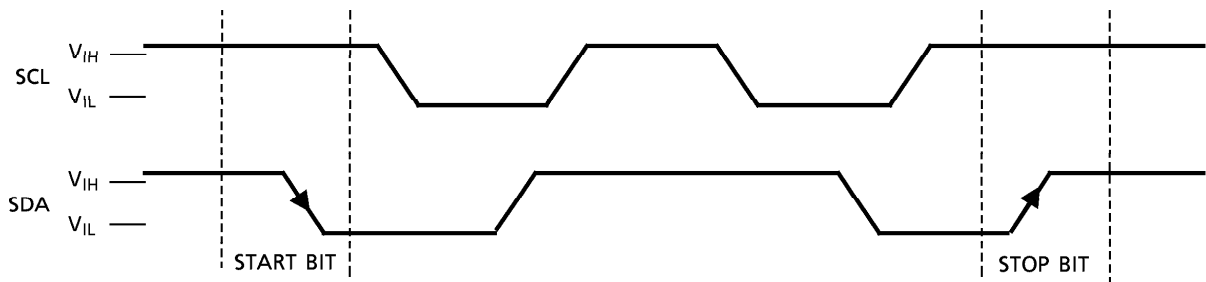
SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
$t_{SCL}$	SCL Clock Frequency	-	80	KHz	
$t_{LOW}$	Clock Low Period	6.7	-	$\mu\text{s}$	
$t_{HIGH}$	Clock High Period	4.5	-	$\mu\text{s}$	
$t_{AA}(\text{SPD})$	SCL Low to SDA Data Out Valid	0.3	7.0	$\mu\text{s}$	
$t_{HD:STA}$	Start Condition Hold Time	4.5	-	$\mu\text{s}$	
$t_{SU:STA}$	Start Condition Set-up Time (for a Repeated Start Condition)	6.7	-	$\mu\text{s}$	
$t_{SU:STO}$	Stop Condition Set-up Time	6.7	-	$\mu\text{s}$	
$t_{HD:DAT}$	Data-in Hold Time	0	-	$\mu\text{s}$	
$t_{SU:DAT}$	Data-in Set-up Time	500	-	ns	
$t_{DH}(\text{SPD})$	Data-out Hold Time	300	-	ns	
$t_R(\text{SPD})$	SDA and SCL Rise Time	-	1	$\mu\text{s}$	
$t_F(\text{SPD})$	SDA and SCL Fall Time	-	300	ns	
$t_{BUF}$	Time the Bus Must Be Free before a New Transmission Can Start	6.7	-	$\mu\text{s}$	

TIMING DIAGRAMS

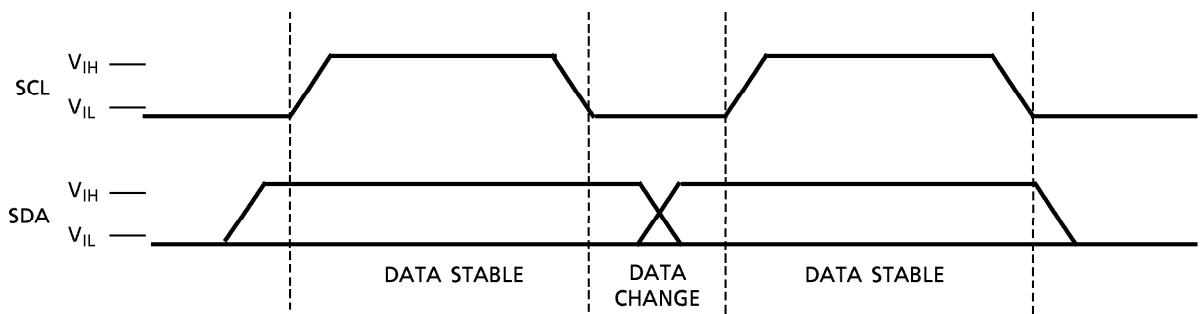
BUS TIMING



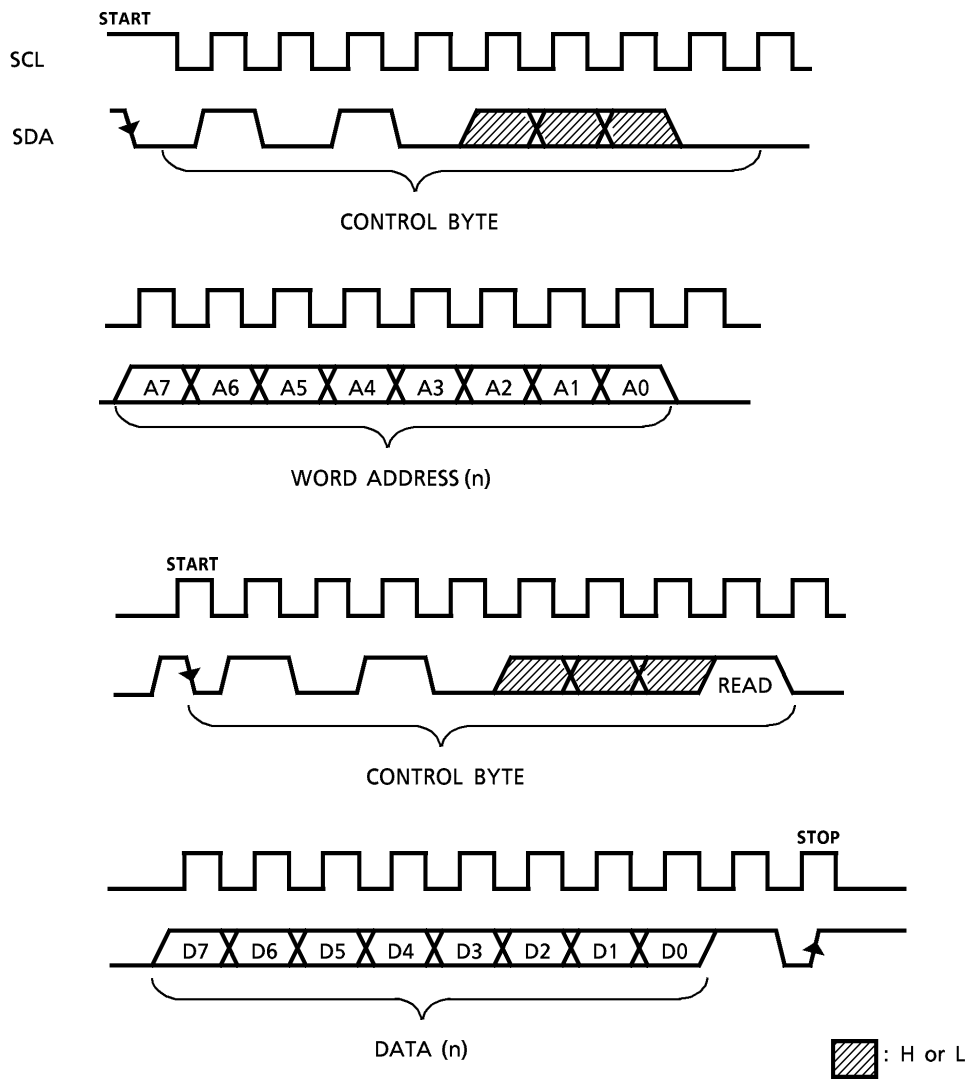
DEFINITION OF START AND STOP



DATA VALIDITY

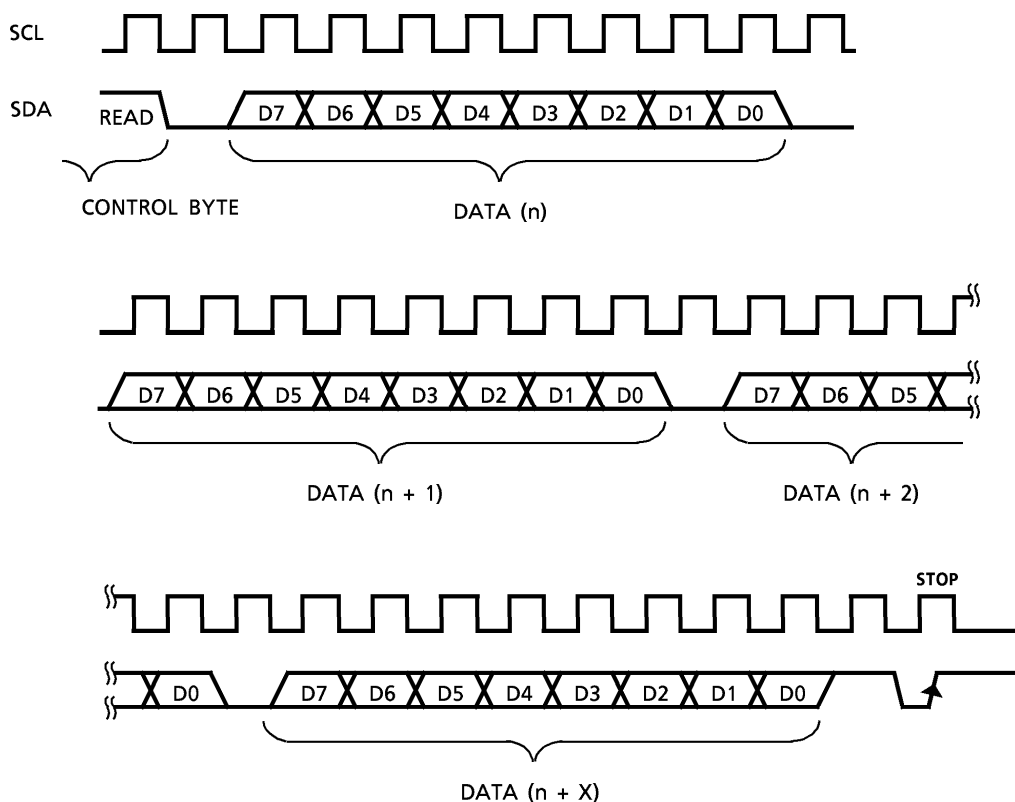


RANDOM READ



NOTE: Random read operations allow the master to access Serial PD DATA in a random manner. To perform this type of read operation, first the word address must be set. (Dummy Write Operation) After the word address is sent, the master generates a start condition following the acknowledge. Then the master issues the control byte again but with READ bit set to a one. E<sup>2</sup>PROM will then issue an acknowledge and transmits the eight bit data word.

SEQUENTIAL READ



NOTE: Sequential reads can be initiated as random access read. The first word is transmitted in the same manner as the other read mode; however, the master now responds with an acknowledge, indicating it requires additional data. E<sup>2</sup>PROM continues to output data for each acknowledge received. The read operation is terminated by generating a stop condition.