8825 DC CLOCKED J-K BINARY

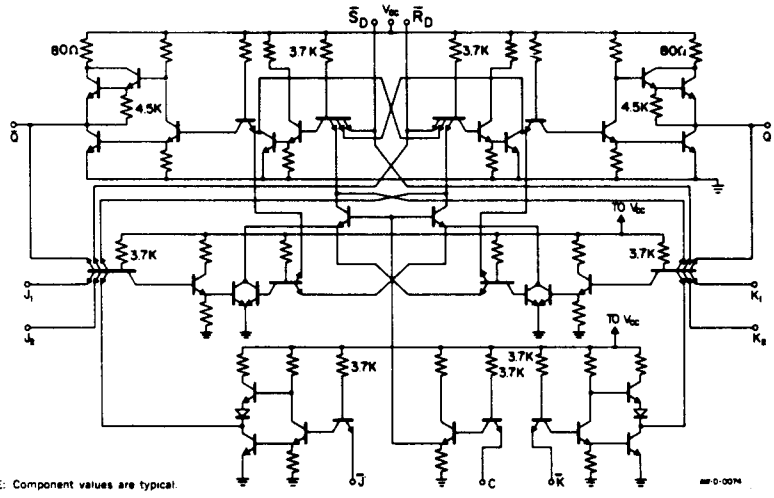
004105

The 8825 is a high-speed, direct-coupled, J-K Binary which responds to the positive transition (rising edge) of the clock pulse. For logic flexibility, two J, two K, an inverting J and an inverting K, inputs are provided. Separate set (S_D) and reset (R_D) lines are available when asynchronous operation is required. To prevent system errors, logic inputs are locked out approximately 10ns after the clock threshold voltage is reached. This feature prevents more than one logic transition per clock pulse.

The characterization of each logic element in the 8000-Series includes loading rules for driving the 8825. A convenient summary of these DC loading rules is provided in Table 1-4, Section 1.

Applications and usage rules for the 8825 may be found in Section 4.

BASIC CIRCUIT SCHEMATIC



NOTE: Component values are typical.

TRUTH TABLE

J_n	K_n	Q_{n+1}	$\bar{S}_D$	$\bar{R}_D$	Q
0	0	Q_n	0	0	†
1	0	1	1	0	0
0	1	0	0	1	1
1	1	$\bar{Q}_n$	1	1	Q

$J = J_1 J_2 \bar{J}$ $\quad K = K_1 K_2 \bar{K}$

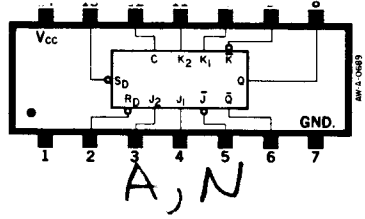
n is time prior to clock

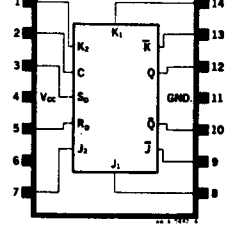
n + 1 is time following clock

† Both outputs in 0 state

ELECTRICAL CHARACTERISTICS (NOTES: 1, 2, 3, 4, 5, 6, 14)

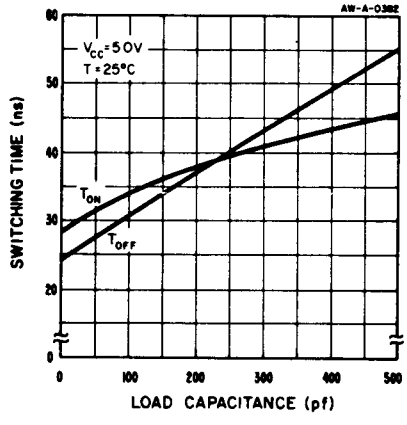
ACCEPTANCE TEST SUB-GROUP	CHARACTERISTIC	LIMITS				TEST CONDITIONS											
		MIN.	TYP.	MAX.	UNITS	TEMP. S8825	TEMP. N8825	V_{cc}	SET	RESET	DRIVEN INPUT	J_1, J_2	$\bar{J}$	K_1, K_2	$\bar{K}$	CLOCK	OUTPUT	NOTES
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	0.8V	2.0V						0V	-500μA	8
A-3	(Q)	2.8			V	+25°C	+25°C	5.0V	0.8V	2.0V						0V	-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	0.8V	2.0V						0V	-500μA	8
A-5	"1" OUTPUT VOLTAGE	2.6			V	-55°C	0°C	4.75V	2.0V	0.8V						0V	-500μA	8
A-3	($\bar{Q}$)	2.8			V	+25°C	+25°C	5.0V	2.0V	0.8V						0V	-500μA	8
A-4		2.6			V	+125°C	+75°C	4.75V	2.0V	0.8V						0V	-500μA	8
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	2.0V	0.8V						0V	16mA	9
A-3	(Q)			0.40	V	+25°C	+25°C	5.0V	2.0V	0.8V						0V	16mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	2.0V	0.8V						0V	16mA	9
A-5	"0" OUTPUT VOLTAGE			0.40	V	-55°C	0°C	4.75V	0.80V	2.0V						0V	16mA	9
A-3	($\bar{Q}$)			0.40	V	+25°C	+25°C	5.0V	0.80V	2.0V						0V	16mA	9
A-4				0.40	V	+125°C	+75°C	4.75V	0.80V	2.0V						0V	16mA	9
C-1	"0" INPUT CURRENT			-1.6	mA	-55°C	0°C	5.25V			0.40V							12
A-3	$J_1, J_2, \bar{J}, K_1, K_2, \bar{K}$, CLOCK			-1.6	mA	-25°C	+25°C	5.25V			0.40V							12
C-1				-1.6	mA	+125°C	+75°C	5.25V			0.40V							12
C-1	"0" INPUT CURRENT			-3.2	mA	-55°C	0°C	5.25V			0.40V		0V		0V	0V		
A-3	SET, RESET			-3.2	mA	-25°C	+25°C	5.25V			0.40V		0V		0V	0V		
C-1				-3.2	mA	+125°C	+75°C	5.25V			0.40V		0V		0V	0V		
A-4	"1" INPUT CURRENT $J_1, J_2, \bar{J}, K_1, K_2, \bar{K}$, CLOCK			40	μA	+125°C	+75°C	5.0V			4.5V							
A-4	"1" INPUT CURRENT SET, RESET			80	μA	+125°C	+75°C	5.0V			4.5V					0V		
A-6	TURN-ON DELAY			50	ns	+25°C	+25°C	5.0V									D.C. F.O.=20	15
A-6	TURN-OFF DELAY			50	ns	+25°C	+25°C	5.0V									D.C. F.O. = 20	15
C-2	OUTPUT FALL TIME			50	ns	-55°C	0°C	4.75V									A.C. F.O.=6	11, 15
A-6	TOGGLE RATE	15			mHz	+25°C	+25°C	5.0V										15
	MINIMUM INPUT SET-UP TIME		15		ns	+25°C	+25°C	5.0V										15
	MINIMUM INPUT HOLD TIME		10		ns	+25°C	+25°C	5.0V										15
C-2	INPUT CAPACITANCE $J_1, J_2, \bar{J}, K_1, K_2, \bar{K}$, CLOCK			3.0	pf	+25°C	+25°C	5.0V			2.0V							7
C-2	INPUT CAPACITANCE SET, RESET			6.0	pf	+25°C	+25°C	5.0V			2.0V							
A-2	POWER CONSUMPTION		70	132	mW	+25°C	+25°C	5.25V								0V		
C-1	INPUT LATCH VOLTAGE ALL INPUTS	5.5			V	+25°C	+25°C	5.0V			10mA							13
A-2	OUTPUT SHORT CIRCUIT CURRENT Q	-20		-70	mA	+25°C	+25°C	5.0V	0V							0V	0V	
	$\bar{Q}$	-20		-70	mA	+25°C	+25°C	5.0V		0V						0V	0V	

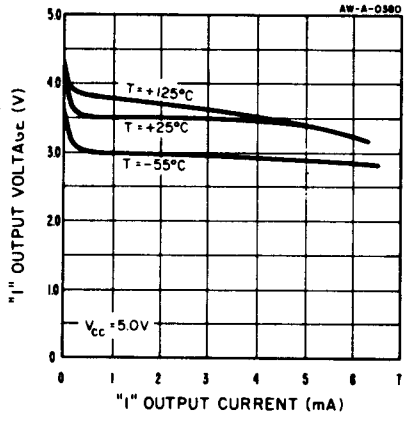


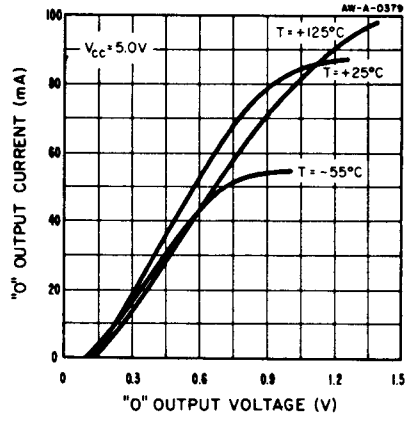


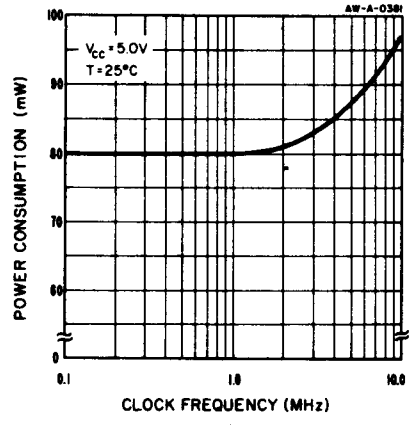
Notes:

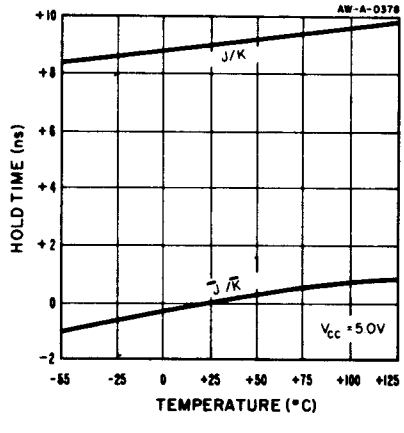
1. All voltage and capacitance measurements are referenced to the ground terminal Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND Logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Capacitance as measured on Boonton Electronic Corporation Model 75A-S8 Capacitance Bridge or equivalent. f = 1MHz, V_{AC} = 25mV rms. All pins not specifically referenced are tied to guard for capacitance tests. Output pins are left open.
8. Output source current is supplied through a resistor ground.
9. Output sink current is supplied through a resistor to V_{CC}.
10. One DC fan-out is defined as 0.8mA.
11. One AC fan-out is defined as 50pf.
12. Input current measurements at J_1, J_2 require $\overline{J}$ = CLOCK = zero volts and momentarily ground RESET. Input current measurements at K_1, K_2 require $\overline{K}$ = CLOCK = zero volts and momentarily ground SET.
13. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
14. Manufacturer reserves the right to make design and process changes and improvements.
15. Detailed test conditions for AC testing are in Section 3.

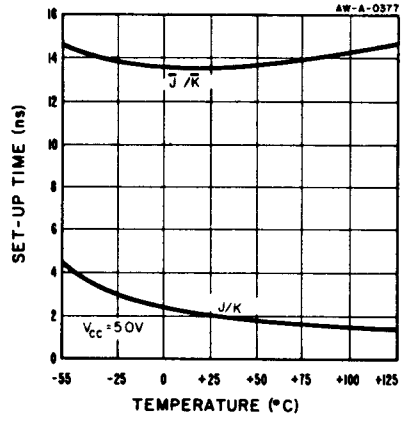


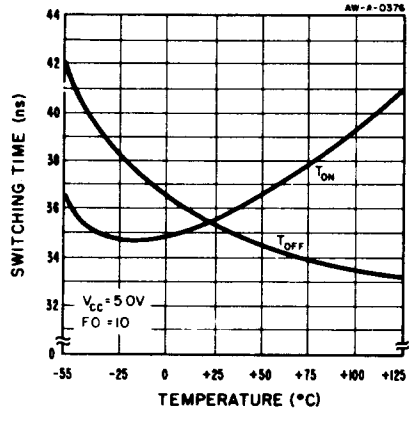












2