REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03, 04, 05, and 06. Add packages U and Z. Rewrite entire document.	94-02-04	K. A. Cottongim
B	Changes in accordance with NOR 5962-R064-95.	95-01-31	K. A. Cottongim
C	Add device types 07, 08, 09, and 10.	97-03-21	K. A. Cottongim

REV	C	C	C	C	C	C	C	C												
SHEET	35	36	37	38	39	40	41	42												
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
91-09-19

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, DIGITAL, MIL-STD-1553, MUX BUS, REMOTE TERMINAL

SIZE	CAGE CODE	
A	**67268**	**5962-91687**

SHEET 1 OF 42

DESC FORM 193
JUL 94

5962-E101-97

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	91687	01	H	X	C
*	*		*	*	*	*
*	*		*	*	*	*
*	*		*	*	*	*
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

_____ _____/
\V
Drawing number

1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	NHI-1553RT	MIL-STD-1553, dual redundant, remote terminal, seperate V_{CC} for internal RAM, hybrid transceivers.
02	NHI-1554RT	MIL-STD-1553, dual redundant, remote terminal, seperate input pin for SSFlag/Terminal Flag, hybrid transceivers.
03	NHI-1561RT	MIL-STD-1553, dual redundant, remote terminal, multichip, monolithic transceivers.
04	NHI-1562RT	MIL-STD-1553, dual redundant, remote terminal, multichip, monolithic transceivers, MacAir.
05	NHI-1572RT	MIL-STD-1553, dual redundant, remote terminal, seperate V_{CC} for internal RAM, multichip, monolithic transceivers.
06	NHI-1576RT	MIL-STD-1553, dual redundant, remote terminal, seperate input pin for SSFlag/Terminal Flag, multichip, monolithic transceivers.
07	NHI-1591RT	MIL-STD-1553, dual redundant, remote terminal, multichip, monolithic transceivers with separation of broadcast data pointer tables.
08	NHI-1592RT	MIL-STD-1553, dual redundant, remote terminal, multichip, monolithic. transceivers, MacAir, with separation of broadcast data pointer tables
09	NHI-15101RT	MIL-STD-1553, dual redundant, remote terminal, multichip, monolithic. transceivers with separation of broadcast data pointer tables and external time tag clock input.
10	NHI-15102RT	MIL-STD-1553, dual redundant, remote terminal, multichip, monolithic transceivers, MacAir, with separation of broadcast data pointer tables and external time tag clock input.

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	68	Flat pack
X	See figure 1	66	Dual-in-line
Y	See figure 1	66	Flat pack
Z	See figure 1	69	Grid array

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +7 V dc
Storage temperature range	-65°C to +150°C
Thermal rise, case-to-junction	+15°C/W
Lead soldering temperature (10 seconds)	+300°C
Power dissipation (P_D):	
Device types 01 and 02, (T_C = +125°C)	1.3 W
Device types 03, 04, 05, 06, 07, 08, 09, and 10:	
Hottest die (100% duty cycle)	0.500 W
Total hybrid (standby)	0.550 W
Total hybrid (100% duty cycle)	1.05 W
Thermal resistance, junction-to-case (θ_{JC})	4°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}):	
Device types 01 and 02	+4.75 V dc to +5.50 V dc
Device types 03, 04, 05, 06, 07, 08, 09, and 10	+4.50 V dc to +5.50 V dc
Minimum logic high input voltage (V_{IH})	+2 V dc
Maximum logic low input voltage (V_{IL})	+0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.
MIL-HDBK-1553 - Multiplex Applications Handbook.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Compliance to MIL-HDBK-1553, Appendix A. The part manufacturer described herein (and/or) listed in QML-38534 shall certify that the parts listed herein have been tested in accordance with and meet the requirements of MIL-HDBK-1553, Appendix A, Remote Terminal Validation Test Plan. This data shall be maintained under document revision control by the manufacturer and be made available upon request.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input voltage high	V_{IH}	V_{CC} = 5.5 V $I_{IH} = \le$ *10 µA*	1, 2, 3	All	2		V
Input voltage low	V_{IL}	$I_{IL} \le$ *10 µA*	1, 2, 3	All		0.8	V
Low level output current 3/	I_{OL1}	V_{CC} = 5.5 V, $V_{OL} \le$ 0.4 V	1, 2, 3	All		8	mA
Low level output current 4/	I_{OL2}					4	
Low level output current 5/	I_{OL3}					4	
Low level output current 6/	I_{OL4}					6	
Low level output current 7/	I_{OL5}					12	
High level output current 3/	I_{OH1}	V_{CC} = 5.5 V, $V_{OH} \le$ 2.7 V	1, 2, 3	All	8		mA
High level output current 4/	I_{OH2}				4		
High level output current 5/	I_{OH3}				4		
High level output current 6/	I_{OH4}				6		
Supply current	I_{CC}	Standby (idle)	1, 2, 3	All		90	mA
		25% duty cycle, 1 MHz				250	
		50% duty cycle, 1 MHz				380	
		100% duty cycle, 1 MHz				675	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input capacitance	C_{IN}	See 4.3.1c	4	All		10	pF
Receiver differential input impedance	Z_{IN}	DC to 1.0 MHz	4, 5, 6	All	10		kΩ
Receiver input threshold voltage	V_{TH}	Direct coupled	4, 5, 6	All	0.6	1.2	V_{PP}
Receiver differential input voltage	V_{IN}	DC to 1.0 MHz	4, 5, 6	All		20	V_{PP}
Receiver common mode rejection ratio	CMRR	DC to 2.0 MHz	4, 5, 6	All	40		dB
Transmitter differential output voltage	V_O	35Ω load	4, 5, 6	All	7.1	9	V_{PP}
		140Ω load			28.3	36	
Waveform distortion	V_{WD}	35Ω load	4, 5, 6	03,04, 05,06, 07,08, 09,10	-0.1	0.1	V_{PEAK}
Output offset voltage	V_{OS}	Direct coupled, measured across the bus.	4, 5, 6	01,02	-90	+90	mV
Output: rise time	t_r	See figure 4	9, 10, 11	01,02	100	300	ns
fall time	t_f				100	300	
Access setup time	TADS	Host read, write and read-modify write, see figure 4. Setup receive message as on figure 4 (receive command).	9, 10, 11	All	0		ns
Access hold time	TADH				200		
Address strobe low to command low	TASLC				0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Data acknowledge low to write high	*TACKWH	Host read, write and read-modify write, see figure 4. Setup receive message as on figure 4 (receive command).	9, 10, 11	All	0		ns
*HWRL, *HWRH high to *HCS high	*TWASH				0		
End of cycle to data acknowledge high	*TACKH				0	30	
End of cycle to data acknowledge low	*TACKL1	no contention			0.3	0.5	µs
	*TACKL2	with contention			0.3	1.2	
	*TACKL3	worst case, one time at start of each message			0.3	2.8	
Data setup time	*TDS				0		ns
Data hold time	*TDH				0		
Data acknowledge low to read high	*TACKRH				0		
*HRD low to data low Z	*TRDLZ				0	20	
*HRD high to data high Z	*TRDHDHZ				0	30	
*HRD high to write low	*TRDHWL				30		
*IRQ to *INTPI output high	*TIRQPOH	Interrupt acknowledge cycle, see figure 4. Setup receive message as on figure 4.	9, 10, 11	All		20	ns
*INPI low to *INTPO low	*TPILPOL					40	
Priority propagation time	*TPR				400	500	
Propagation time	*TPRE				0		
*INTACK low to *IRQ high	*TINAIRQH				0	200	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
*INTACK high to next *IRQ low	*TINAIRQL	Interrupt acknowledge cycle, see figure 4. Setup receive message on figure 4	9, 10, 11	All	0	200	ns
*INTACK high to *INTPO low	*TINAPOL				30	40	
*HRD low to *DTACK low	*TRINAH				0		
*HRD low to *DTACK low	*ITACK				300	400	
*DTACK low to *HRD high	*TACKRH				0		
*HRD low to data in low Z	*TRDLZ				0	20	
*HRD low to data in high Z	*TRSHDHZ				0	30	
End of cycle to *DTACK high	*TACKH				0	30	
Transmitter output rise and fall time	*tr, tf				100	300	
Vadid address to I/O write low	*TVAWL	I/O write and command write, see figure 4. Setup receive message as on figure 4.	9, 10, 11	All	50		ns
Address valid to I/O write high	*TWHVA				50		
I/O *WR pulse width	*TIOWW				90	110	
Data setup time	*TDS				25	50	
Data hold time	*TDH				40	80	
Command write pulse width	*TCMWW				290	310	
Command strobe to I/O write low	*TCMHWL				40		
Write high to CMDS low	*TWHCML				100		

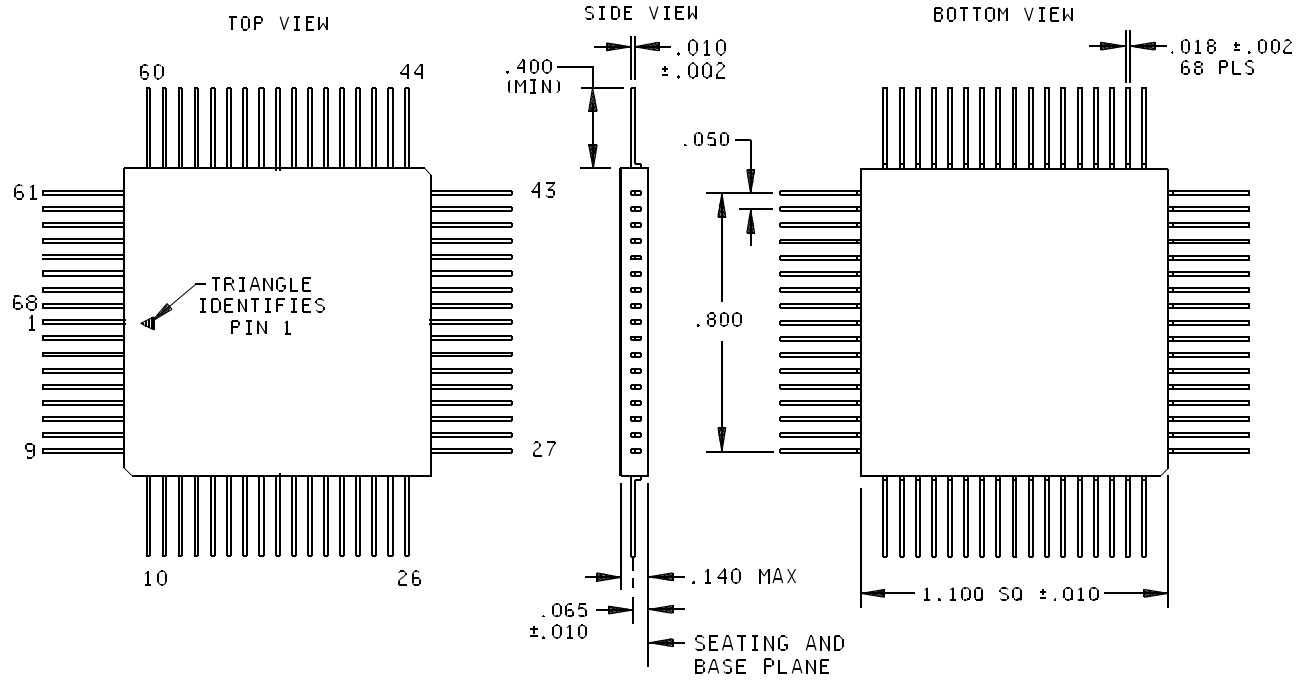
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Valid address to read low	*TVARL	I/O read and terminal address read, see figure 4. Setup receive message as on figure 4.	9, 10, 11	All	50		ns
Adress valid after read high	*TRHVA				50		
I/O *RD pulse width	*TOIORW				190	210	
I/O *RD high to data high Z	*TRHDHZ				0	200	
I/O *RD high to CMDS low	*TRHCML				100		
I/O data bus high Z to data on bus	*TIODHZRL				100		
I/O data bus high Z to data on bus	*TIODHZDL				100		
I/O *RD low to data stable	*TRLDS					80	
I/O *RD high to data bus in low Z	*RHIODLZ				50		
Output impedence	*R_{OUT}	When transmitting	4, 5, 6	04,08, 10		10	Ω
Rise time	*t_r	10% to 90%	9, 10, 11	04,08, 10	220	300	ns
Fall time	*t_f	90% to 10%	9, 10, 11	04,08, 10	220	300	ns
Output harmonic content (referenced to the average peak value at 1.0 MHz)		at 1.5 MHz	4, 5, 6	04,08, 10	-3		dB
		at 2.5 MHz			-13.5		
		at 4.0 MHz			-25.5		

1/ Device types 01 and 02, V_{CC} = +4.75 V dc to +5.50 V dc, unless otherwise specified.
Device types 03, 04, 05, 06, 07, 08, 09, and 10, V_{CC} = +4.50 V dc to +5.50 V dc, unless otherwise specified.
2/ All group A subgroup testing of the same temperature may be performed concurrently.
3/ Measured at pin functions: H_DAT0 through H_DAT15.
4/ Measured at pin functions: I/O_DAT0 through I/O_DAT7, I/O_ADR1, I/O_ADR2.
5/ Measured at pin functions: DSC_INTPO_L.
6/ Measured at pin functions: PLSCMD, I/O_RD, I/O_WR, CMDS, MDCDRST.
7/ Measured at pin functions: IRQ_L, DTACK_L.

Case outline U.
(Device types 03, 04, 07, 08, 09, and 10)

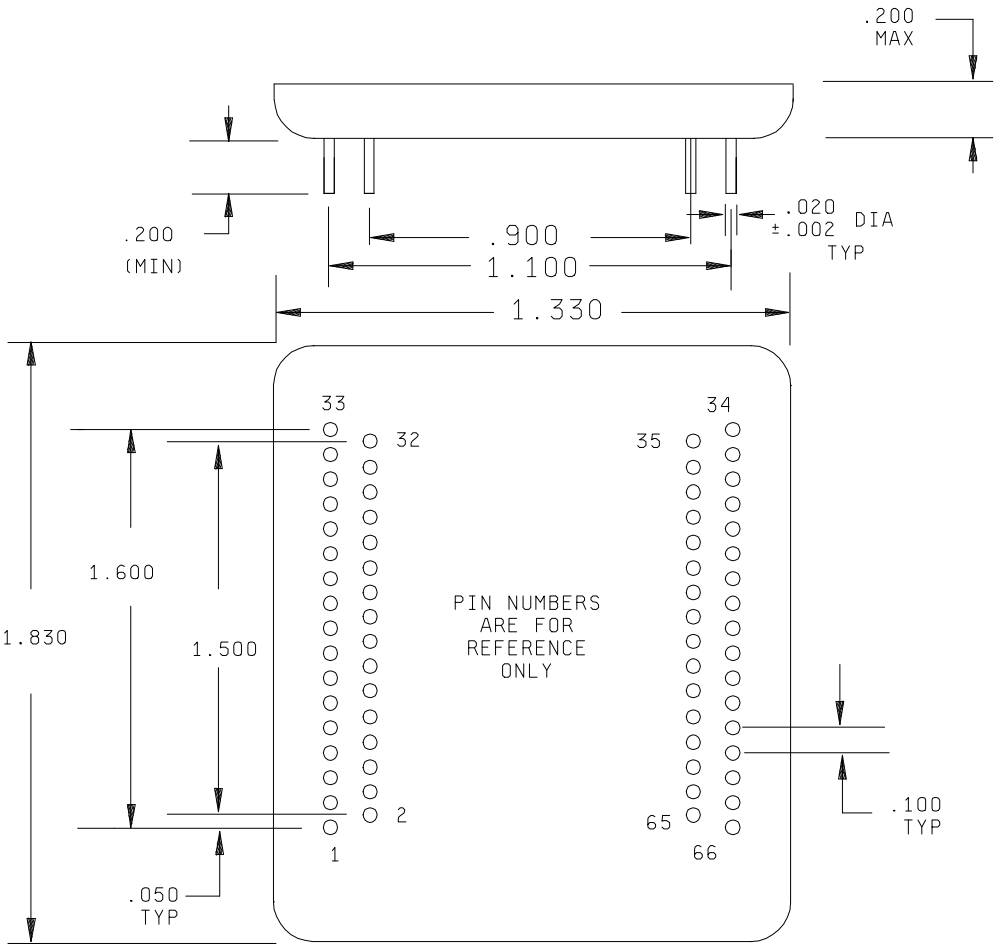


Inches	mm	Inches	mm	Inches	mm
.005	0.13	.020	0.51	.075	1.91
.008	0.20	.040	1.02	.120	3.05
.010	0.25	.043	1.09	.250	6.35
.012	0.30	.050	1.27	.290	7.37
.015	0.38	.060	1.52	.800	20.32
		.074	1.88	.950	24.13

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.25 mm) for two place decimals.

FIGURE 1. Case outline(s).

Case outline X.
(Device types 01, 02, 05, and 06)

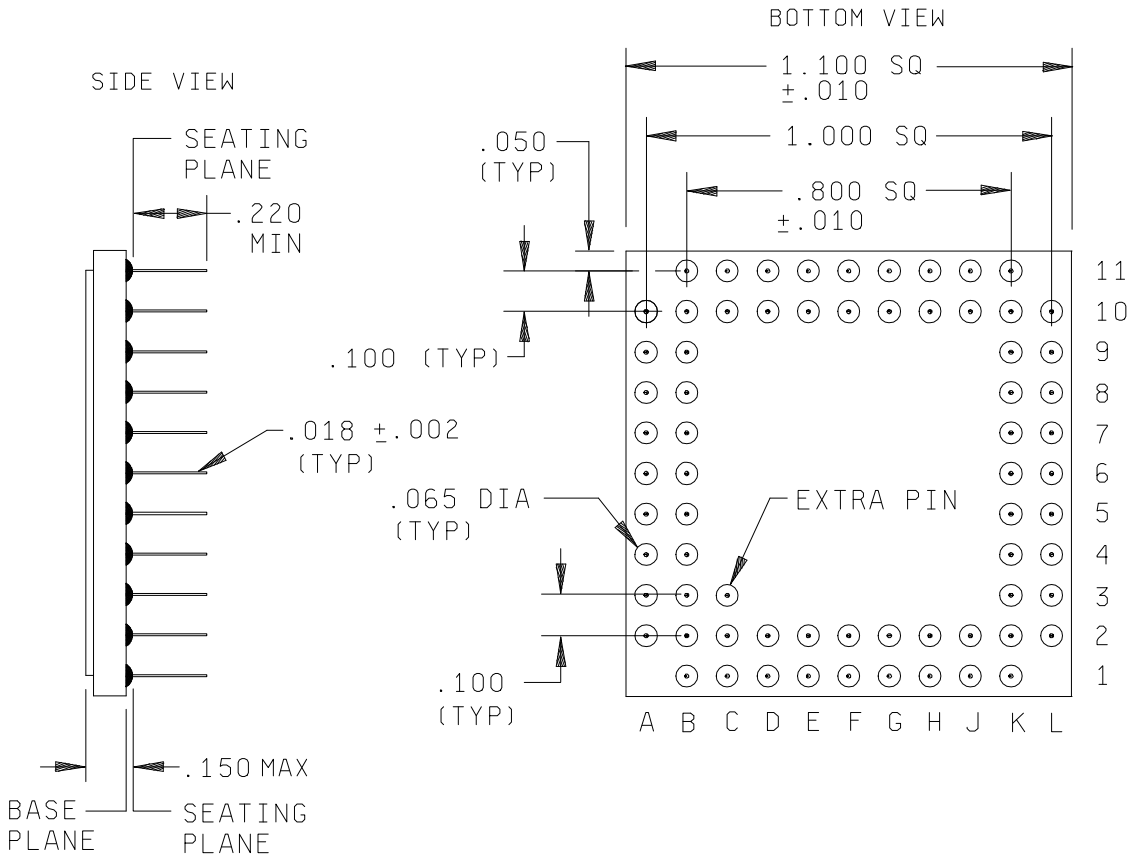


Inches	mm
.020	0.50
.050	1.27
.100	2.54
.200	5.08
.900	22.88
1.100	27.94
1.330	33.78
1.500	38.10
1.800	40.64
1.830	46.48

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.25 mm) for two place decimals.

FIGURE 1. Case outline(s) - Continued.

Case outline Z.
(Device types 03, 04, 07, 08, 09, and 10)



Inches	mm	Inches	mm
.002	0.05	.080	2.03
.005	0.13	.100	2.54
.010	0.25	.120	3.05
.012	0.30	.800	20.32
.018	0.46	1.000	25.40
.050	1.27	1.100	27.94

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm) for three place decimals and ±.01 (0.3 mm) for two place decimals.

FIGURE 1. Case outline(s) - Continued.

Device types	03, 04, 07, 08, 09, and 10			Device types	03, 04, 07, 08, 09, and 10		
Case outline	U			Case outline	U		
Terminal number	Terminal symbol		Type	Terminal number	Terminal symbol		Type
1	I/O_DAT1		I/O	21	CMDS		O
2	I/O_DAT2		I/O	22	TXINH_B		I
3	I/O_DAT3		I/O	23	BUS_B		I/O
4	I/O_DAT4		I/O	24	$\overline{\text{BUS\_B}}$		I/O
5	I/O_DAT5		I/O	25	NC		---
6	I/O_DAT6		I/O	26	$\overline{\text{I/O\_RD}}$		O
7	I/O_DAT7		I/O	27	$\overline{\text{I/O\_WR}}$		O
8	$\overline{\text{HCS}}$		I	28	MDCDRST		O
9	SSF_TF		I	29	PLSCMD		O
10	$\overline{\text{RST}}$		I	30	$\overline{\text{IRQ}}$		O
11	CLK10		I	31	$\overline{\text{DTACK}}$		O
12	I/O_ADR1		O	32	H_DAT12		I/O
13 (see note)	I/O_ADR2		O	33	H_ADR2		I
14	$\overline{\text{INTPO\_DSC}}$		O	34	H_ADR3		I
15	$\overline{\text{INTPI}}$		I	35	H_ADR4		I
16	$\overline{\text{INTACK}}$		I	36	H_ADR5		I
17	TXINH_A		I	37	H_ADR6		I
18	BUS_A		I/O	38	H_ADR7		I
19	$\overline{\text{BUS\_A}}$		I/O	39	+5 V		I
20	NC		---	40	+5 V		I

NOTE: Terminal 13 for device types 09 and 10 is terminal symbol TAGCLK_IN and type I.

FIGURE 2. Terminal connections.

Device types	03, 04, 07, 08, 09, and 10			Device types	03, 04, 07, 08, 09, and 10		
Case outline	U			Case outline	U		
Terminal number	Terminal symbol		Type	Terminal number	Terminal symbol		Type
41	GND		---	55	H_DAT6		I/O
42	GND		---	56	H_DAT7		I/O
43	GND		---	57	H_DAT8		I/O
44	H_ADR8		I	58	H_DAT9		I/O
45	H_ADR9		I	59	H_DAT10		I/O
46	H_ADR10		I	60	H_DAT11		I/O
47	H_ADR11		I	61	H_ADR1		I
48	H_ADR12		I	62	$\overline{\text{HRD}}$		I
49	H_DAT0		I/O	63	$\overline{\text{HWRL}}$		I
50	H_DAT1		I/O	64	$\overline{\text{HWRH}}$		I
51	H_DAT2		I/O	65	H_DAT13		I/O
52	H_DAT3		I/O	66	H_DAT14		I/O
53	H_DAT4		I/O	67	H_DAT15		I/O
54	H_DAT5		I/O	68	I/O_DAT0		I/O

FIGURE 2. Terminal connections - Continued.

Device types	01, 02, 05, and 06			Device types	01, 02, 05, and 06		
Case outlines	X and Y			Case outlines	X and Y		
Terminal number	Terminal symbol		Type	Terminal number	Terminal symbol		Type
1	TXINH_A		I	21	H_DAT6		I/O
2	+5 V		I	22	H_DAT7		I/O
3	H_ADR1		I	23	H_DAT8		I/O
4	H_ADR2		I	24	H_DAT9		I/O
5	H_ADR3		I	25	H_DAT10		I/O
6	H_ADR4		I	26	H_DAT11		I/O
7	H_ADR5		I	27	H_DAT12		I/O
8	H_ADR6		I	28	H_DAT13		I/O
9	H_ADR7		I	29	H_DAT14		I/O
10	H_ADR8		I	30	H_DAT15		I/O
11	H_ADR9		I	31	$\overline{\text{HWRH}}$		I
12	H_ADR10		I	32	+5 V		I
13	H_ADR11		I	33	TXINH_B		I
14	H_ADR12		I	34	BUS_B		I/O
15	H_DAT0		I/O	35	$\overline{\text{BUS\_B}}$		I/O
16	H_DAT1		I/O	36	GND		---
17	H_DAT2		I/O	37	I/O_DAT0		I/O
18	H_DAT3		I/O	38	I/O_DAT1		I/O
19	H_DAT4		I/O	39	I/O_DAT2		I/O
20	H_DAT5		I/O	40	I/O_DAT3		I/O

FIGURE 2. Terminal connections - Continued.

Device types	01, 02, 05, and 06			Device types	01, 02, 05, and 06		
Case outlines	X and Y			Case outlines	X and Y		
Terminal number	Terminal symbol		Type	Terminal number	Terminal symbol		Type
41	I/O_DAT4		I/O	54	$\overline{\text{INTPI}}$		I
42	I/O_DAT5		I/O	55	$\overline{\text{INTACK}}$		I
43	I/O_DAT6		I/O	56	CMDS		O
44	I/O_DAT7		I/O	57	PLSCMD		O
45	$\overline{\text{HCS}}$		I	58	$\overline{\text{HWRL}}$		I
46	See note		I	59	$\overline{\text{HRD}}$		I
47	$\overline{\text{RST}}$		I	60	$\overline{\text{I/O\_RD}}$		O
48	CLK10		I	61	$\overline{\text{I/O\_WR}}$		O
49	I/O_ADR1		O	62	$\overline{\text{IRQ}}$		O
50	I/O_ADR2		O	63	$\overline{\text{DTACK}}$		O
51	+5 V		I	64	GND		---
52	$\overline{\text{INTPO\_DSC}}$		O	65	$\overline{\text{BUS\_A}}$		I/O
53	MDCDRST		O	66	BUS_A		I/O

NOTE: Terminal 46, the terminal symbol is +5 V RAM supply for device types 01 and 05, SSF_TF for device types 02 and 06.

FIGURE 2. Terminal connections - Continued.

Device types	03, 04, 07,08, 09, and 10			Device types	03, 04, 07, 08, 09, and 10		
Case outline	Z			Case outline	Z		
Terminal number	Terminal symbol		Type	Terminal number	Terminal symbol		Type
L10	I/O_DAT1		I/O	L3	CMDS		O
H10	I/O_DAT2		I/O	K4	TXINH_B		I
J10	I/O_DAT3		I/O	K1	GND		---
K10	I/O_DAT4		I/O	H1	$\overline{\text{BUS\_B}}$		I/O
K9	I/O_DAT5		I/O	J1	GND		---
L9	I/O_DAT6		I/O	L4	$\overline{\text{I/O\_RD}}$		O
L8	I/O_DAT7		I/O	H2	$\overline{\text{I/O\_WR}}$		O
G11	$\overline{\text{HCS}}$		I	K2	MDCDRST		O
H11	SSF_TF		I	F2	PLSCMD		O
G10	$\overline{\text{RST}}$		I	F1	$\overline{\text{IRQ}}$		O
J11	CLK10		I	E1	$\overline{\text{DTACK}}$		O
K8	I/O_ADR1		O	G1	H_DAT12		I/O
L7 (see note)	I/O_ADR2		O	E2	H_ADR2		I
K7	$\overline{\text{INTPO\_DSC}}$		O	D1	H_ADR3		I
L6	$\overline{\text{INTPI}}$		I	C3	NC		---
K6	$\overline{\text{INTACK}}$		I	D2	H_ADR4		I
J2	BUS_B		I/O	C1	H_ADR5		I
K3	NC		---	B1	H_ADR6		I
L2	NC		---	A2	H_ADR7		I
G2	TXINH_A		I	L5	+5 V		I
				K5	+5 V		I

NOTE: Terminal L7, for device types 09 and 10 is terminal symbol TAGCLK_IN and type I.

FIGURE 2. Terminal connections - Continued.

Device types	03, 04, 07, and 08			Device types	03, 04, 07, and 08		
Case outline	Z			Case outline	Z		
Terminal number	Terminal symbol		Type	Terminal number	Terminal symbol		Type
B2	GND		---	A10	H_DAT6		I/O
B3	BUS_A		I/O	B8	H_DAT7		I/O
C2	$\overline{\text{BUS\_A}}$		I/O	B9	H_DAT8		I/O
A3	H_ADR8		I	B10	H_DAT9		I/O
B4	H_ADR9		I	B11	H_DAT10		I/O
A4	H_ADR10		I	C11	H_DAT11		I/O
B5	H_ADR11		I	C10	H_ADR1		I
A5	H_ADR12		I	D11	$\overline{\text{HRD}}$		I
B6	H_DAT0		I/O	E11	$\overline{\text{HWRL}}$		I
A6	H_DAT1		I/O	F11	$\overline{\text{HWRH}}$		I
A7	H_DAT2		I/O	D10	H_DAT13		I/O
B7	H_DAT3		I/O	E10	H_DAT14		I/O
A8	H_DAT4		I/O	F10	H_DAT15		I/O
A9	H_DAT5		I/O	K11	I/O_DAT0		I/O

FIGURE 2. Terminal connections - Continued.

Device types 01 and 05.

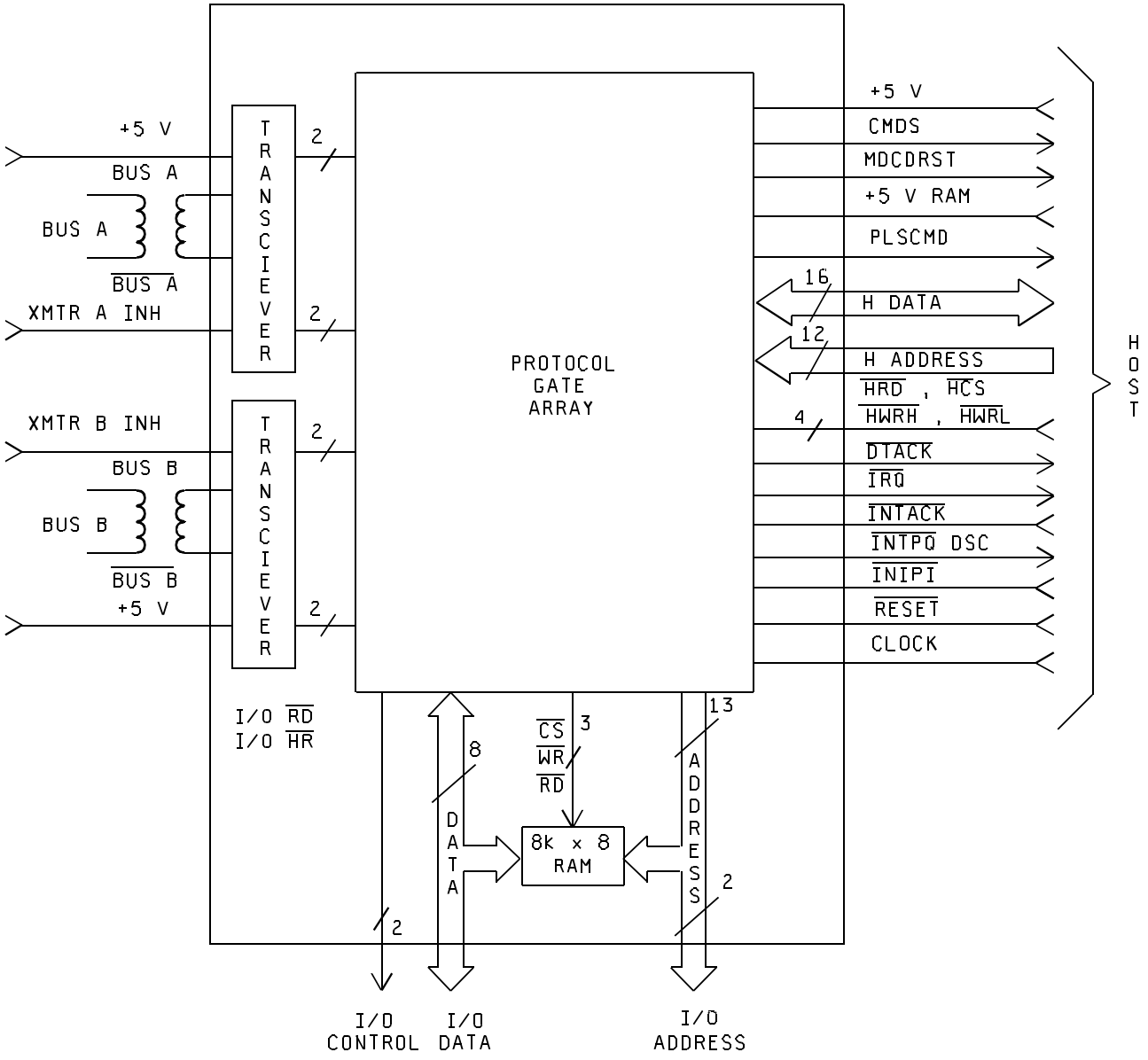


FIGURE 3. Block diagram.

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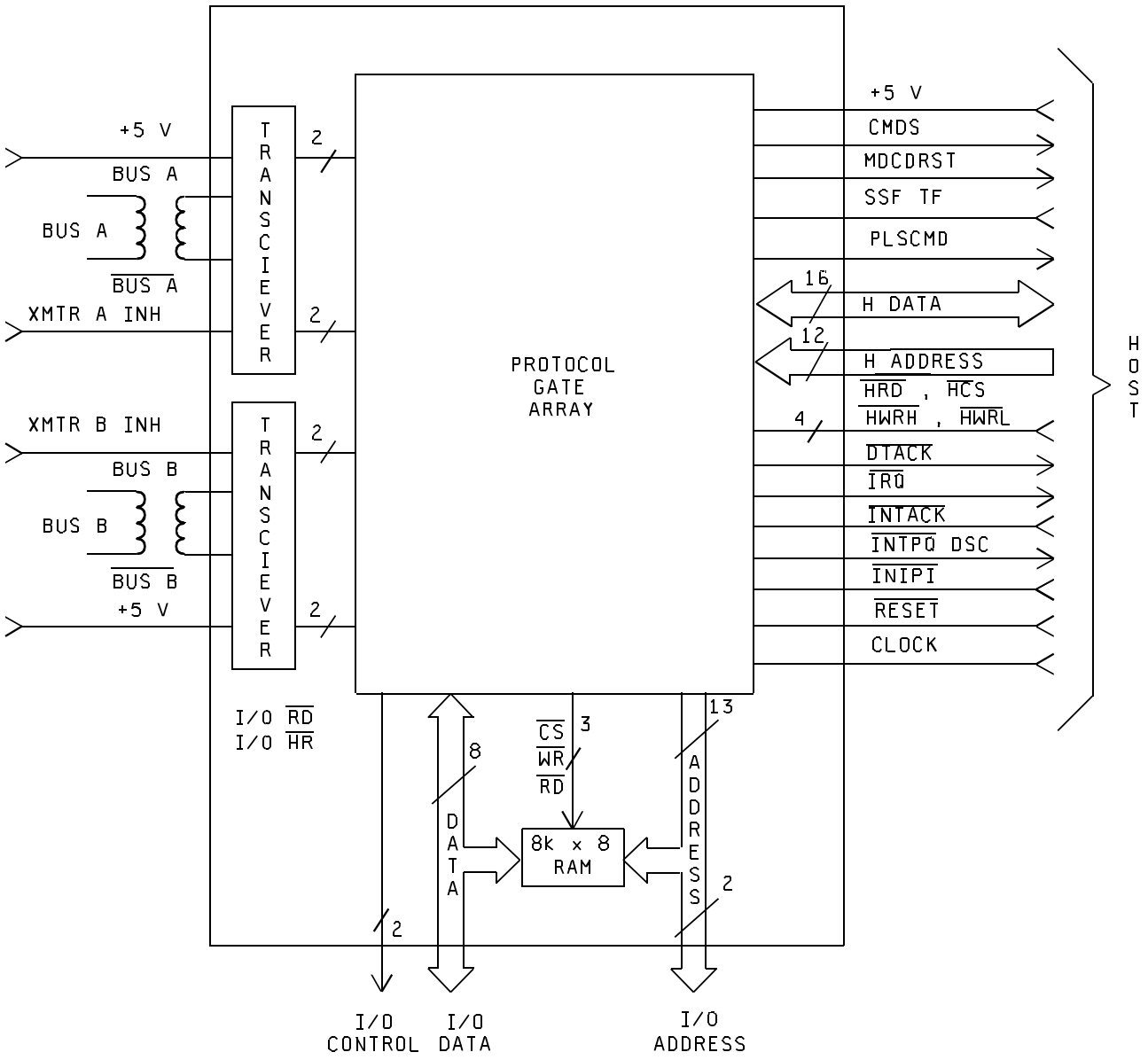
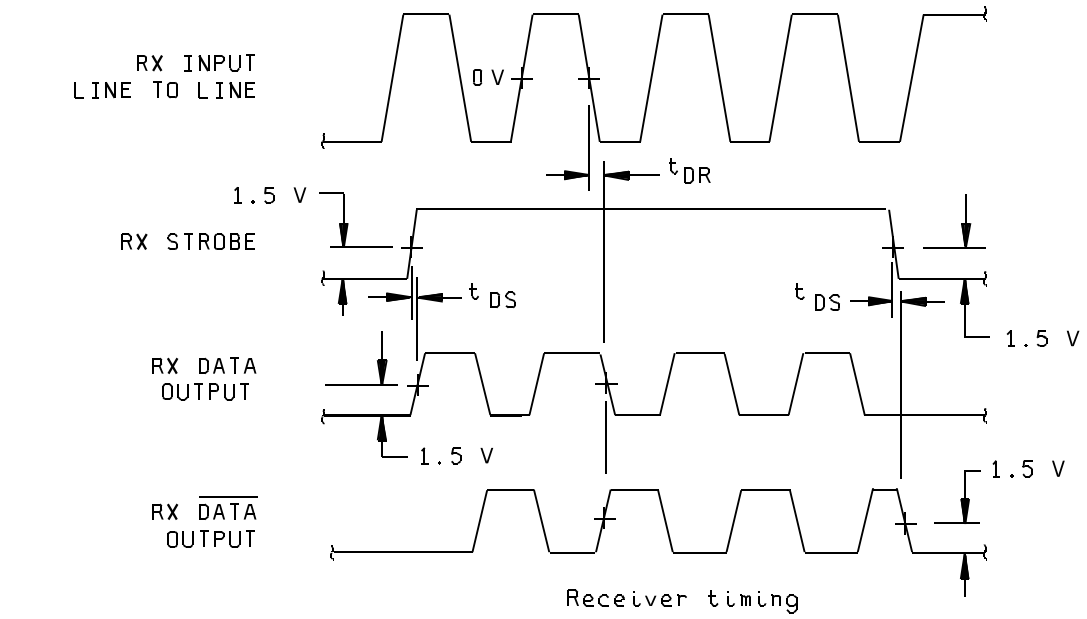
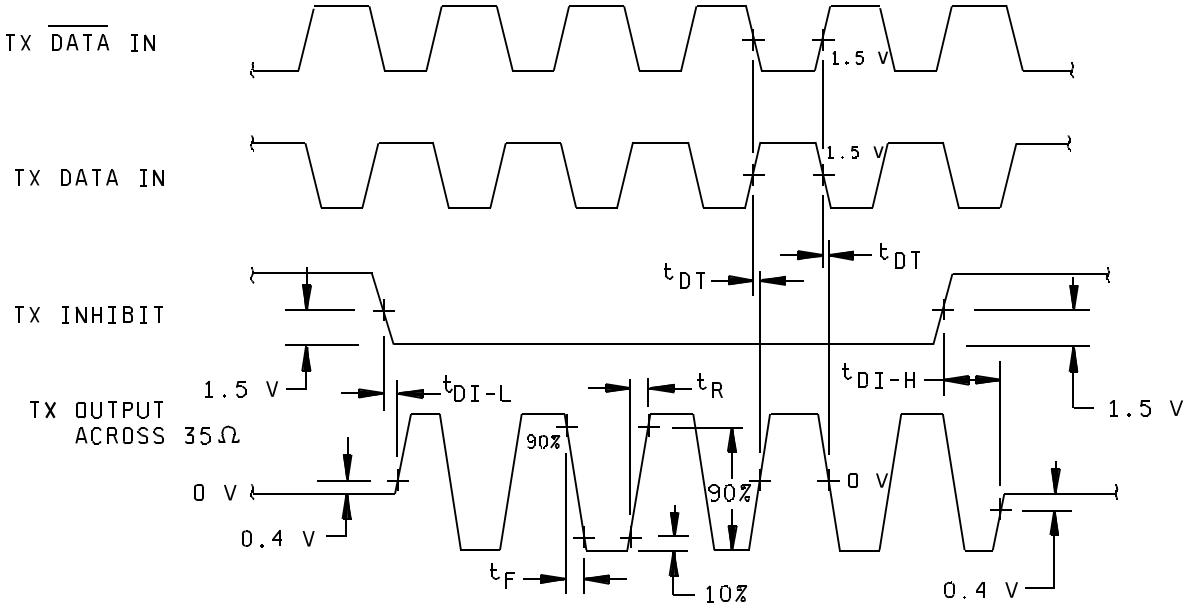


FIGURE 3. Block diagram - Continued.

Device types 01, 02, 03, 05, 06, 07, and 09.



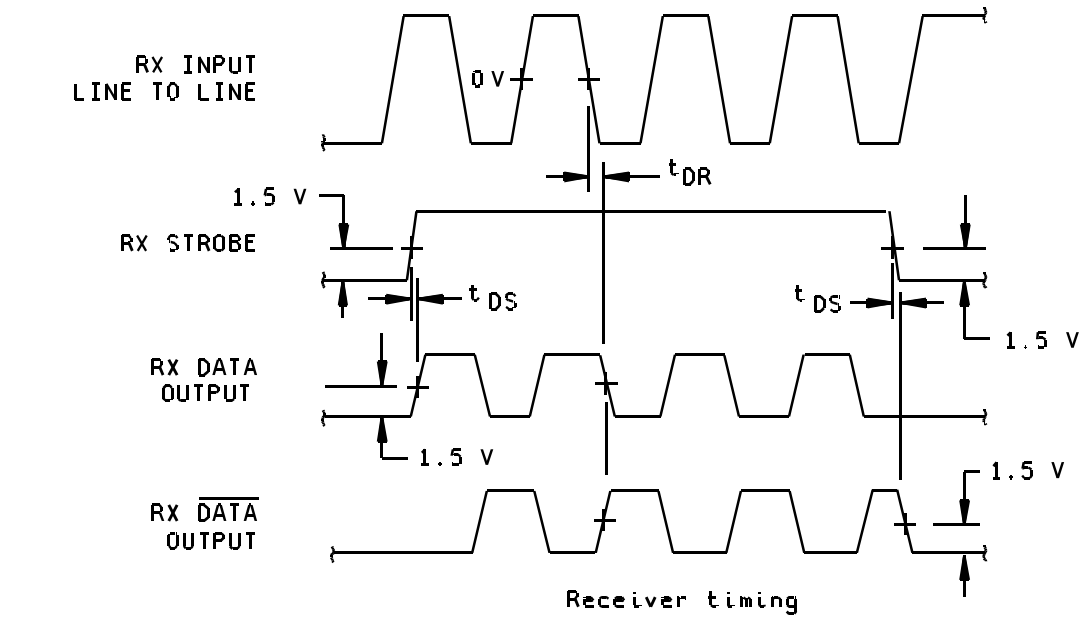
Receiver timing



Transmitter timing

FIGURE 4. Timing waveforms.

Device types 04, 08, and 10.



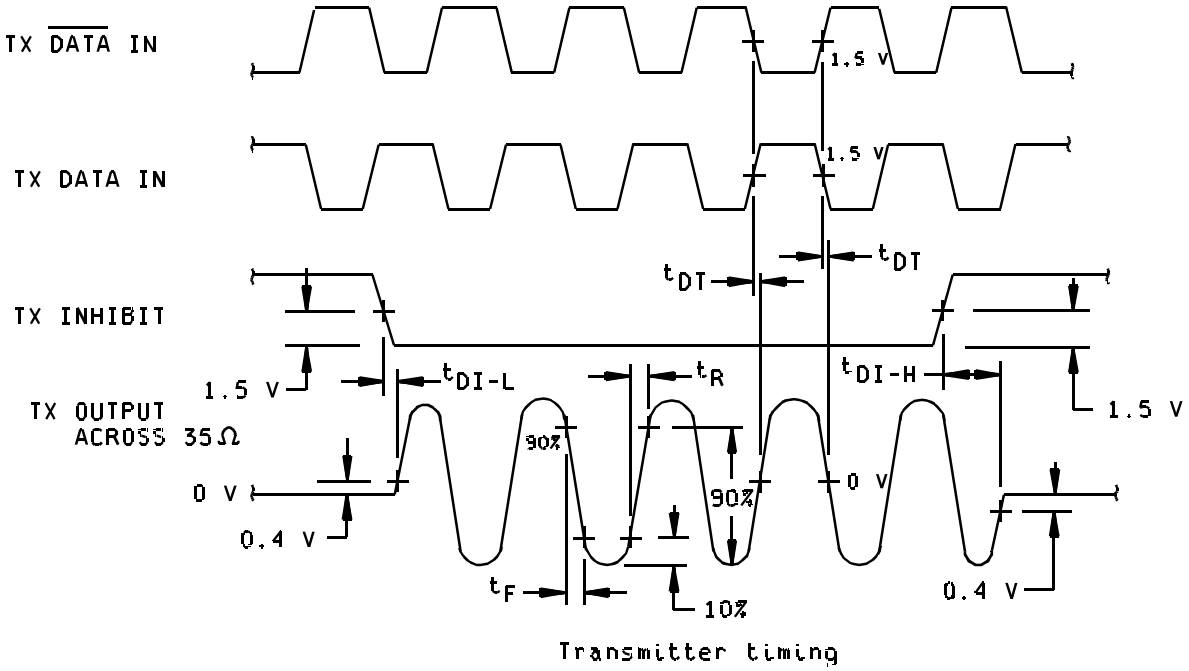


FIGURE 4. Timing waveforms - Continued.

Host write cycle

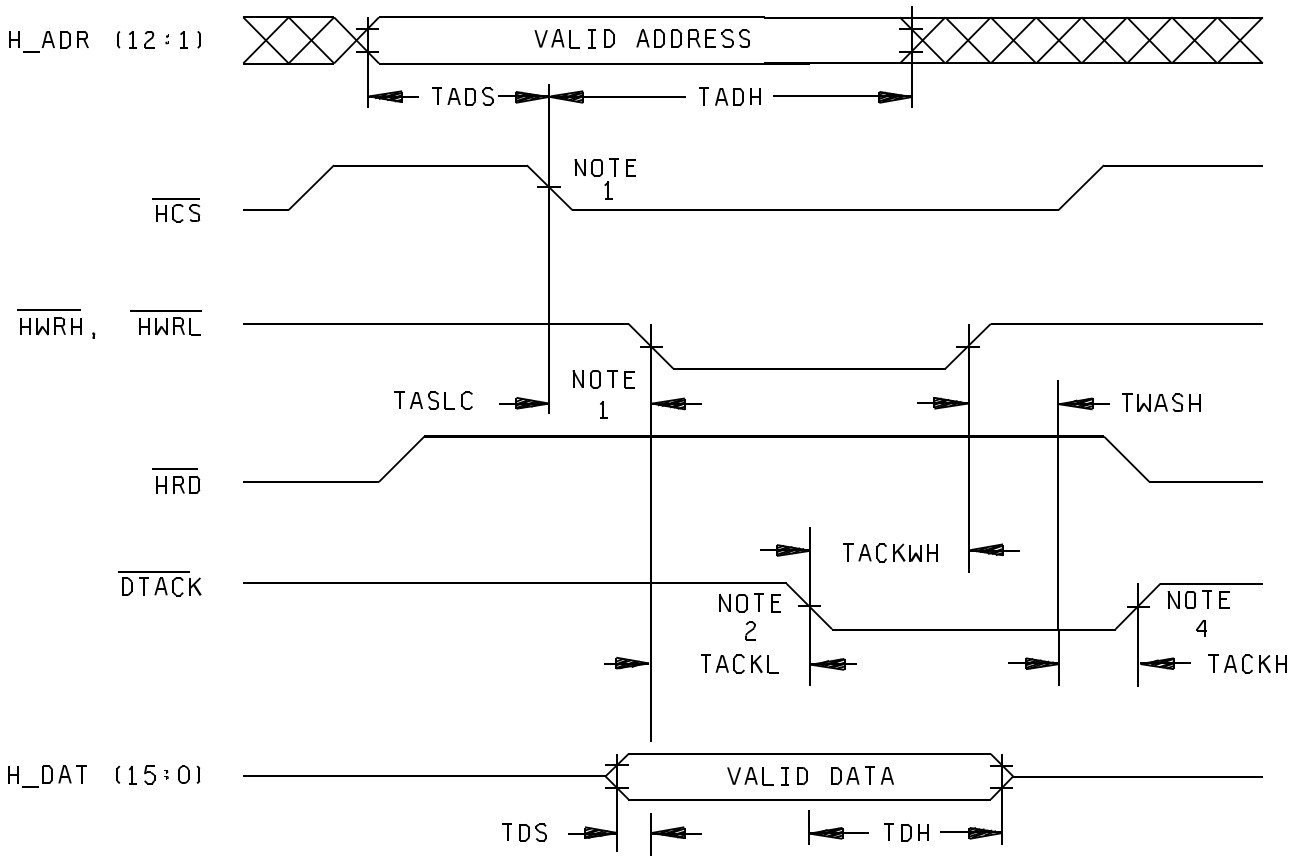


FIGURE 4. Timing waveforms - Continued.

Host read cycle

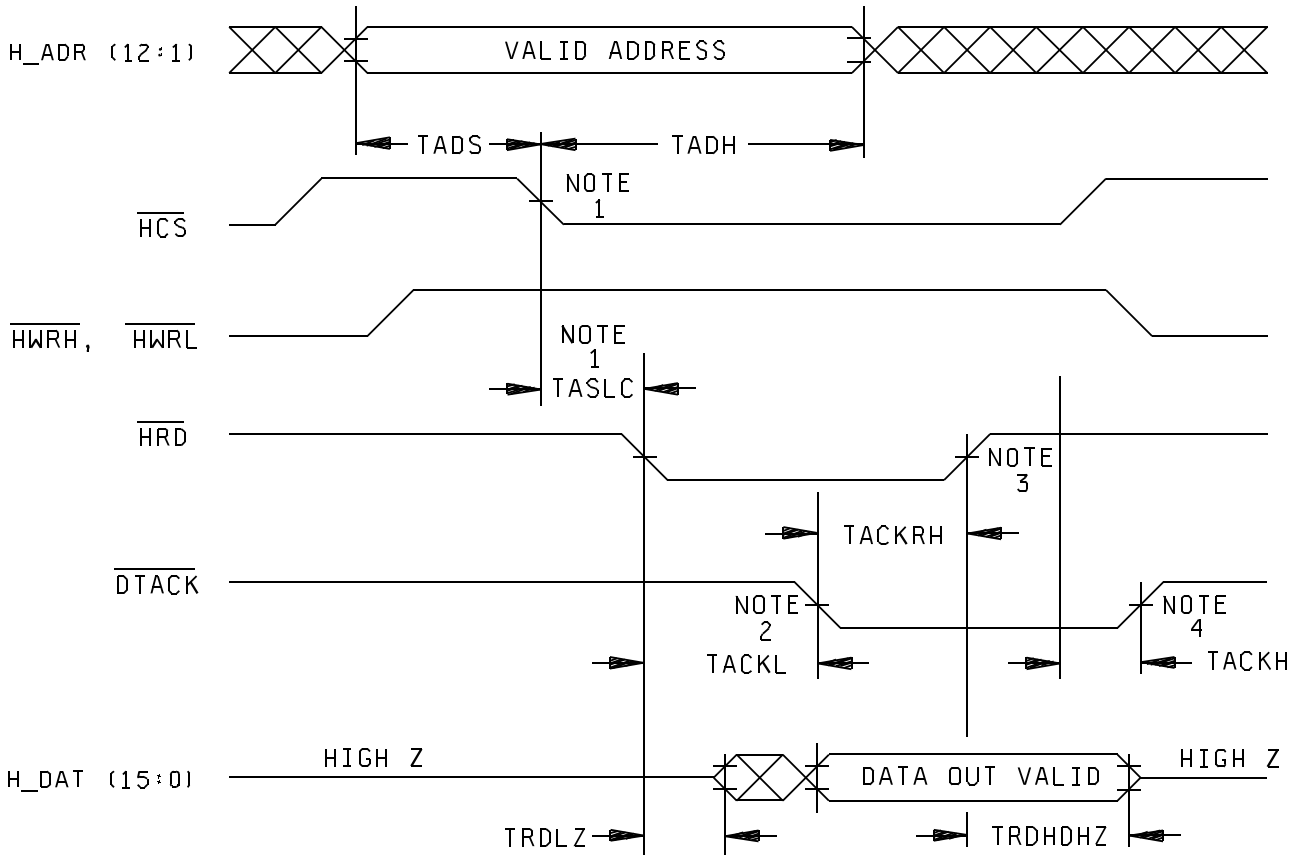


FIGURE 4. Timing diagrams - Continued.

Host read-modify-write cycle

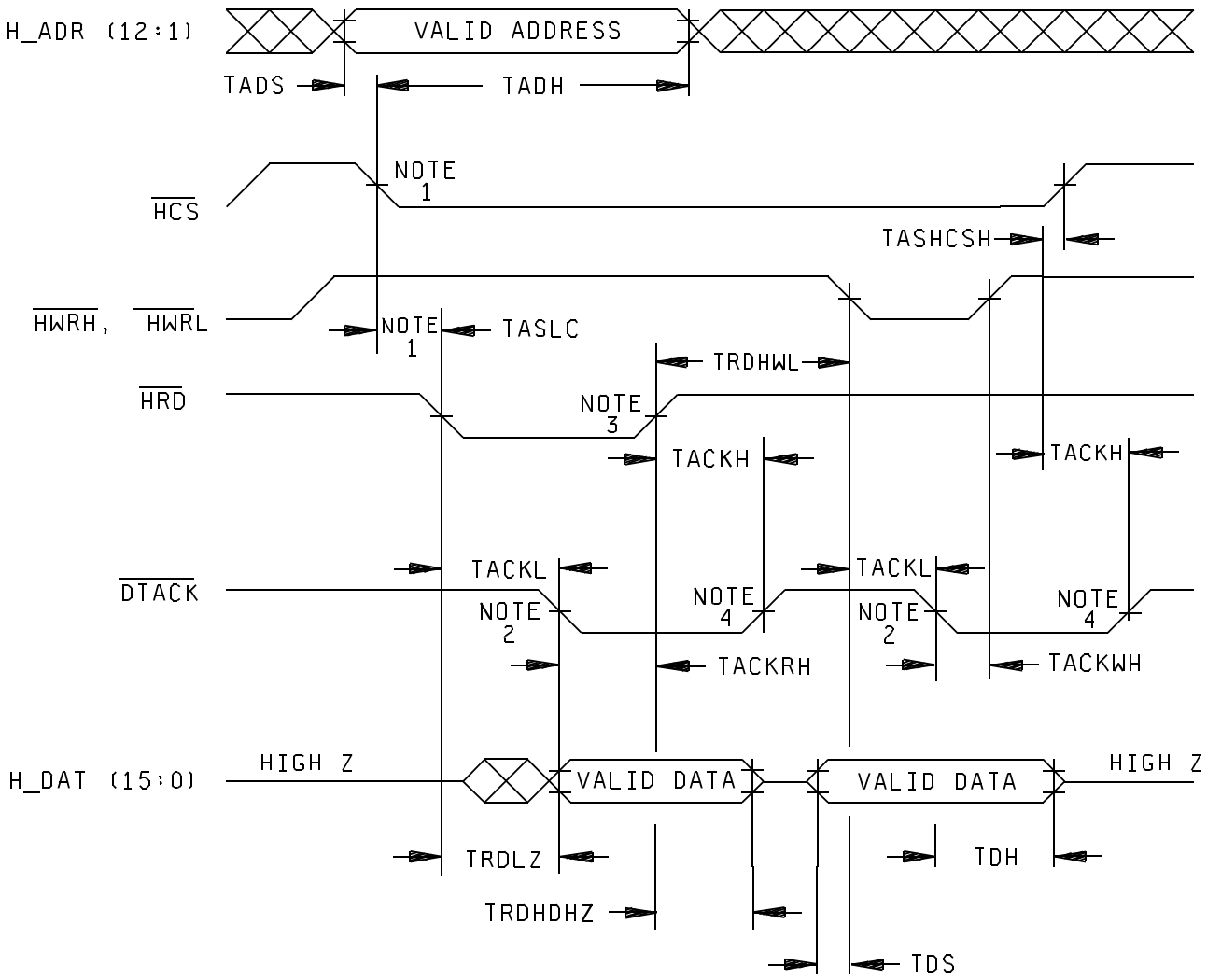


FIGURE 4. Timing diagrams - Continued.

Interrupt acknowledge cycle

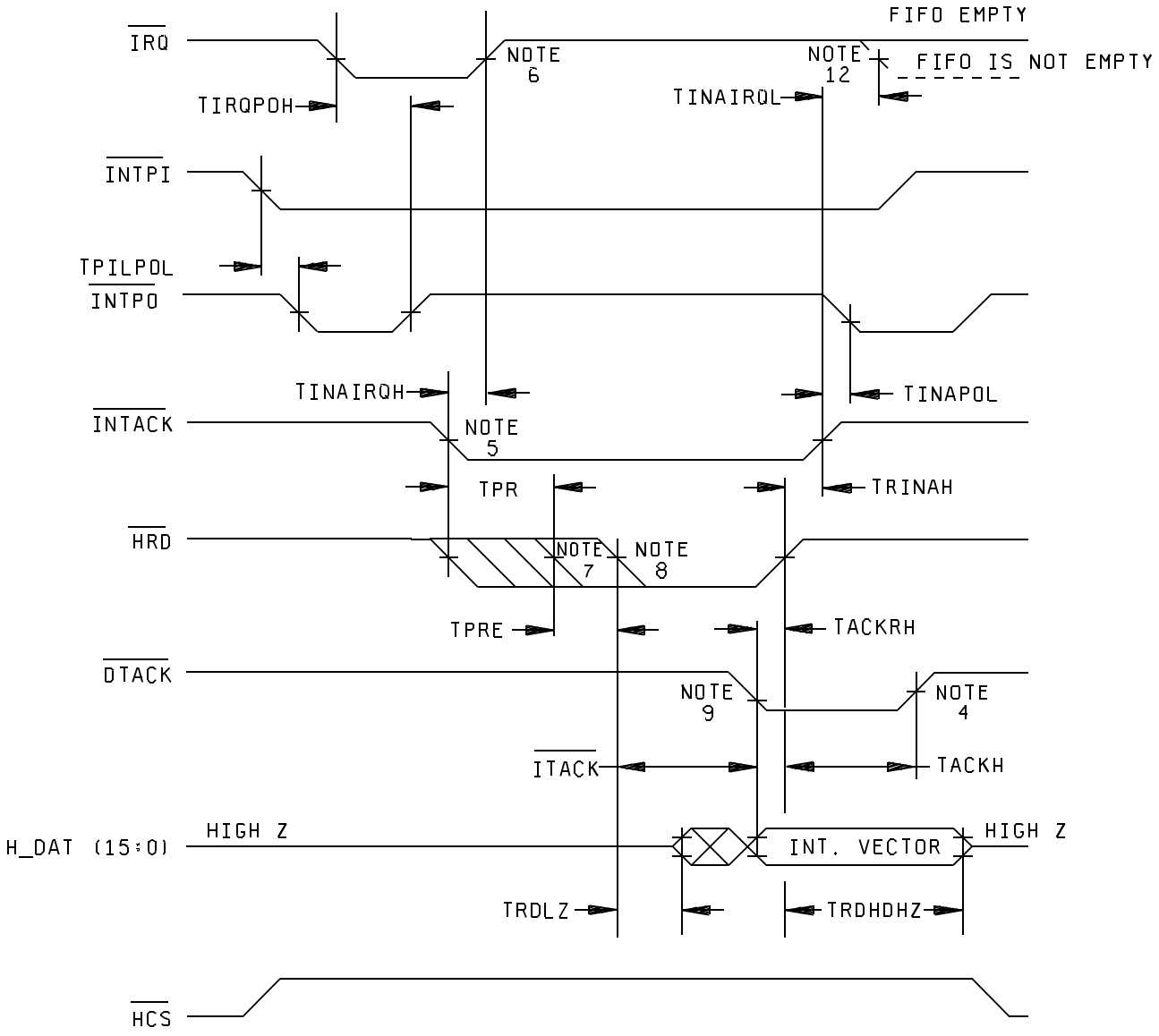


FIGURE 4. Timing diagrams - Continued.

I\O write cycle

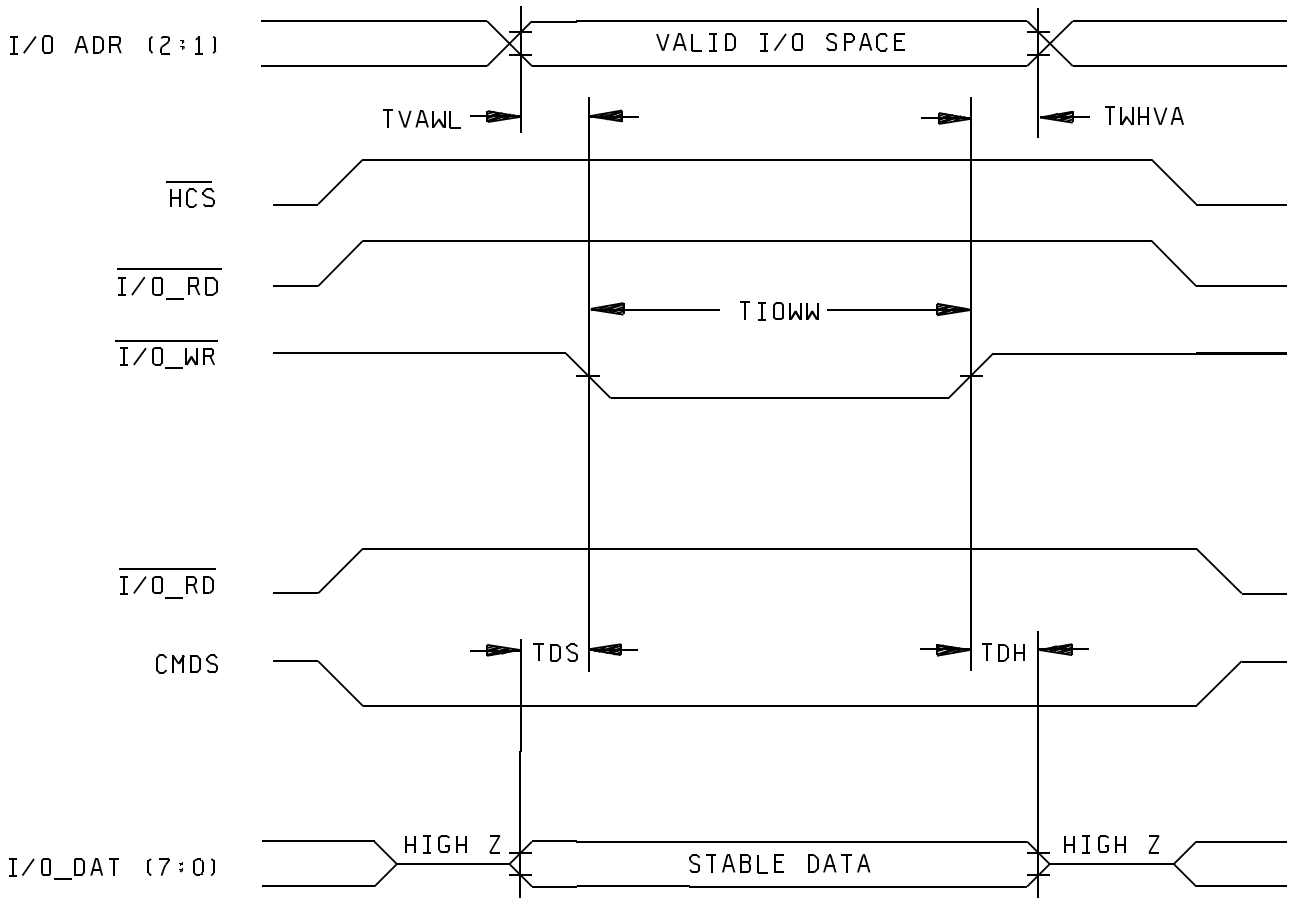


FIGURE 4. Timing waveforms - Continued.

Command write cycle

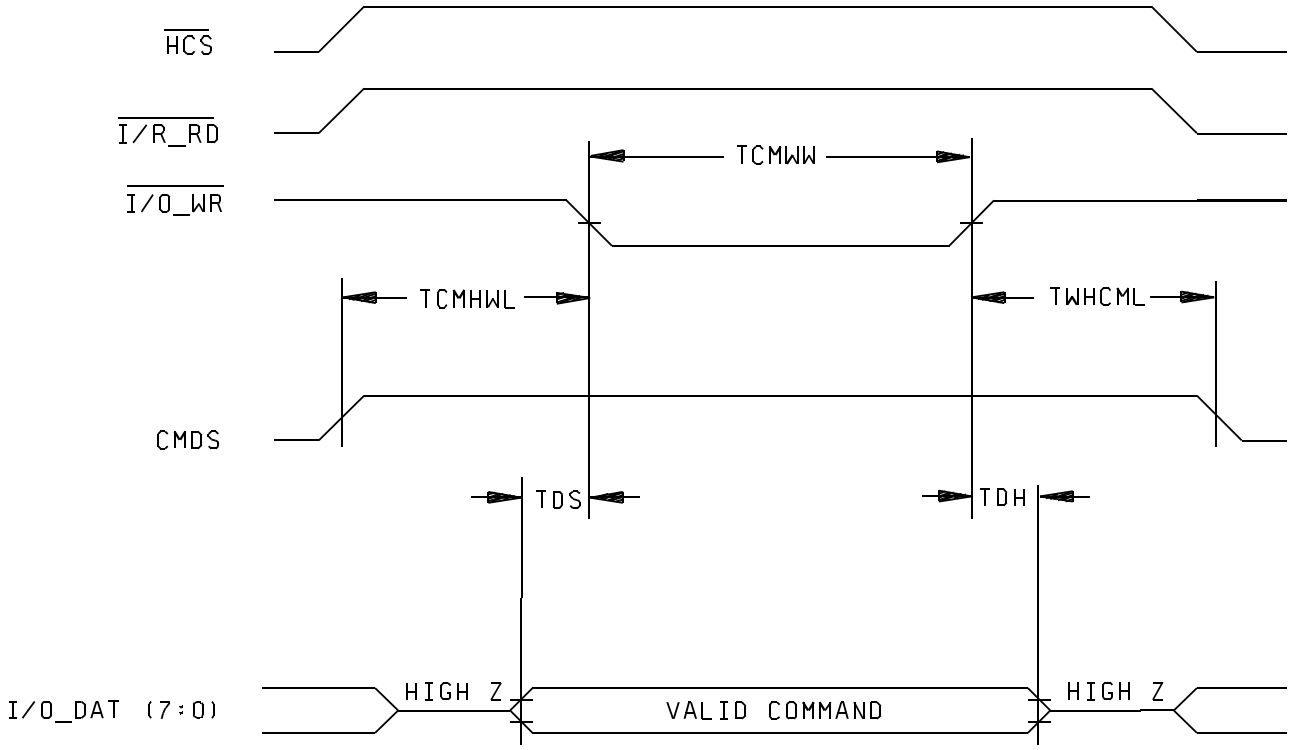


FIGURE 4. Timing diagrams - Continued.

I\O read cycle

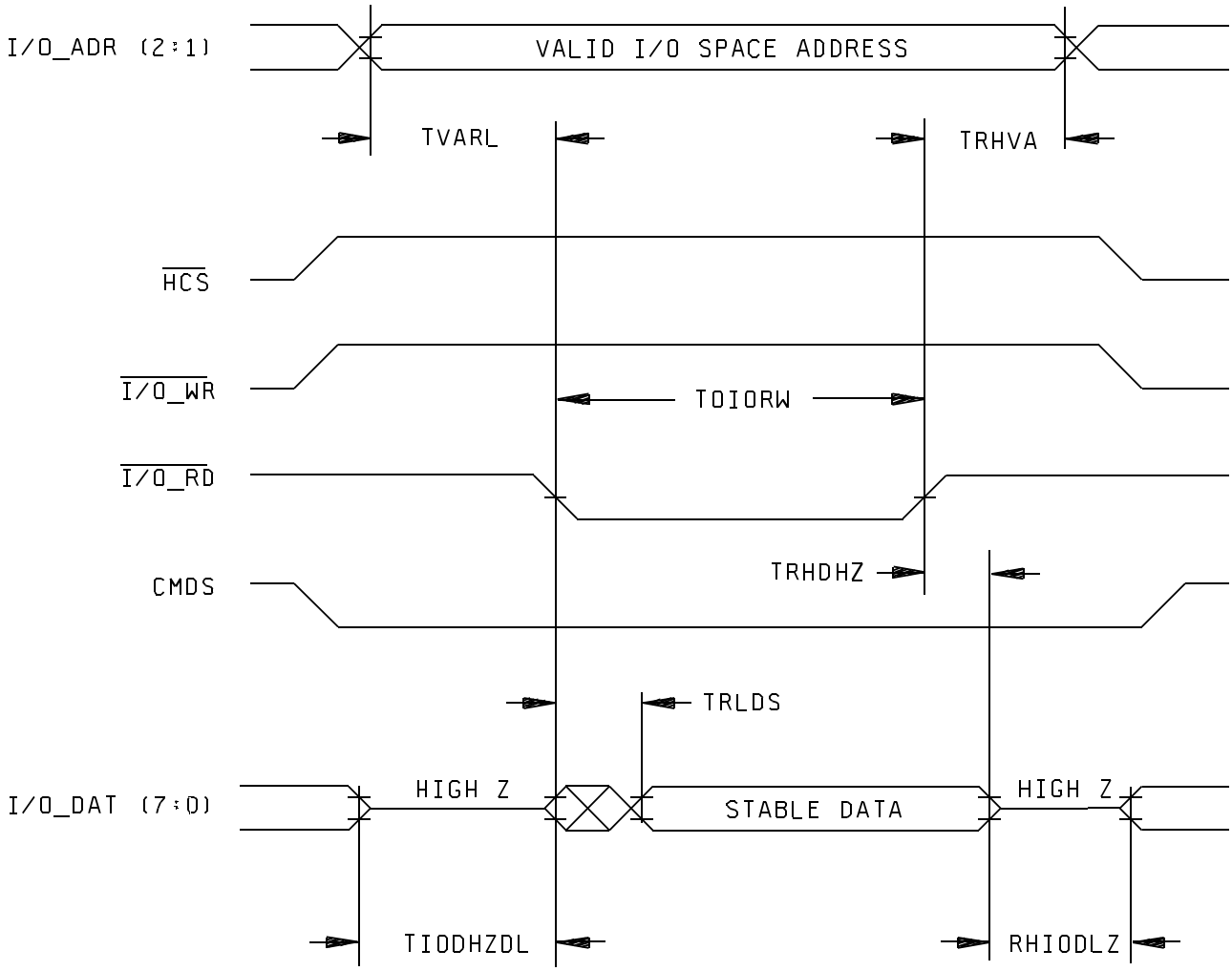


FIGURE 4. Timing diagrams - Continued.

Terminal address read cycle

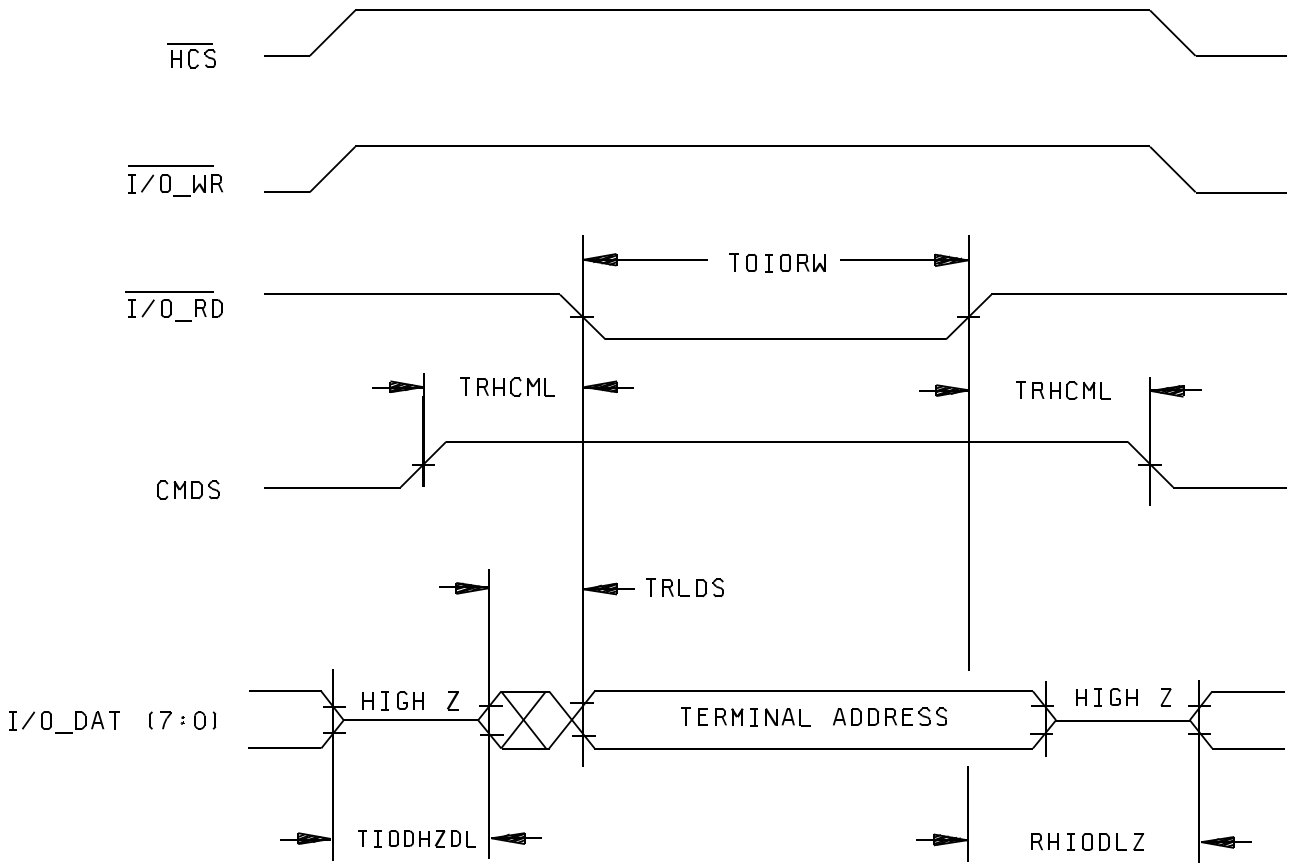


FIGURE 4. Timing diagrams - Continued.

Receive command

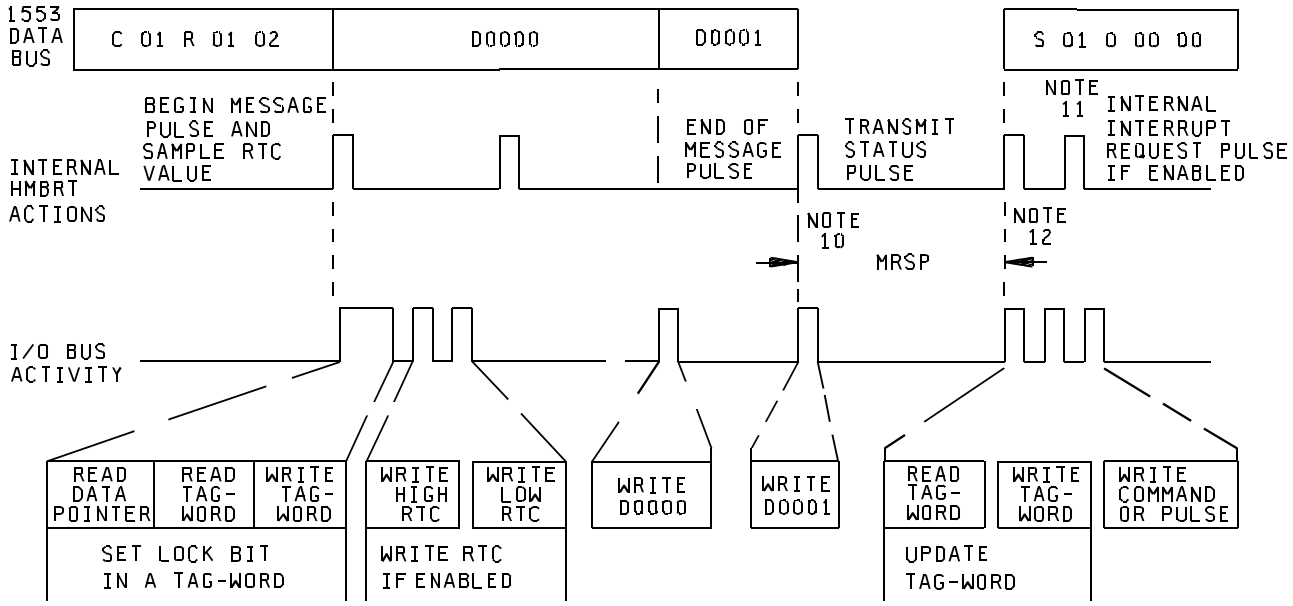


FIGURE 4. Timing diagrams - Continued.

Transmit command

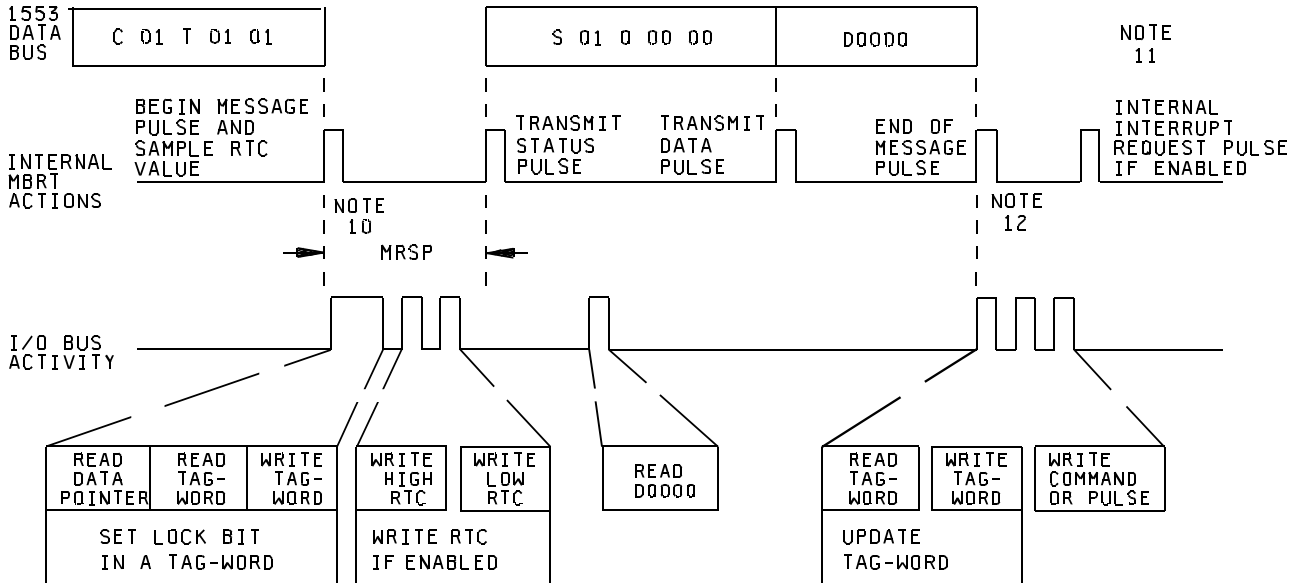


FIGURE 4. Timing diagrams - Continued.

Remote terminal reset command

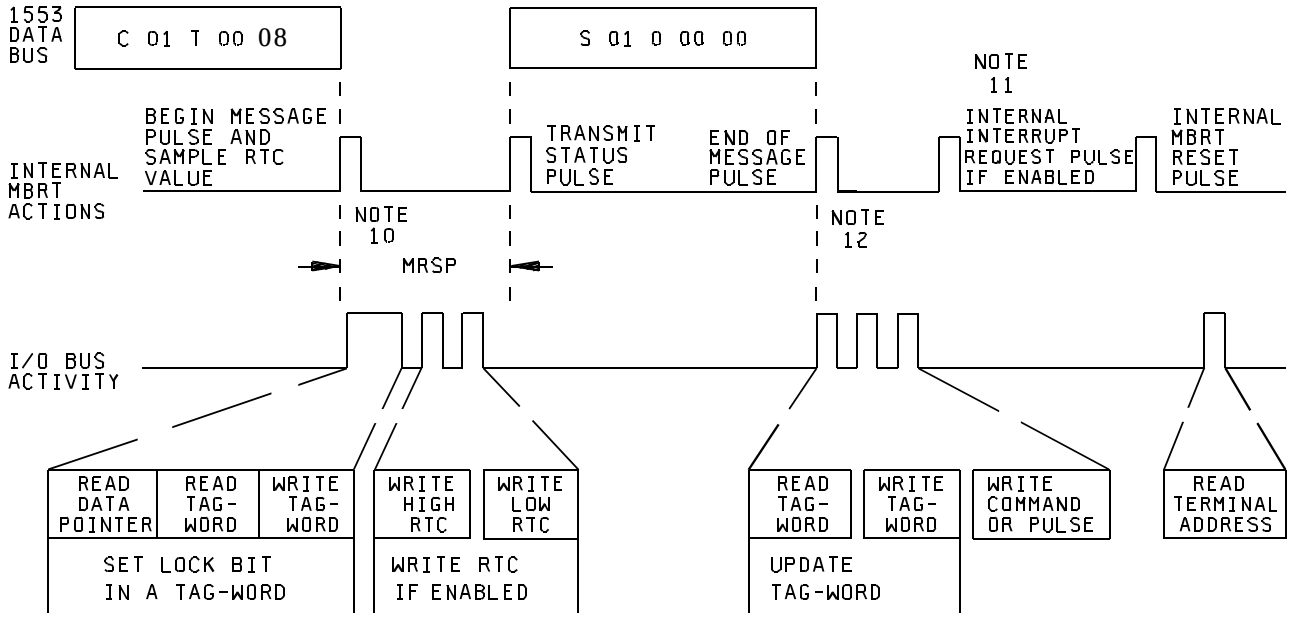


FIGURE 4. Timing diagrams - Continued.

NOTES:
(Notes 1 through 9 describe the HMBRT signal responses to messages on the address, data, and control lines.)

1. The address is latched by the HMBRT on the high-to-low transition of the HCS line. TADS, TADH, and TASLC are referenced to the high-to-low transition of HCS.
2. TACK is a function of the contending access performed by the HMBRT (see table I).
3. The low-to-high transition of HRD or I/O_RD terminates the read cycle.
4. The DTACK line is three stated after delay "TACKH". It is the rise time, a function of the internal 5 kohm pull-up resistor and external load.
5. While INTACK is low, INTPO will be affected by changes in IRQ.
6. In order to support edge triggered interrupt requests, IRQ is returned high "TINAIRQH" nanoseconds after ITACK goes low. If the HMBT is not empty, IRQ will go low "TINAIRQL" nanoseconds after INTACK returns high.
7. After INTACK goes low, the HMBRT waits "TPR" nanoseconds to allow for the propagation of INTPO and INTPI through the daisy chain.
8. The minimum propagation time "TPR" through the daisy chain can be extended by delaying the HRD signal by any amount "TPRE".
9. If HRD falling edge occurs less than "TPR" nanoseconds after INTACK, INTACK starts "TPR" nanoseconds after ITACK, otherwise ITACK starts after the falling edge of HRD.
10. Status response is delayed by MBRT for MRSP = 6.5 microseconds.
11. Internal interrupt request pulse will enter the FIFO immediately if associated level is not masked and IRQ signal will be activated if IRE bit is set in the control word.
12. The exact timing command write and IRQ activation depends on a host bus activity.

FIGURE 4. Timing diagrams - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,2,3,4,5,6,9,10,11
Final electrical parameters	1*,2,3,4,5,6,9,10,11
Group A test requirements	1,2,3,4,5,6,9,10,11
Group C end-point electrical parameters	1,2,3,4,5,6,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall be omitted.

c. Input capacitance shall be measured only for the initial test and after process or design changes which may affect input capacitance.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-7603.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

TABLE III. Pin functions.

Terminal symbol	I/O	Description
TXINH_A	I	Bus A inhibit. This signal inhibits the bus A transmitter
+5 V	I	+5 volt power supply connections (3 pins)
H_ADR1	I	Host address bus bit 1.
H_ADR2	I	Host address bus bit 2.
H_ADR3	I	Host address bus bit 3.
H_ADR4	I	Host address bus bit 4.
H_ADR5	I	Host address bus bit 5.
H_ADR6	I	Host address bus bit 6.
H_ADR7	I	Host address bus bit 7.
H_ADR8	I	Host address bus bit 8.
H_ADR9	I	Host address bus bit 9.
H_ADR10	I	Host address bus bit 10.
H_ADR11	I	Host address bus bit 11.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
H_ADR12	I	Host address bus bit 12.
H_DAT0	I/O	Host data bus bit 0.
H_DAT1	I/O	Host data bus bit 1.
H_DAT2	I/O	Host data bus bit 2.
H_DAT3	I/O	Host data bus bit 3.
H_DAT4	I/O	Host data bus bit 4.
H_DAT5	I/O	Host data bus bit 5.
H_DAT6	I/O	Host data bus bit 6.
H_DAT7	I/O	Host data bus bit 7.
H_DAT8	I/O	Host data bus bit 8.
H_DAT9	I/O	Host data bus bit 9.
H_DAT10	I/O	Host data bus bit 10.
H_DAT11	I/O	Host data bus bit 11.
H_DAT12	I/O	Host data bus bit 12.
H_DAT13	I/O	Host data bus bit 13.
H_DAT14	I/O	Host data bus bit 14.
H_DAT15	I/O	Host data bus bit 15.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{\text{HWRH}}$	I	Host write higher byte (active low).
+5 V	I	+5 volt power supply connections (3 pins)
TXINH_B	I/O	Bus B inhibit. This signal inhibits the bus B transmitter
BUS_B	I/O	1553 Bus B, positive phase signal. This signal should be connected to a bus coupling transformer. Device types 01 and 02 require a turns ratio: 1:2.12 direct, 1:1.5 stub. Technitrol Q1553-5 or equivalent. Device types 03, 04, 05, 06, 07, and 08 require a turns ratio of 1:2.50 direct, 1:1.79 stub. Technitrol Q1553-45 or equivalent.
$\overline{\text{BUS\_B}}$	I/O	1553 Bus B, negative phase signal. This signal should be connected to a bus coupling transformer. Device types 01 and 02 require a turns ratio: 1:2.12 direct, 1:1.5 stub. Technitrol Q1553-5 or equivalent. Device types 03, 04, 05, 06, 07, and 08 require a turns ratio of 1:2.50 direct, 1:1.79 stub. Technitrol Q1553-45 or equivalent.
GND	---	Power supply return connection.
I/O_DAT0	I/O	I/O data bus bit 0.
I/O_DAT1	I/O	I/O data bus bit 1.
I/O_DAT2	I/O	I/O data bus bit 2.
I/O_DAT3	I/O	I/O data bus bit 3.
I/O_DAT4	I/O	I/O data bus bit 4.
I/O_DAT5	I/O	I/O data bus bit 5.
I/O_DAT6	I/O	I/O data bus bit 6.
I/O_DAT7	I/O	I/O data bus bit 7.

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
$\overline{HCS}$	I	Chip select (active low). This signal selects the remote terminal. The falling edge of /HCS is used to latch the host's address and indicates the start of a host memory cycle. During a host read-modify-write cycle, this signal must remain active from the beginning of the read cycle to the end of the write cycle. Note: The host should not hold /HCS active for more than 5 microseconds, otherwise timing errors on the 1553 bus may occur.
+5 V RAM	I	+5 volt power supply connection to RAM.
SSF_TF	I	Subsystem Flag or Terminal Flag.
$\overline{RST}$	I	Initializes all registers and state machines (active low).
CLK10	I	Clock from 10 MHz oscillator.
I/O ADR1	O	I/O address 1.
I/O ADR2	O	I/O address 2.
$\overline{INTPO\_DSC}$	O	Interrupt priority output, disconnect signal. This pin has two functions, depending on the M1760 bit in the RTC Control register. If M1760 = 0, the signal is used to daisy chain interrupt requests on the host bus. When the RT requests an interrupt, this signal is output high; otherwise, this signal is equal to /INTPI. If M1760 = 1, the pin is set to "1" when the store is disconnected.
MDCDRST	O	Mode command reset (active high). This signal is pulsed high whenever a mode command "Reset" is received.
$\overline{INTPI}$	I	Interrupt priority input (active low). This signal is used to daisy chain interrupt requests on the host bus. This signal must be active for the RT to output an interrupt vector.
$\overline{INTACK}$	I	Host interrupt acknowledge (active low). This signal indicates that the host is acknowledging an interrupt. When /HRD = 0, and /INTA = 0, and /HCSN = 1, an interrupt vector is popped form the FIFO, the IVR/AVR registers are updated, and the IVR is outputed onto both the lower and upper bytes of the host data bus.
$\overline{HWRL}$	I	Host write lower byte (active low).
$\overline{HRD}$	I	Host read (active low).

TABLE III. Pin functions - Continued.

Terminal symbol	I/O	Description
CMDS	O	Command strobe (active high). This strobe is used for two I/O operations. When the strobe is active during a write cycle (i.e. CMDS = 1, /I/O WR = 0), valid commands/pulses appear on the I/O bus. When the strobe ia active during a read cycle (i.e. CMDS = 1, /I/O RD = 0), the external address buffer is accessed.
PLSCMD	O	Pulse command (active high). This signal depends on the value of the CMDO bit in the control register. If CMDO = 0, then a pulse is issued whenever a 1553 message accesses a data table with Pulse (3:0) = 14 (decimal) in its tag word. If CMDO = 1, then a pulse is issued whenever a valid broadcast command is received. Note: NTAG bit in control register must be "0" for a pulse output.
$\overline{\text{I/O\_RD}}$	O	I/O read (active low).
$\overline{\text{I/O\_WR}}$	O	I/O write (active low).
$\overline{\text{IRQ}}$	O	Host interrupt request signal (active low, open drain).
$\overline{\text{DTACK}}$	O	Host data transfer acknowledge (active low, open drain). This signal indicates to the host that a data transfer has been completed. When the host is reading data, it takes /HCS low and /HRD low. The HMBRT will bring the /DTACK low to signal that data is on the bus and stable. The host will then read the data on the rising edge of /HRD. When the host is writing data, it takes /HCS low and HWRH low. The HMBRT will bring the /DTACK low to signal that it has taken the data. The host will then take /HWRL and /HWRH high.
BUS_A	I/O	1553 Bus A, positive phase signal. This signal should be connected to a bus coupling transformer. Device types 01 and 02 require a turns ratio: 1:2.12 direct, 1:1.5 stub. Technitrol Q1553-5 or equivalent. Device types 03, 04, 05, 06, 07, and 08 require a turns ratio of 1:2.50 direct, 1:1.79 stub. Technitrol Q1553-45 or equivalent.
$\overline{\text{BUS\_A}}$	I/O	1553 Bus A, negative phase signal. This signal should be connected to a bus coupling transformer. Device types 01 and 02 require a turns ratio: 1:2.12 direct, 1:1.5 stub. Technitrol Q1553-5 or equivalent. Device types 03, 04, 05, 06, 07, and 08 require a turns ratio of 1:2.50 direct, 1:1.79 stub. Technitrol Q1553-45 or equivalent.
TAGCLK_IN	I	Clock input pin for internal time tag counter.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-03-21

Approved sources of supply for SMD 5962-91687 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9168701HXA	57363	NHI-1553RT/883
5962-9168701HXC	57363	NHI-1553RT/883
5962-9168701HYA	57363	NHI-1553RTFP/883
5962-9168701HYC	57363	NHI-1553RTFP/883
5962-9168702HXA	57363	NHI-1554RT/883
5962-9168702HXC	57363	NHI-1554RT/883
5962-9168702HYA	57363	NHI-1554RTFP/883
5962-9168702HYC	57363	NHI-1554RTFP/883
5962-9168703HUA	57363	NHI-1561RTFP/883
5962-9168703HUC	57363	NHI-1561RTFP/883
5962-9168703HZA	57363	NHI-1561RT/883
5962-9168703HZC	57363	NHI-1561RT/883
5962-9168704HUA	57363	NHI-1562RTFP/883
5962-9168704HUC	57363	NHI-1562RTFP/883
5962-9168704HZA	57363	NHI-1562RT/883
5962-9168704HZC	57363	NHI-1562RT/883
5962-9168705HXA	57363	NHI-1572RT/883
5962-9168705HXC	57363	NHI-1572RT/883
5962-9168705HYA	57363	NHI-1572RTFP/883
5962-9168705HYC	57363	NHI-1572RTFP/883
5962-9168706HXA	57363	NHI-1576RT/883
5962-9168706HXC	57363	NHI-1576RT/883
5962-9168706HYA	57363	NHI-1576RTFP/883
5962-9168706HYC	57363	NHI-1576RTFP/883

1/ The lead finish shown for each PIN is available from the manufacturer listed for that part.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9168707HUA	57363	NHI-1591RTFP/883
5962-9168707HUC	57363	NHI-1591RTFP/883
5962-9168707HZA	57363	NHI-1591RT/883
5962-9168707HZC	57363	NHI-1591RT/883
5962-9168708HUA	57363	NHI-1592RTFP/883
5962-9168708HUC	57363	NHI-1592RTFP/883
5962-9168708HZA	57363	NHI-1592RT/883
5962-9168708HZC	57363	NHI-1592RT/883
5962-9168709HUA	57363	NHI-15101RTFP/883
5962-9168709HUC	57363	NHI-15101RTFP/883
5962-9168709HZA	57363	NHI-15101RT/883
5962-9168709HZC	57363	NHI-15101RT/883
5962-9168710HUA	57363	NHI-15102RTFP/883
5962-9168710HUC	57363	NHI-15102RTFP/883
5962-9168710HZA	57363	NHI-15102RT/883
5962-9168710HZC	57363	NHI-15102RT/883

1/ The lead finish shown for each PIN is available from the manufacturer listed for that part.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
57363	National Hybrid, Incorproated 2200 Smithtown Avenue Ronkonkoma, NY 11779

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.