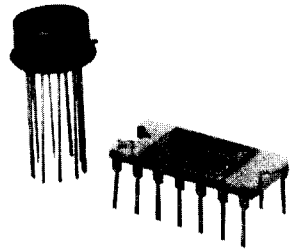
BURR-BROWN®



VFC62

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  - ±0.005% max at 10kHz FS
  - ±0.03% max at 100kHz FS
  - ±0.1% typ at 1MHz FS
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE
- ACTIVE PULL-UP OUTPUT

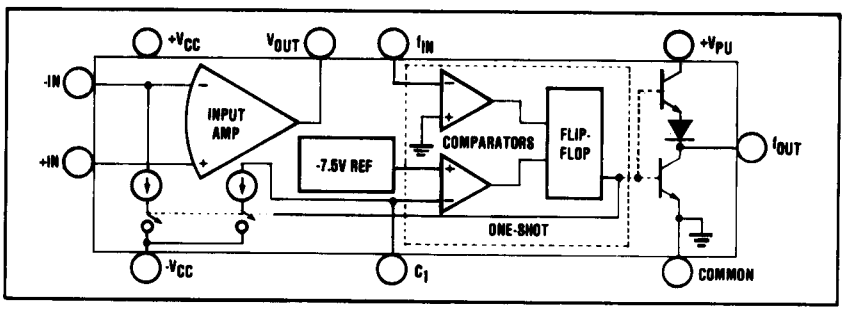
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- 2-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC62 monolithic voltage-to-frequency and frequency-to voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. In the noise-immune digital form the analog signal may be transmitted long distances without degradation. It may be converted to a binary number with a counter or microprocessor or may be returned to analog form using a frequency-to-voltage converter.

The digital output is an active pull-up type which provides better load driving capability than the usual open collector outputs. Output pulses are DTL, TTL and CMOS compatible. High accuracy (±0.005% max nonlinearity at 10kHz) is achieved with relatively few external components. Only one resistor and two capacitors are required.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-484D

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC62BG/BM/SM MIN	VFC62BG/BM/SM TYP	VFC62BG/BM/SM MAX	VFC62CG/CM MIN	VFC62CG/CM TYP	VFC62CG/CM MAX	UNITS
V/F CONVERTER $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	> 0		Note 2	*		*	V
	Fig. 4 with $e_1 = 0$	< 0		-10	*		*	V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 ‖ 5	650 ‖ 5		*	*		kΩ ‖ pF
Common-mode Impedance		300 ‖ 3	500 ‖ 3		*	*		kΩ ‖ pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig. 4 with e_2 + = 0(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% of FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.03		*	*	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% of FSR
Offset Error	Input Offset Voltage(3)			±15			*	ppm of FSR
Offset Drift(7)			±0.5			*		ppm of FSR/°C
Gain Error(3)			±5	±10			*	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR/°C
Full Scale Drift (offset drift & gain drift(7)(8)(9)	f = 10kHz			50			20	ppm of FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			*		
Overload Recovery	< 50% overload		Note 10			*		
ACTIVE PULL-UP OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Voltage, Logic "1"		V_{PU} - 2.6		V_{PU}	*		*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		nsec
F/V CONVERTER V_{OUT} = 7.5 R_1C_1 F_{IN}, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 ‖ 10	150 ‖ 10		*	*		kΩ ‖ pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		-V_{CC}		-0.05	*		*	V
Pulse-width Range		0.25			*			µsec
OUTPUT FROM OP AMP								
Voltage	I_O = 6mA	0 to +10			*	*		V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-loop			0.1			*	Ω
Capacitive Load	Without oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range, V_{CC}		±13		±20	*		*	V
Pull-up Voltage		+3.5		+V_{CC}	*		*	V
Quiescent Current	not including load current		±6	±7.5		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Operating								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Storage		-65		+150	-65		+150	°C

*Specification the same as for VFC62BG/BM/SM.

NOTES:
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section.
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section.
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For $e_1 = 0$ typical linearity errors are 0.01% at 10kHz, 0.2% at 100kHz.
7. Exclusive of external components drift.
8. FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical.

ABSOLUTE MAXIMUM RATINGS

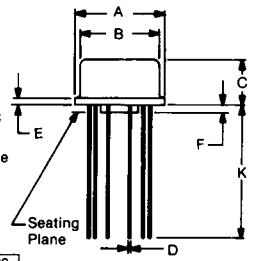
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	$\pm V_{CC}$
Input Voltage, +Input	$\pm V_{CC}$
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

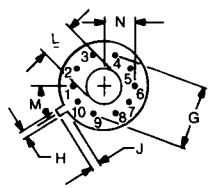
MECHANICAL

VFC62BM, CM/SM TO-100 PACKAGE

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



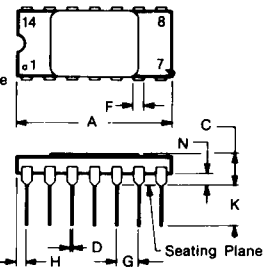


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.70	—
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC62BG/CG CERAMIC DUAL-IN-LINE

NOTE: Leads in true position within .010" (0.25mm) R at MMC at seating plane.

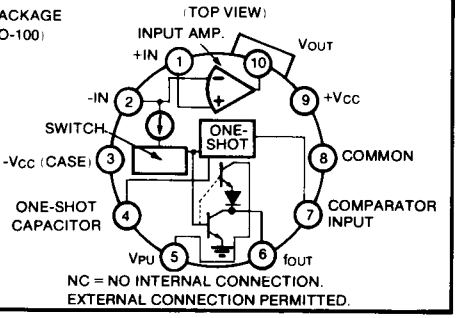
Pin numbers shown for reference only. Numbers may not be marked on package.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M	—	10°	—	10°
N	.009	.060	0.23	1.52

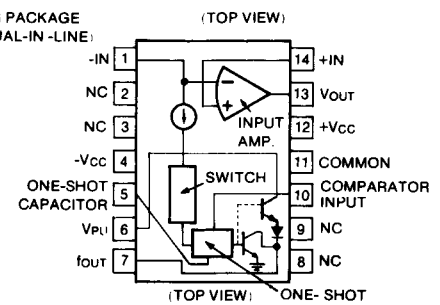
PIN CONFIGURATIONS

M PACKAGE (TO-100) (TOP VIEW)



NC = NO INTERNAL CONNECTION.
EXTERNAL CONNECTION PERMITTED.

G PACKAGE (DUAL-IN-LINE) (TOP VIEW)



(TOP VIEW)

DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC62 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

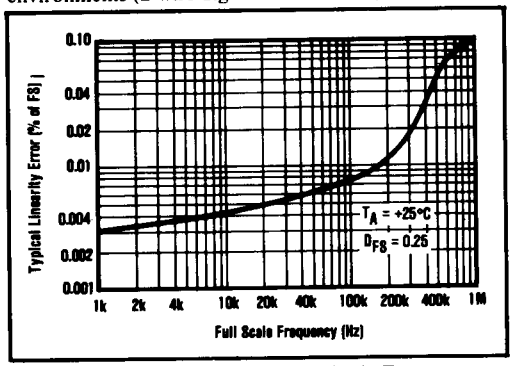


FIGURE 1. Linearity Error vs Full Scale Frequency.

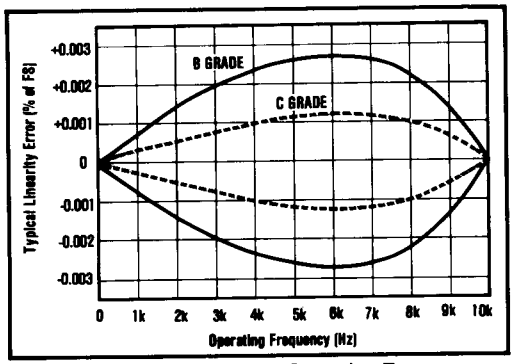


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC62 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC62.

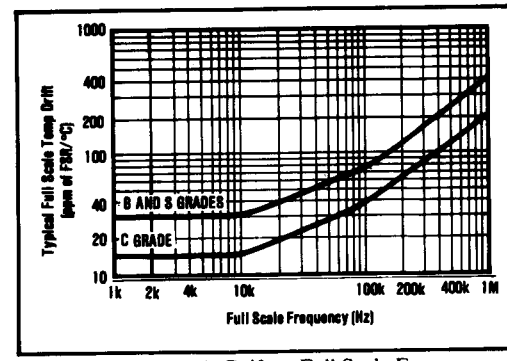


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC62 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC62 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μsec.

THEORY OF OPERATION

The VFC62 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an active pull-up output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC62 is derived as follows

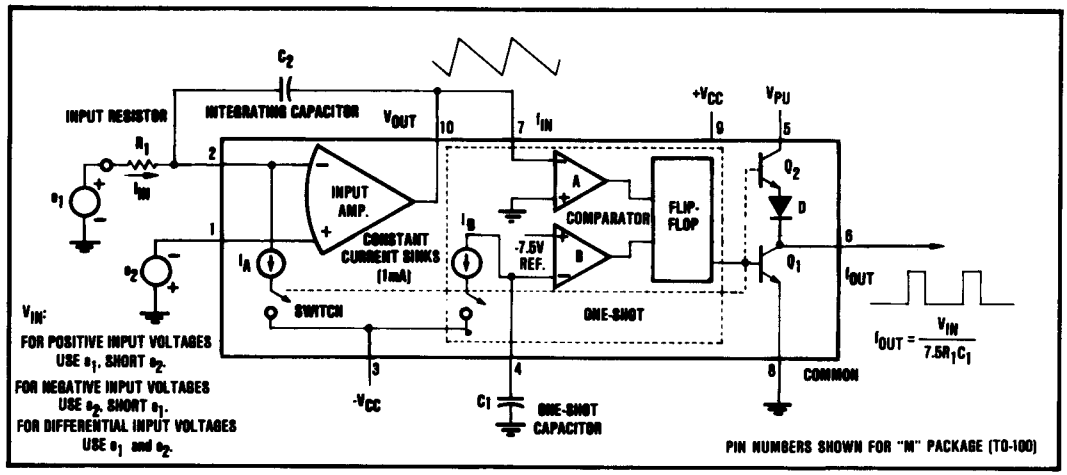


FIGURE 4. Functional Block Diagram of the VFC62.

for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time $t_1 + t_2$, the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}\,(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

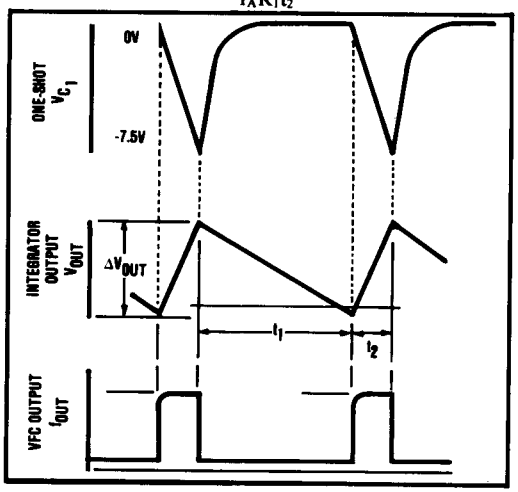


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yields } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

$$\text{Since } I_A = I_B \text{ the result is}$$

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC62 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC62, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user-determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = \text{PW} \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ \text{max} / R_1}{1\text{mA}} = \frac{I_{IN}\ \text{max}}{1\text{mA}}$$

Thus $D_{FS} = 0.25$ corresponds to I_{IN} max = 0.25mA.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC62 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

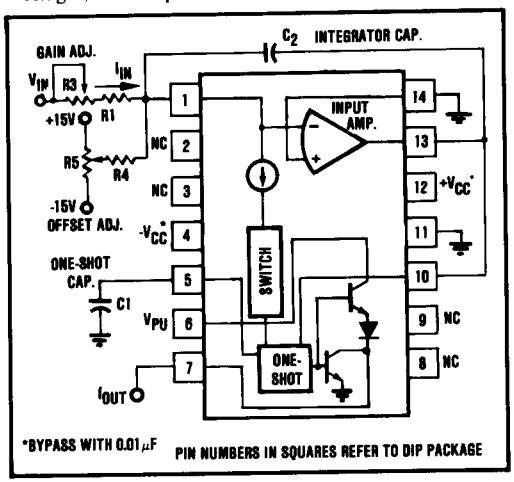


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

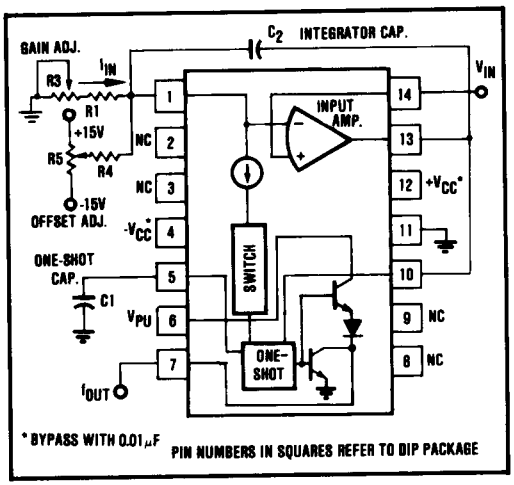


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, and (5) selecting the integrator capacitor C_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value of R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1\ (pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC62 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

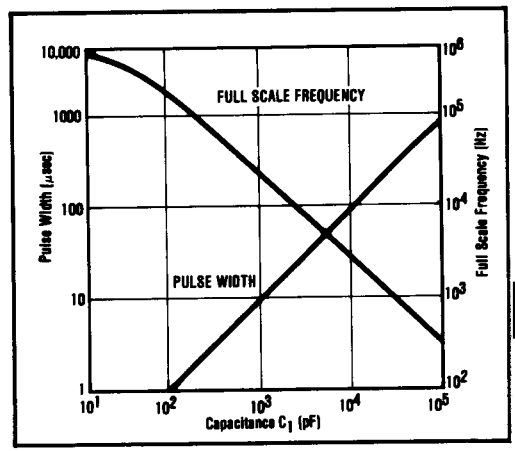


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

determine a range of acceptable values,

$$C_2\,(\mu F) = \begin{cases} \frac{100}{f_{FS}}\text{; if } f_{FS} \leq 100\text{kHz} \\ 0.001\text{; if } 100\text{kHz} < f_{FS} \leq 500\text{kHz} \\ 0.0005\text{; if } f_{FS} > 500\text{kHz} \end{cases} \quad (13)$$

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC62 is 0.015% of FSR/% maximum. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

Internal circuitry causes some current to flow in the common connection (pin 11 on DIP package). Current flowing into the f_{OUT} pin (logic sink current) will also contribute to this current. It is advisable to separate this common lead ground from the analog ground associated with the integrator input to avoid errors produced by these currents flowing through any ground return impedance.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\quad [(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100\text{kHz}] - 15$

$= 315\text{pF}$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\text{ max}/0.25\text{mA}$ $\quad V_{IN}\text{ max}/0.5\text{mA}$ if $D_{FS} = 0.5$

$= 10\text{V}/0.25\text{mA}$

$= 40\text{k}\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100\text{kHz}$

$= 0.001\mu\text{F}$

Choose a 0.001μF capacitor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC62 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1T (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

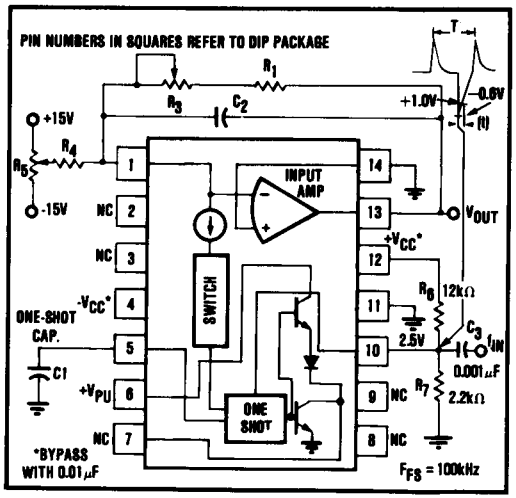


FIGURE 9. Connection Diagram for F/V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC62 ideal for a variety of VFC applications. High accuracy allows the VFC62 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC62.

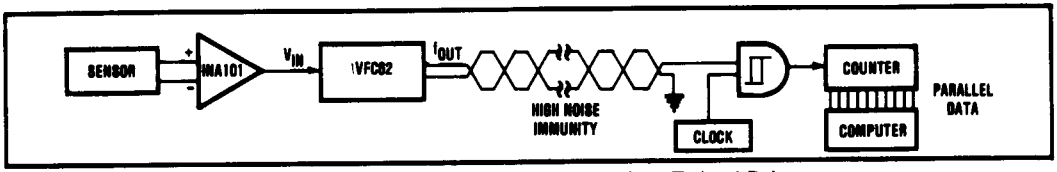


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

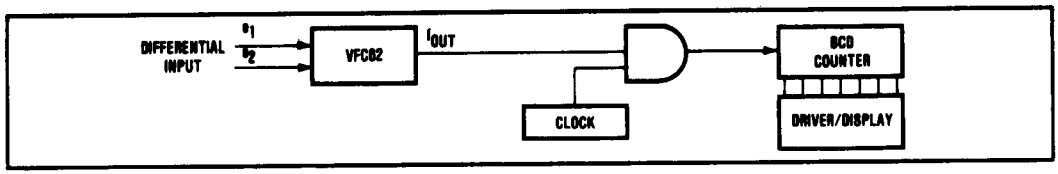


FIGURE 11. Inexpensive Digital Panel Meter.

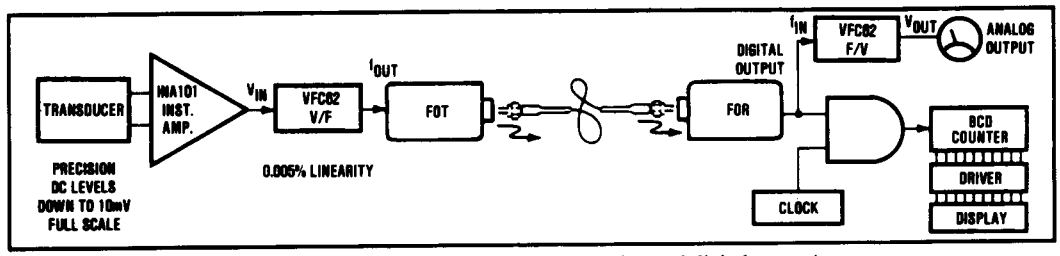


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

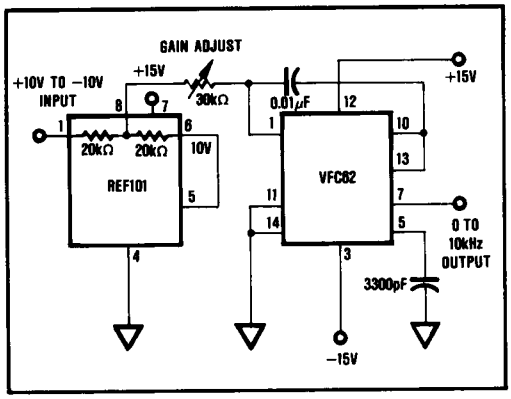


FIGURE 13. Bipolar input is accomplished by offsetting the input to the VFC with a reference voltage. Accurately matched resistors in the REF101 provide a stable half-scale output frequency at zero volts input.

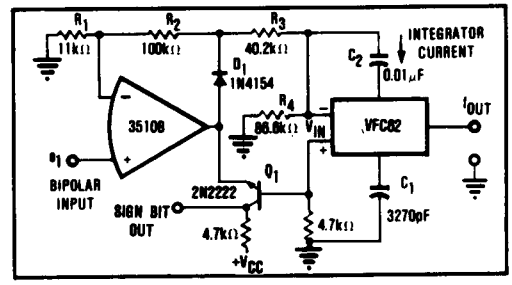


FIGURE 14. Absolute value circuit with the VFC62. Op amp, D_1 and Q_1 (its base-emitter junction functioning as a diode) provide full-wave rectification of bipolar input voltages. VFC output frequency is proportional to $|e_1|$. The sign bit output provides indication of the input polarity.