

# MAS9180

This is preliminary information on a new product under development. Micro Analog Systems Oy reserves the right to make any changes without notice.

**Preliminary**

## AM Receiver IC

- Single Band Receiver IC
- High Sensitivity
- Very Low Power Consumption
- Wide Supply Voltage Range
- Power Down Control
- Control for AGC On
- High Selectivity by Crystal Filter
- Fast Startup Feature

### DESCRIPTION

The MAS9180 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiver. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly

by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary.

MAS9180 has differential input and two options for compensating shunt capacitances of different crystals (See ordering information on page 12).

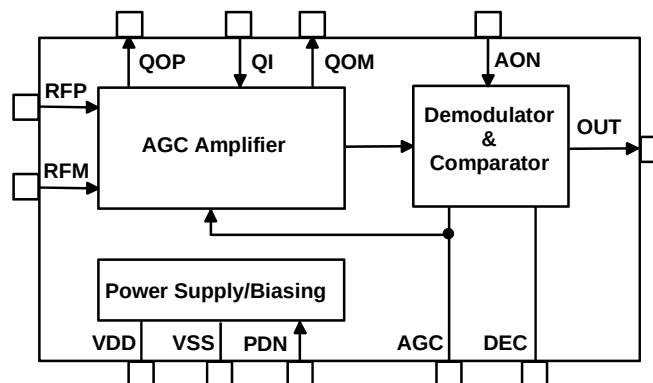
### FEATURES

- Single Band Receiver IC
- Highly Sensitive AM Receiver, 0.4  $\mu\text{V}_{\text{RMS}}$  typ.
- Wide Supply Voltage Range from 1.1 V to 5 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter

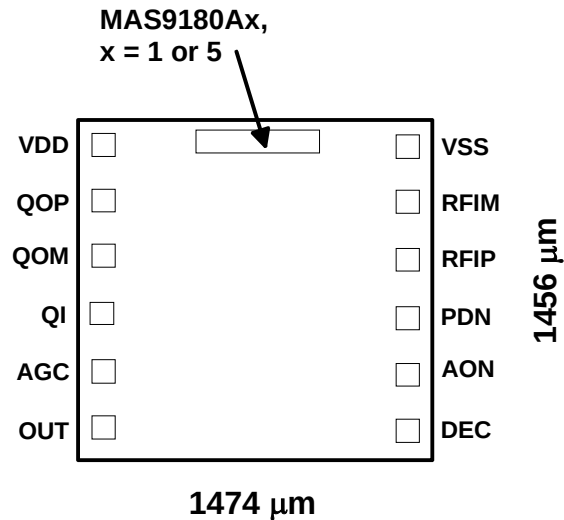
### APPLICATIONS

- Single Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK) and BPC (China)

### BLOCK DIAGRAM



## MAS9180 PAD LAYOUT



DIE size = 1.47 x 1.46 mm; round PAD  $\varnothing$  80  $\mu\text{m}$

**Note:** Because the substrate of the die is internally connected to VDD, the die has to be connected to VDD or left floating. Please make sure that VDD is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

**Note:** Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

| Pad Identification                                                  | Name | X-coordinate       | Y-coordinate       | Note |
|---------------------------------------------------------------------|------|--------------------|--------------------|------|
| Power Supply Voltage                                                | VDD  | 174 $\mu\text{m}$  | 1262 $\mu\text{m}$ |      |
| Positive Quartz Filter Output for Crystal                           | QOP  | 174 $\mu\text{m}$  | 1057 $\mu\text{m}$ |      |
| Negative Quartz Filter Output for Crystal                           | QOM  | 174 $\mu\text{m}$  | 854 $\mu\text{m}$  | 4    |
| Quartz Filter Input for Crystal and External Compensation Capacitor | QI   | 174 $\mu\text{m}$  | 648 $\mu\text{m}$  |      |
| AGC Capacitor                                                       | AGC  | 174 $\mu\text{m}$  | 444 $\mu\text{m}$  |      |
| Receiver Output                                                     | OUT  | 175 $\mu\text{m}$  | 240 $\mu\text{m}$  | 1    |
| Demodulator Capacitor                                               | DEC  | 1295 $\mu\text{m}$ | 225 $\mu\text{m}$  |      |
| AGC On Control                                                      | AON  | 1295 $\mu\text{m}$ | 425 $\mu\text{m}$  | 2    |
| Power Down                                                          | PDN  | 1295 $\mu\text{m}$ | 624 $\mu\text{m}$  | 3    |
| Positive Receiver Input                                             | RFIP | 1295 $\mu\text{m}$ | 825 $\mu\text{m}$  | 5    |
| Negative Receiver Input                                             | RFIM | 1295 $\mu\text{m}$ | 1039 $\mu\text{m}$ | 5    |
| Power Supply Ground                                                 | VSS  | 1282 $\mu\text{m}$ | 1200 $\mu\text{m}$ |      |

Notes:

- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu\text{A}$
  - at power down the output is pulled to VSS (pull down switch)
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up with current  $< 1 \mu\text{A}$  which is switched off at power down
- PDN = VSS means receiver on; PDN = VDD means receiver off  
Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
- External crystal compensation capacitor pin QOM is connected only in MAS9190A5 version. It is left unconnected in MAS9180A1 version which has internal compensation capacitor.
- Receiver inputs RFIP and RFIM have both 600 k $\Omega$  biasing MOSFET-transistors towards ground

## ABSOLUTE MAXIMUM RATINGS

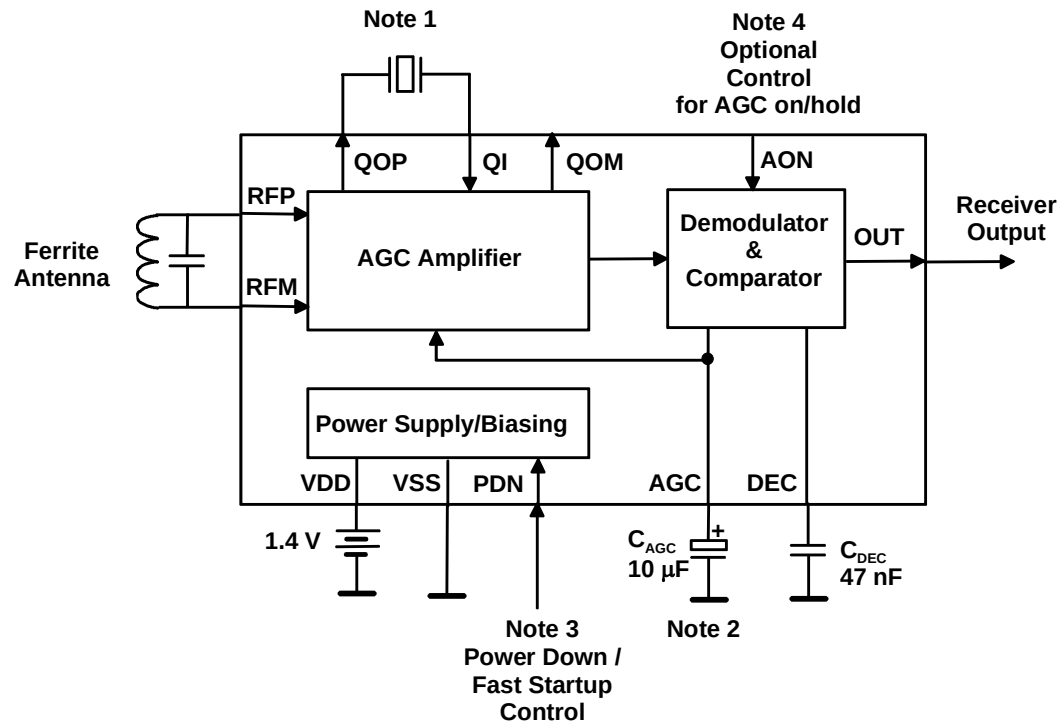
| Parameter             | Symbol          | Conditions | Min          | Max          | Unit |
|-----------------------|-----------------|------------|--------------|--------------|------|
| Supply Voltage        | $V_{DD}-V_{SS}$ |            | -0.3         | 6            | V    |
| Input Voltage         | $V_{IN}$        |            | $V_{SS}-0.3$ | $V_{DD}+0.3$ | V    |
| Power Dissipation     | $P_{MAX}$       |            |              | 100          | mW   |
| Operating Temperature | $T_{OP}$        |            | -40          | +85          | °C   |
| Storage Temperature   | $T_{ST}$        |            | -55          | +150         | °C   |

## ELECTRICAL CHARACTERISTICS

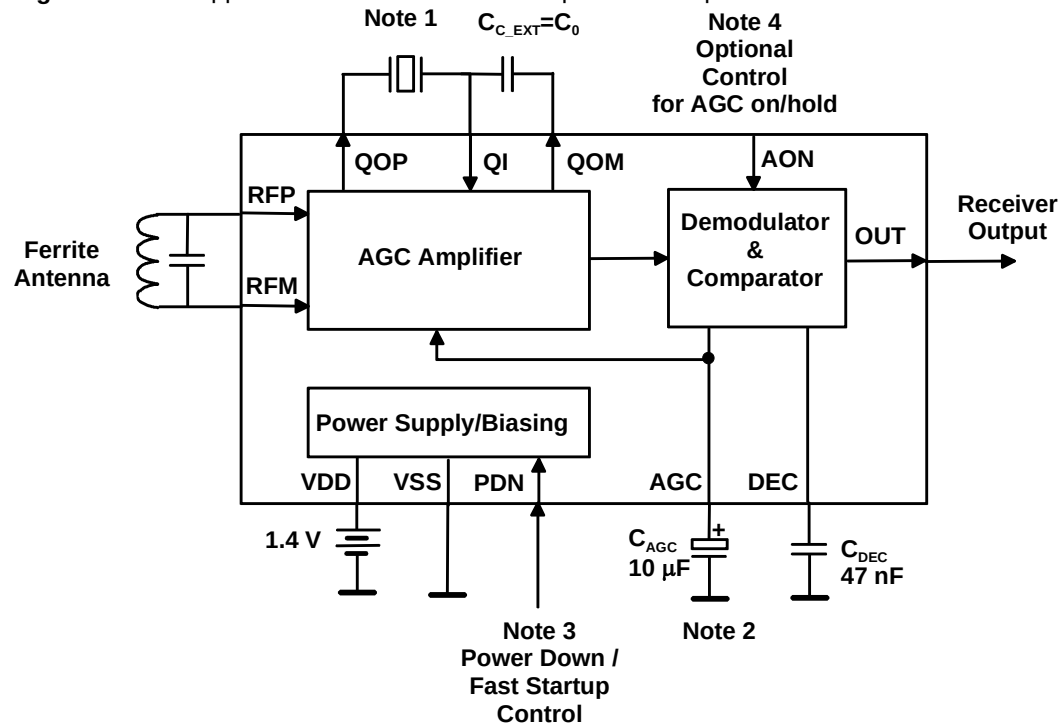
Operating Conditions:  $V_{DD} = 1.4V$ , Temperature = 25°C

| Parameter                                                     | Symbol               | Conditions                                                                                                                                                       | Min         | Typ                  | Max         | Unit          |
|---------------------------------------------------------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|----------------------|-------------|---------------|
| Operating Voltage                                             | $V_{DD}$             |                                                                                                                                                                  | 1.10        |                      | 5           | V             |
| Current Consumption                                           | $I_{DD}$             | $V_{DD}=1.4V$ , $V_{IN}=0.4\mu V_{rms}$<br>$V_{DD}=1.4V$ , $V_{IN}=20mV_{rms}$<br>$V_{DD}=3.6V$ , $V_{IN}=0.4\mu V_{rms}$<br>$V_{DD}=3.6V$ , $V_{IN}=20mV_{rms}$ |             | 49<br>36<br>50<br>38 | 75<br>50    | $\mu A$       |
| Stand-By Current                                              | $I_{DDoff}$          |                                                                                                                                                                  |             |                      | 0.1         | $\mu A$       |
| Input Frequency Range                                         | $f_{IN}$             |                                                                                                                                                                  | 40          |                      | 100         | kHz           |
| Minimum Input Voltage                                         | $V_{INmin}$          |                                                                                                                                                                  |             | 0.4                  | 1           | $\mu V_{rms}$ |
| Maximum Input Voltage                                         | $V_{INmax}$          |                                                                                                                                                                  | 20          |                      |             | mVrms         |
| Receiver Input Resistance                                     | $R_{RFI}$            | $f=40kHz..77.5kHz$                                                                                                                                               |             | 330                  |             | k $\Omega$    |
| Receiver Input Capacitance                                    | $C_{RFI}$            |                                                                                                                                                                  |             | 4.5                  |             | pF            |
| Input Levels $ I_{IN}  < 0.5\mu A$                            | $V_{IL}$<br>$V_{IH}$ |                                                                                                                                                                  | $0.8V_{DD}$ |                      | $0.2V_{DD}$ | V             |
| Output Current<br>$V_{OL} < 0.2V_{DD}$ ; $V_{OH} > 0.8V_{DD}$ | $ I_{OUT} $          |                                                                                                                                                                  | 5           |                      |             | $\mu A$       |
| Output Pulse                                                  | $T_{100ms}$          | $1\mu V_{rms} \leq V_{IN} \leq 20mV_{rms}$                                                                                                                       | 50          |                      | 140         | ms            |
|                                                               | $T_{200ms}$          | $1\mu V_{rms} \leq V_{IN} \leq 20mV_{rms}$                                                                                                                       | 150         |                      | 230         | ms            |
|                                                               | $T_{500ms}$          | $1\mu V_{rms} \leq V_{IN} \leq 20mV_{rms}$                                                                                                                       | 400         | 500                  | 600         | ms            |
|                                                               | $T_{800ms}$          | $1\mu V_{rms} \leq V_{IN} \leq 20mV_{rms}$                                                                                                                       | 700         | 800                  | 900         | ms            |
| Startup Time                                                  | $T_{Start}$          | Fast Start-up, $V_{IN}=0.4\mu V_{rms}$<br>Fast Start-up, $V_{IN}=20mV_{rms}$                                                                                     |             | 1.3<br>3.5           |             | s             |
| Output Delay Time                                             | $T_{Delay}$          |                                                                                                                                                                  |             | 50                   | 100         | ms            |

## TYPICAL APPLICATION

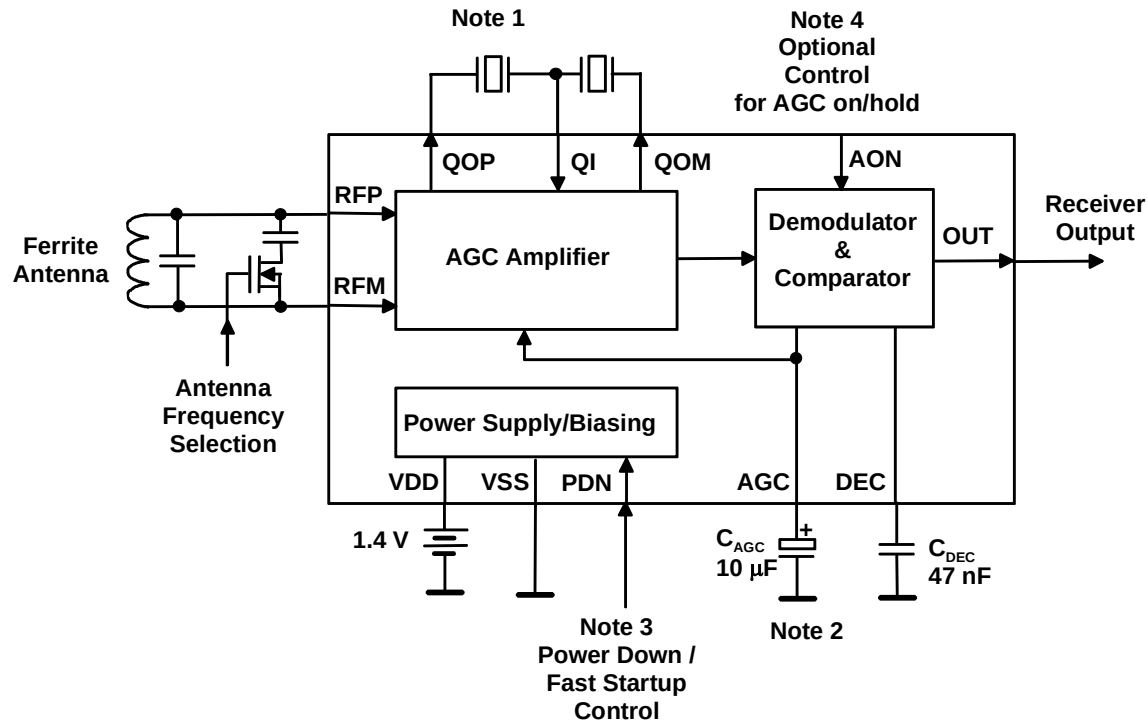


**Figure 1** Application circuit of internal compensation capacitance version MAS9180A1.



**Figure 2** Application circuit of external compensation capacitance version MAS9180A5.

## TYPICAL APPLICATION (Continued)



**Figure 3** Dual band application circuit of external compensation capacitance version MAS9180A5.

### Note 1: Crystals

The crystal as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 1). The crystal shunt capacitance  $C_0$  should be matched as well as possible with the internal shunt capacitance compensation capacitor  $C_C$  of MAS9180. MAS9180A5 has also option for external crystal compensation capacitor. The external compensation capacitor should be matched as well as possible with crystal shunt capacitance. See Compensation Capacitance Options on table 2.

**Table 1** Time-Signal System Frequencies

| Time-Signal System | Location       | Antenna Frequency | Recommended Crystal Frequency |
|--------------------|----------------|-------------------|-------------------------------|
| DCF77              | Germany        | 77.5 kHz          | 77.503 kHz                    |
| MSF                | United Kingdom | 60 kHz            | 60.003 kHz                    |
| WWVB               | USA            | 60 kHz            | 60.003 kHz                    |
| JJY                | Japan          | 40 kHz and 60 kHz | 40.003 kHz and 60.003 kHz     |
| BPC                | China          | 68.5 kHz          | 68.505 kHz                    |

**Table 2** Compensation Capacitance Options

| Device    | $C_C$        | Crystal Description                               |
|-----------|--------------|---------------------------------------------------|
| MAS9180A1 | 0.75 pF      | For low $C_0$ crystal                             |
| MAS9180A5 | $C_{C\_EXT}$ | For any crystals, external compensation capacitor |

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example crystal with 1 pF floating package shunt capacitance can have 0.85 pF grounded package shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

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**TYPICAL APPLICATION (Continued)**

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In dual band receiver configuration the crystals can be connected in parallel thus external compensation capacitor value  $C_{C\_EXT}$  must be sum of two crystals' shunt capacitances. Instead of parallel crystal connection it is also possible to connect other crystal from QOP pin and the other crystal from QOM pin to common QI pin (figure 3). In this circuit configuration no external compensation capacitor is required since the crystals compensate each other. The sensitivity of dual band receiver configuration will be lower than that of single band receiver configuration since the noise band width of crystal filter with two parallel crystals is double.

**Note 2: AGC Capacitor**

The AGC and DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum 100 M $\Omega$ . Also probes with at least 100 M $\Omega$  impedance should be used for voltage probing of AGC and DEC pins. DEC capacitor can be low leakage chip capacitor.

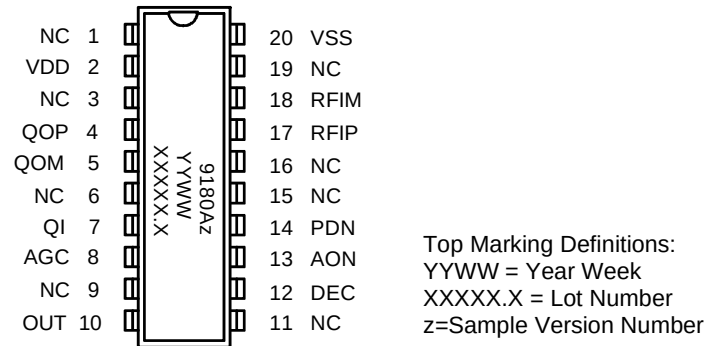
**Note 3: Power Down / Fast Startup Control**

Both power down and fast startup are controlled using the PDN pin. The device is in power down (turned off) if PDN = VDD and in power up (turned on) if PDN = VSS. Fast startup is triggered automatically by the falling edge of PDN signal, i.e., controlling device from power down to power up. The VDD must be high before falling edge of PDN to guarantee proper operation of fast startup circuitry. The startup time without proper fast startup control can be several minutes but with fast startup it is shortened typically to few seconds.

**Note 4: Optional Control for AGC On/Hold**

AON control pin has internal pull up which turns AGC circuit on all the time if AON pin is left unconnected. Optionally AON control can be used to hold and release AGC circuit. Stepper motor drive etc. can produce disturbing amount of noise which can shift the input amplifier gain to unoptimal level. This can be avoided by controlling AGC hold (AON=VSS) during stepper motor drive periods and releasing AGC (AON=VDD) when motors are not driven.

## MAS9180 SAMPLES IN SBDIL 20 PACKAGE



## PIN DESCRIPTION

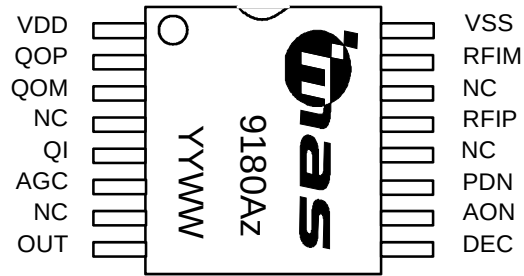
| Pin Name | Pin | Type | Function                                                                            | Note |
|----------|-----|------|-------------------------------------------------------------------------------------|------|
| NC       | 1   |      |                                                                                     |      |
| VDD      | 2   | P    | Positive Power Supply                                                               |      |
| NC       | 3   |      |                                                                                     |      |
| QOP      | 4   | AO   | Positive Quartz Filter Output for Crystal                                           |      |
| QOM      | 5   |      | Negative Quartz Filter Output for External Compensation Capacitor or Second Crystal | 5    |
| NC       | 6   |      |                                                                                     | 1    |
| QI       | 7   | AI   | Quartz Filter Input for Crystal and External Compensation Capacitor                 |      |
| AGC      | 8   | AO   | AGC Capacitor                                                                       |      |
| NC       | 9   |      |                                                                                     |      |
| OUT      | 10  | DO   | Receiver Output                                                                     | 2    |
| NC       | 11  |      |                                                                                     |      |
| DEC      | 12  | AO   | Demodulator Capacitor                                                               |      |
| AON      | 13  | DI   | AGC On Control                                                                      | 3    |
| PDN      | 14  | DI   | Power Down Input                                                                    | 4    |
| NC       | 15  |      |                                                                                     |      |
| NC       | 16  |      |                                                                                     |      |
| RFIP     | 17  | AI   | Positive Receiver Input                                                             | 6    |
| RFIM     | 18  | AI   | Negative Receiver Input                                                             | 6    |
| NC       | 19  |      |                                                                                     |      |
| VSS      | 20  | G    | Power Supply Ground                                                                 |      |

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

### Notes:

- Pin 6 between QOM and QI must be connected to VSS to eliminate DIL package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu A$
  - at power down the output is pulled to VSS (pull down switch)
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up with current  $< 1 \mu A$  which is switched off at power down
- PDN = VSS means receiver on; PDN = VDD means receiver off
  - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
- External crystal compensation capacitor pin QOM is connected only in MAS9190A5 version. It is left unconnected in MAS9180A1 version which has internal compensation capacitor.
- Receiver inputs RFIP and RFIM have both 600 k $\Omega$  biasing MOSFET-transistors towards ground

## PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE



Top Marking Definitions:  
z = Version Number  
YYWW = Year Week

## PIN DESCRIPTION

| Pin Name | Pin | Type | Function                                                                            | Note |
|----------|-----|------|-------------------------------------------------------------------------------------|------|
| VDD      | 1   | P    | Positive Power Supply                                                               |      |
| QOP      | 2   | AO   | Positive Quartz Filter Output for Crystal                                           |      |
| QOM      | 3   | AO   | Negative Quartz Filter Output for External Compensation Capacitor or Second Crystal | 5    |
| NC       | 4   |      |                                                                                     | 1    |
| QI       | 5   | AI   | Quartz Filter Input for Crystal and External Compensation Capacitor                 |      |
| AGC      | 6   | AO   | AGC Capacitor                                                                       |      |
| NC       | 7   |      |                                                                                     |      |
| OUT      | 8   | DO   | Receiver Output                                                                     | 2    |
| DEC      | 9   | AO   | Demodulator Capacitor                                                               |      |
| AON      | 10  | DI   | AGC On Control                                                                      | 3    |
| PDN      | 11  | DI   | Power Down Input                                                                    | 4    |
| NC       | 12  |      |                                                                                     |      |
| RFIP     | 13  | AI   | Positive Receiver Input                                                             | 6    |
| NC       | 14  |      |                                                                                     |      |
| RFIM     | 15  | AI   | Negative Receiver Input                                                             | 6    |
| VSS      | 16  | G    | Power Supply Ground                                                                 |      |

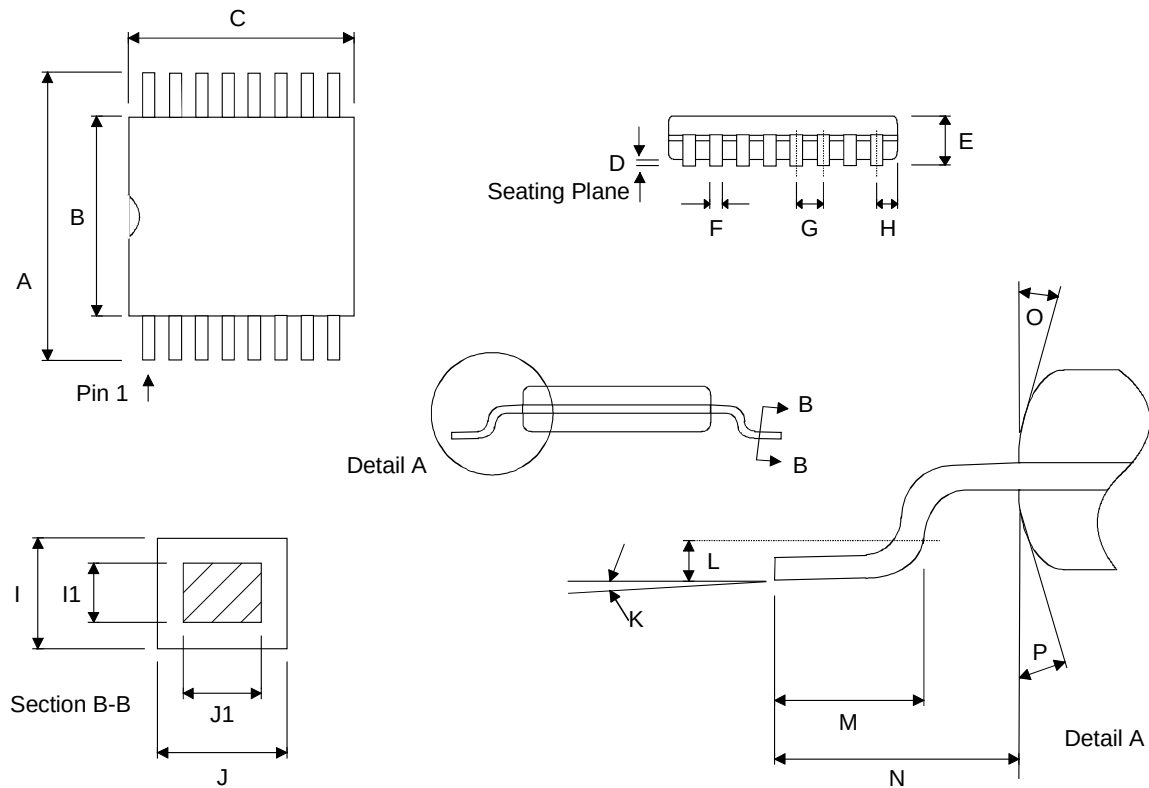
A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

### Notes:

- Pin 4 between quartz crystal filter pins must be connected to VSS to eliminate package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
- OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
  - the output is a current source/sink with  $|I_{OUT}| > 5 \mu A$
  - at power down the output is pulled to VSS (pull down switch)
- AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
  - Internal pull-up (to AGC on) with current  $< 1 \mu A$  which is switched off at power down
- PDN = VSS means receiver on; PDN = VDD means receiver off
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# PACKAGE (TSSOP16) OUTLINES



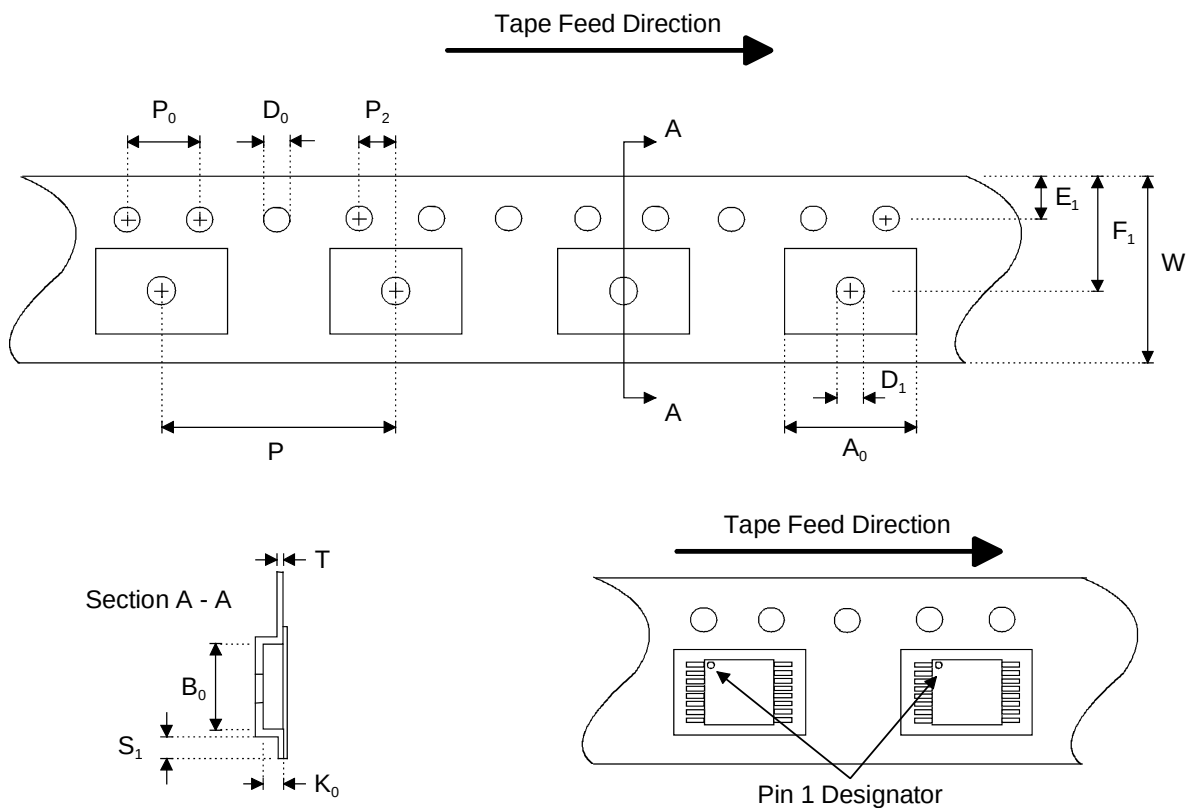
| Dimension                                               | Min      | Max  | Unit |
|---------------------------------------------------------|----------|------|------|
| A                                                       | 6.40 BSC |      | mm   |
| B                                                       | 4.30     | 4.50 | mm   |
| C                                                       | 5.00 BSC |      | mm   |
| D                                                       | 0.05     | 0.15 | mm   |
| E                                                       |          | 1.10 | mm   |
| F                                                       | 0.19     | 0.30 | mm   |
| G                                                       | 0.65 BSC |      | mm   |
| H                                                       | 0.18     | 0.28 | mm   |
| I                                                       | 0.09     | 0.20 | mm   |
| I1                                                      | 0.09     | 0.16 | mm   |
| J                                                       | 0.19     | 0.30 | mm   |
| J1                                                      | 0.19     | 0.25 | mm   |
| K                                                       | 0°       | 8°   |      |
| L                                                       | 0.24     | 0.26 | mm   |
| M                                                       | 0.50     | 0.75 | mm   |
| (The length of a terminal for soldering to a substrate) |          |      |      |
| N                                                       | 1.00 REF |      | mm   |
| O                                                       | 12°      |      |      |
| P                                                       | 12°      |      |      |

Dimensions do not include mold flash, protrusions, or gate burrs.  
All dimensions are in accordance with JEDEC standard MO-153.

## SOLDERING INFORMATION

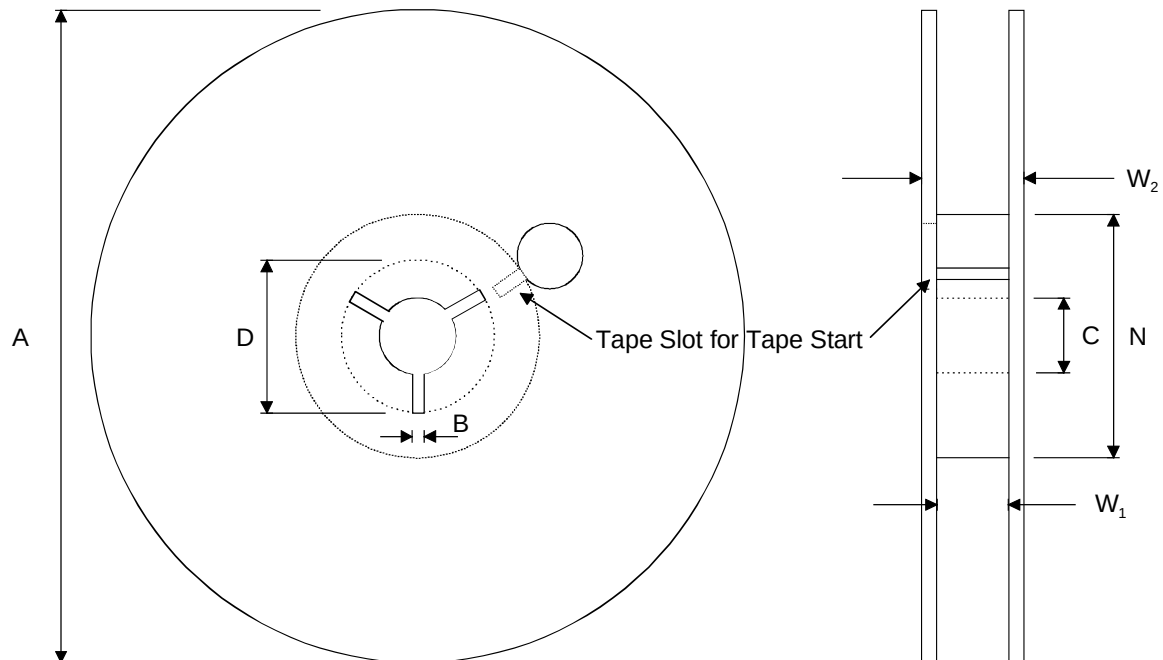
|                                 |                                                                                                                                  |
|---------------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| Resistance to Soldering Heat    | According to RSH test IEC 68-2-58/20 2*220°C                                                                                     |
| Maximum Temperature             | 240°C                                                                                                                            |
| Maximum Number of Reflow Cycles | 2                                                                                                                                |
| Reflow profile                  | Thermal profile parameters stated in JESD22-A113 should not be exceeded. <a href="http://www.jedec.org">http://www.jedec.org</a> |
| Seating Plane Co-planarity      | max 0.08 mm                                                                                                                      |
| Lead Finish                     | Solder plate 7.62 - 25.4 $\mu$ m, material Sn 85% Pb 15%                                                                         |

## EMBOSED TAPE SPECIFICATIONS



| Dimension | Min                | Max   | Unit |
|-----------|--------------------|-------|------|
| $A_0$     | 6.50               | 6.70  | mm   |
| $B_0$     | 5.20               | 5.40  | mm   |
| $D_0$     | 1.50 +0.10 / -0.00 |       | mm   |
| $D_1$     | 1.50               |       | mm   |
| $E_1$     | 1.65               | 1.85  | mm   |
| $F_1$     | 7.20               | 7.30  | mm   |
| $K_0$     | 1.20               | 1.40  | mm   |
| $P$       | 11.90              | 12.10 | mm   |
| $P_0$     | 4.0                |       | mm   |
| $P_2$     | 1.95               | 2.05  | mm   |
| $S_1$     | 0.6                |       | mm   |
| $T$       | 0.25               | 0.35  | mm   |
| $W$       | 11.70              | 12.30 | mm   |

## REEL SPECIFICATIONS

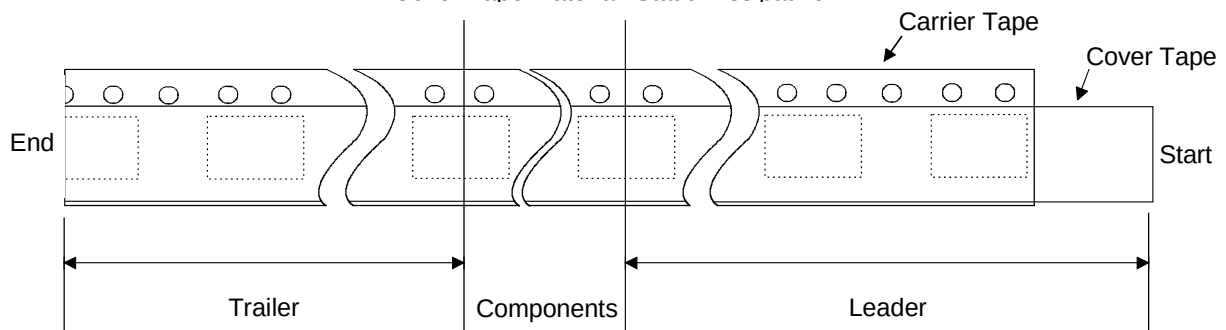


2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative

Carrier Tape Material: Conductive

Cover Tape Material: Static Dissipative



| Dimension                           | Min                                                                                | Max   | Unit |
|-------------------------------------|------------------------------------------------------------------------------------|-------|------|
| A                                   |                                                                                    | 330   | mm   |
| B                                   | 1.5                                                                                |       | mm   |
| C                                   | 12.80                                                                              | 13.50 | mm   |
| D                                   | 20.2                                                                               |       | mm   |
| N                                   | 50                                                                                 |       | mm   |
| W <sub>1</sub><br>(measured at hub) | 12.4                                                                               | 14.4  | mm   |
| W <sub>2</sub><br>(measured at hub) |                                                                                    | 18.4  | mm   |
| Trailer                             | 160                                                                                |       | mm   |
| Leader                              | 390,<br>of which minimum 160<br>mm of empty carrier tape<br>sealed with cover tape |       | mm   |
| Weight                              |                                                                                    | 1500  | g    |

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**ORDERING INFORMATION**

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| Product Code  | Product                                            | Description                         | Capacitance Option              |
|---------------|----------------------------------------------------|-------------------------------------|---------------------------------|
| MAS9180A1TC00 | Single Band AM-Receiver IC with Differential Input | EWS-tested wafer, Thickness 400 µm. | C <sub>C</sub> = 0.75 pF        |
| MAS9180A5TC00 | Single Band AM-Receiver IC with Differential Input | EWS-tested wafer, Thickness 400 µm. | External compensation capacitor |
| MAS9180A1UA06 | Single Band AM-Receiver IC with Differential Input | TSSOP-16, Tape & Reel               | C <sub>C</sub> = 0.75 pF        |

Contact Micro Analog Systems Oy for other wafer thickness options.

**Offered in North America by**

Evox Rifa, Inc.  
300 Tri-State International, Suite 375  
Lincolnshire, IL 60069 USA  
Tel: 1 847 948 9511  
Fax: 1 847 948 9320  
Email: [service@evoxrifa.com](mailto:service@evoxrifa.com)  
Web: [http://www.evoxrifa.com/n\\_america](http://www.evoxrifa.com/n_america)

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**MICRO ANALOG SYSTEMS OY CONTACTS**

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