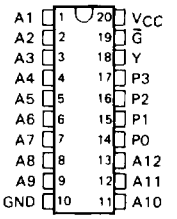
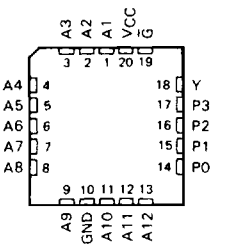
D2833, MARCH 1984 – REVISED JUNE 1989

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC679 . . . J PACKAGE
SN74HC679 . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC679 . . . FK PACKAGE
(TOP VIEW)



description

The 'HC679 address comparator simplifies addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied tothe 12-A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

The 'HC679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs.

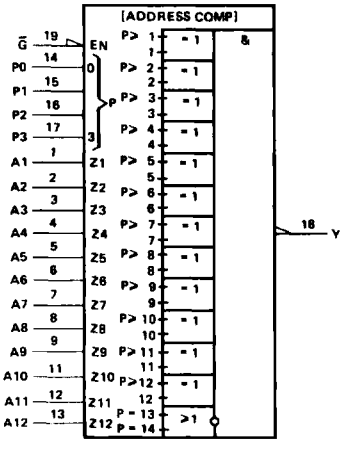
The 'HC679 is functionally unilaterally interchangeable with its TTL ALS counterpart, 'ALS679 in all cases of normal use as 12-bit address comparators. They differ in two respects. First, they may be programmed to recognize all A inputs low either by connecting all P inputs high (1111 = decimal 15), or by combination HHLL (1100 = 12), the latter option not being valid for the TTL ALS parts. Second, the combinations HHLH and HHHL (1101 = 13 and 1110 = 14) cannot be used (but are not needed) in address-comparator applications. These two combinations cause the outputs to be disabled (high).

The SN54HC679 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC679 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

$\overline{G}$	INPUTS																OUTPUT
	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	All other combinations																H
H	Any combination																H

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

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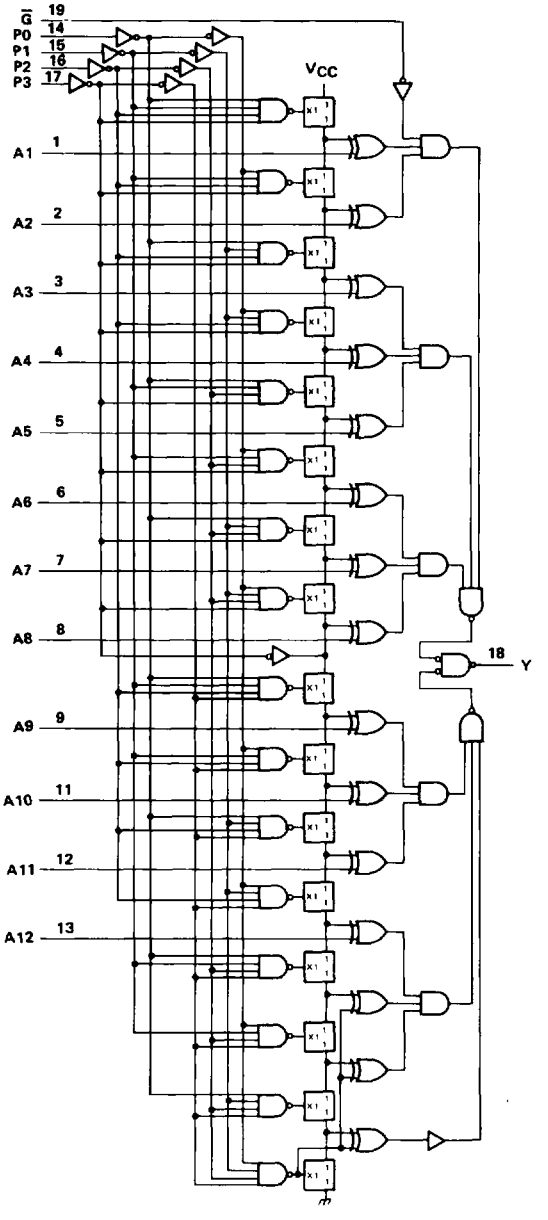
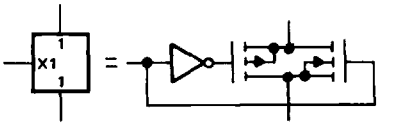
'logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

In order to understand the implementation of this device, it is essential that the function of the vertical string of transmission gates be understood. A schematic of one of these gates is shown below. If the input to the transmission gate labeled "X1" is high, then the transmission path between the two ports labeled "1" is on. If the "X1" input is low, then the transmission path between the two ports labeled "1" is off. Only one of the 16 transmission gates can be off while the device is operating; which one is off is determined by inputs P0 through P3. The lines going from the string of transmission gates to the Exclusive-OR gates located above the transmission gate that is off will be high. The lines going to the Exclusive-OR gates located below that transmission gate will be low.



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC679			SN74HC679			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°			SN54HC679		SN74HC679		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC679		SN74HC679		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Any P	Y	2 V		185	300		450		375	ns
			4.5 V		37	60		90		75	
			6 V		31	51		76		64	
t_{pd}	Any A	Y	2 V		105	160		240		200	ns
			4.5 V		21	32		48		40	
			6 V		18	27		41		34	
t_{pd}	$\overline{G}$	Y	2 V		75	125		187		156	ns
			4.5 V		15	25		37		31	
			6 V		13	21		31		26	
t_t		Y	2 V		38	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	40 pF typ

TYPICAL APPLICATION INFORMATION

The 'HC679 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made.

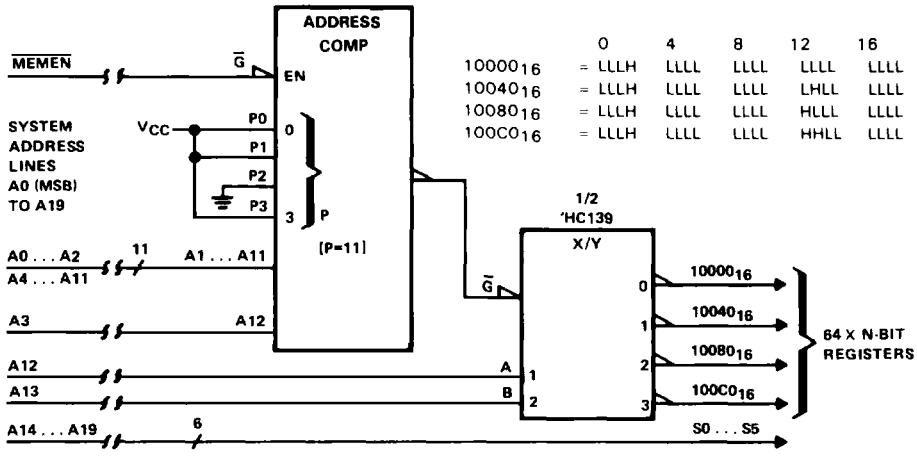
P3 to 0 V, P2 to V_{CC}, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.



REGISTER BANK DECODER

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