DDC
ILC DATA DEVICE CORPORATION®

SDC-14610/15 SERIES

THREE CHANNEL 14- AND 16-BIT TRACKING S/D CONVERTERS

DESCRIPTION

The SDC-14610/15 Series are small low cost triple synchro- or resolver-to-digital converters. The SDC-14610 Series is fixed at 14 bits, the SDC-14615 at 16 bits. The three channels are independent tracking types but share digital output pins and a common reference.

The velocity output (VEL) from the SDC-14610/15 Series, which can be used to replace a tachometer, is a 4 V signal referenced to ground with a linearity of 1% of output voltage.

A $\overline{\text{BIT}}$ output is optional and is a logic line that indicates LOS (Loss Of Signal) or excessive converter error. Due to pin limitations this option will exclude the velocity output.

SDC-14610/15 Series converters are available with operating temperature ranges of 0°C to +70°C and -55°C to +125°C, and MIL-PRF-38534 processing is available.

APPLICATIONS

With its low cost, small size, high accuracy, and versatile performance, the SDC-14610/15 Series converters are ideal for use in modern high-performance military and industrial position control systems. Typical applications include radar antenna positioning, navigation and fire control systems, motor control, and robotics.

FEATURES

- ***Fixed 14- or 16-Bit Resolution***
- ***Small Size 36-Pin DDIP Package***
- ***Three Independent Converters***
- ***Low Cost***
- ***Velocity Output Eliminates Tachometer***
- ***Optional $\overline{\text{BIT}}$ Output***
- ***High Reliability Single Chip Monolithic***
- ***-55°C to +125°C Operating Temperature Range***
- ***MIL-PRF-38534 Processing Available***

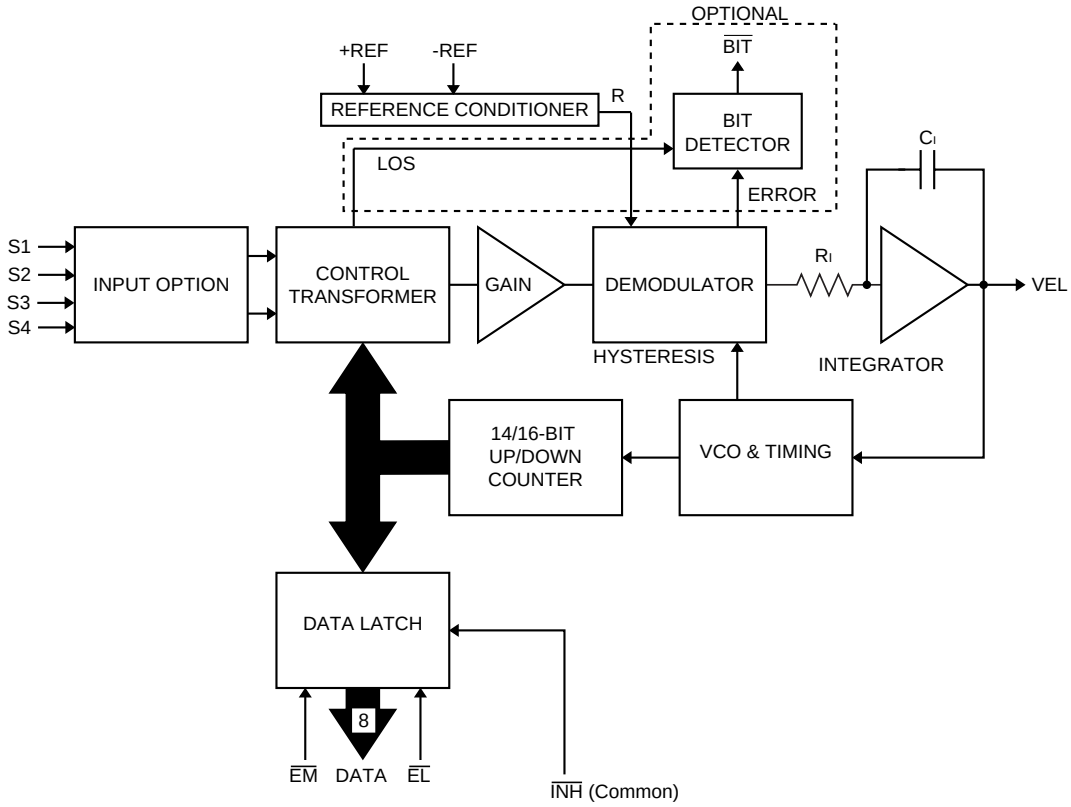


FIGURE 1. SDC-14610/15 BLOCK DIAGRAM (ONE CHANNEL)

TABLE 1. SDC-14610/15 SPECIFICATIONS (EACH CHANNEL)

These specs apply over the rated power supply, temperature, and reference frequency ranges; 10% signal amplitude variation, and 10% harmonic distortion. **Each Channel unless stated otherwise.**

PARAMETER	UNIT	VALUE	
RESOLUTION	Bits	14	16
ACCURACY	Min	4 + 1 LSB	2(4) + 1 LSB
REPEATABILITY	LSB	1 max	
DIFFERENTIAL LINEARITY	LSB	1 max	
REFERENCE INPUT		(+REF, -REF), **Common to All Channels**	
Type		differential	
		2 & 11.8 V UNITS	**90 V unit**
Voltage Range	Vrms	2-35	10-130
Frequency	Hz	360-5000	see note
Input Impedance			
single ended	Ohm	60k	270k min
differential	Ohm	120k	540k min
Common Mode Range	Vpeak	50, 100 transient	200 300 transient
SIGNAL INPUT CHARACTERISTICS		**Each Channel**	
90 V Synchro Input (L-L)			
Zin line-to-line	Ohm	123k	
Zin line-to-ground	Ohm	80k	
Common Mode Voltage	V	180 max	
11.8 V Synchro Input (L-L)			
Zin line-to-line	Ohm	52k	
Zin line-to-ground	Ohm	34k	
Common Mode Voltage	V	30 max	
11.8 V Resolver Input (L-L)			
Zin line-to-line	Ohm	140k	
Zin line-to-ground	Ohm	70k	
Common Mode Voltage	V	30 max	
2 V Direct Input (L-L)			
Voltage Range	Vrms	2 nom, 2.3 max	
Max Voltage No Damage	V	25 cont, 100 pk transient	
Input Impedance	Ohm	20 M//10 pF min	
DIGITAL INPUT/OUTPUT			
Logic Type		TTL/CMOS compatible	
Inputs		Logic 0 = 0.8 V max. Logic 1 = 2.0 V min. Loading =10 µa max P.U. current source to +5 V //5 pF max. CMOS transient protected	
		Each Channel	
Inhibit ($\overline{INH}$)(common)		Logic 0 inhibits; Data stable within 0.5 µs	
Enable Bits 1 to 8 ($\overline{EM}$)		Logic 0 enables; Data stable within 150 ns	
Enable Bits 9 to 14(16) ($\overline{EL}$)		Logic 1 = High Impedance Data High Z within 100 ns	
Outputs		**Common to All Channels**	
Parallel Data [1-14(16)]	bits	8 parallel lines; 2 bytes natural binary angle, positive logic	

TABLE 1. SDC 14610/15 SPECIFICATIONS (CONTINUED)

PARAMETER	UNIT	VALUE			
DIGITAL INPUT/OUTPUT					
OUTPUTS (continued)					
Built-In-Test (BIT)(Optional)		Logic 0 = BIT condition ±100 LSBs of error with a filter of 500 µs or LOS.			
		Each Channel			
Drive Capability	TTL	50 pF + Logic 0; 1 TTL load, 1.6 mA at 0.4 V max Logic 1; 10 TTL loads, -0.4 mA at 2.8 V min			
	CMOS	Logic 0; 100 mV max driving Logic 1; +5 V supply minus 100 mV min driving			
DYNAMIC CHARACTERISTICS Each Channel		**Device Type**			
		60 Hz		**4000 Hz**	
Input Frequency	Hz	47-5 k		360-5 k	
Bandwidth(Closed Loop)	Hz	15		103	
Ka	$1/s^2$	830		53k	
A1	1/s	0.17		1.33	
A2	1/s	5k		40k	
A	1/s	29		230	
B	1/s	14.5		115	
Resolution	bits	14	16	14	16
Tracking Rate					
typical	rps	1.25	0.31	10	2.5
minimum	rps	1	0.25	8	2
Acceleration (1 LSB lag)	deg/s^2	18	4.5	1160	290
Settling Time (179° step max)	msec	1100	2500	140	320
VELOCITY CHARACTERISTICS		**Each Channel**			
Polarity		Positive for increasing angle			
Voltage Range(Full Scale)	±V	4.5 typ,4 min			
Voltage Scaling	rps/FS	10			
Scale Factor	±%	10 typ	20 max		
Scale Factor TC	ppm/°C	100 typ	200 max		
Reversal Error	±%	1 typ	2 max		
Linearity	±%	0.5 typ	1 max		
Zero Offset	mV	5 typ	10 max		
Zero Offset TC	µV/°C	15 typ	30 max		
Load	kOhm		20 max		
Noise	(Vp/V)%	1 typ	2 max		
POWER SUPPLIES		**Total Device**			
Nominal Voltage	V	+5	-5		
Voltage Range	±%	5	10		
Max Volt. w/o Damage	V	+7	-7		
Current (Ea.)	mA	36 typ, 51 max			
TEMPERATURE RANGE					
Operating					
-30X	°C	0 to +70			
-10X	°C	-55 to +125			
Storage	°C	-65 to +150			
PHYSICAL CHARACTERISTICS					
Size	in	1.70 x 0.78 x 0.21			
	(mm)	(43.2 x 19.8 x 5.3)			
Weight	oz	0.66			

Note: 47 - 5k for 90 V, 60 Hz; 360 - 5k for 90 V, 400 Hz

THEORY OF OPERATION

The SDC-14610/15 Series of converters are based upon a single chip CMOS custom monolithic. They are implemented using the latest IC technology which merges precision analog circuitry with digital logic to form a complete high performance tracking resolver-to-digital converter.

FIGURE 1 is the Functional Block Diagram of SDC-14610/15 Series. The converter operates with ±5 V dc power supplies. Analog signals are referenced to analog ground, which is at ground potential. The converter is made up of three main sections; an input front-end, a converter, and a digital interface. The converter front-end differs for synchro, resolver and direct inputs. An electronic Scott-T is used for synchro inputs, a resolver conditioner for resolver inputs and a sine and cosine voltage follower for direct inputs. These amplifiers feed the high accuracy Control Transformer (CT). Its other input is the 14-bit digital angle ϕ. Its output is an analog error angle, or difference angle, between the two inputs. The CT performs the ratiometric trigonometric computation of $SIN\theta COS\phi - COS\theta SIN\phi = SIN(\theta - \phi)$ using amplifiers, switches, logic and capacitors in precision ratios.

The converter accuracy is limited by the precision of the computing elements in the CT. In these converters ratioed capacitors are used in the CT, instead of the more conventional precision ratioed resistors. Capacitors used as computing elements with op-amps need to be sampled to eliminate voltage drifting. Therefore, the circuits are sampled at a high rate to eliminate this drifting and at the same time to cancel out the op-amp offsets.

The error processing is performed using the industry standard technique for type II tracking R/D converters. The dc error is integrated yielding a velocity voltage which in turn drives a voltage controlled oscillator (VCO). This VCO is an incremental integrator (constant voltage input to position rate output) which together with the velocity integrator forms a type II servo feedback loop. A lead in the frequency response is introduced to stabilize the loop and another lag at higher frequency is introduced to reduce the gain and ripple at the carrier frequency and above.

TRANSFER FUNCTION AND BODE PLOT

The dynamic performance of the converter can be determined from its functional block diagram and its bode plots (open and closed loop); these are shown in FIGUREs 1 and 2 respectively.

The open loop transfer function is as follows:

$$\text{Open Loop Transfer Function} = \frac{A^2\left(\frac{S}{B}+1\right)}{S^2\left(\frac{S}{10B}+1\right)}$$

where A is the gain coefficient

and B is the frequency of lead compensation

The components of gain coefficient are error gradient, integrator gain, and VCO gain. These can be broken down as follows:

- Error Gradient = 0.011 volts per LSB (CT+Error Amp+Demod)

- Integrator gain = $\frac{1}{R_iC_i}$ volts per second per volt

- VCO Gain = $\frac{1}{1.25\ R_vC_v}$ LSBs per second per volt

GENERAL SETUP CONSIDERATIONS

The following recommendations should be considered when connecting the SDC-14610/15 Series converters:

1) Power supplies are ±5 V dc. For lowest noise performance it is recommended that a 0.1 µF or larger cap be connected from each supply to ground near the converter package.

2) Direct inputs are referenced to A GND.

INHIBIT AND ENABLE TIMING

The Inhibit ($\overline{INH}$) signal is used to freeze the digital output angle in the transparent output data latch while data is being transferred. Application of an Inhibit signal does not interfere with the continuous tracking of the converter. As shown in FIGURE 3, angular output data is valid 500 nanoseconds maximum after the application of the low-going inhibit pulse.

Output angle data is enabled onto the tri-state data bus in six bytes. The Enable MSB ($\overline{EM\ A}$,$\overline{EM\ B}$, or $\overline{EM\ C}$) is used for the most significant 8 bits and Enable LSB ($\overline{EL\ A}$, $\overline{EL\ B}$, or $\overline{EL\ C}$) is used for the least significant bits. As shown in FIGURE 4, output data is valid 150 nanoseconds maximum after the application of a low-going enable pulse. The tri-state data bus returns to the high impedance state 100 nanoseconds maximum after the rising edge of the enable signal.

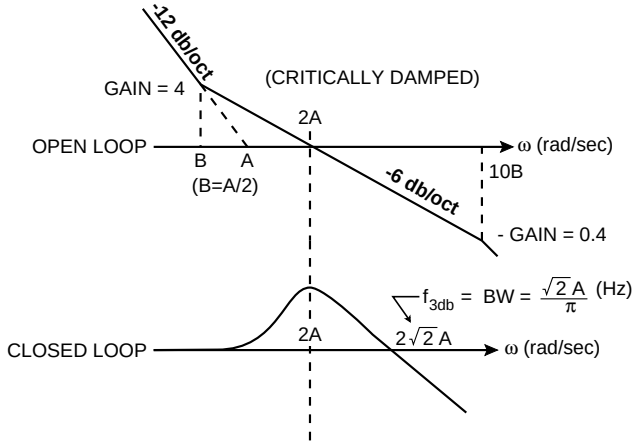


FIGURE 2. BODE PLOTS

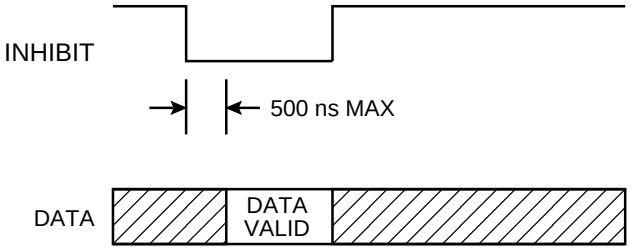


FIGURE 3. INHIBIT TIMING

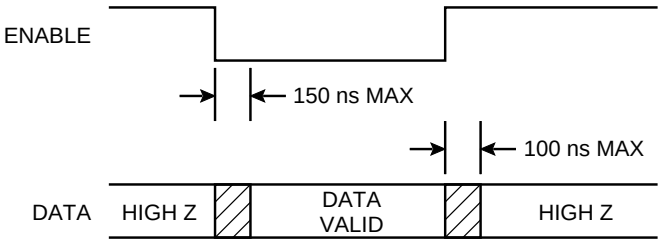
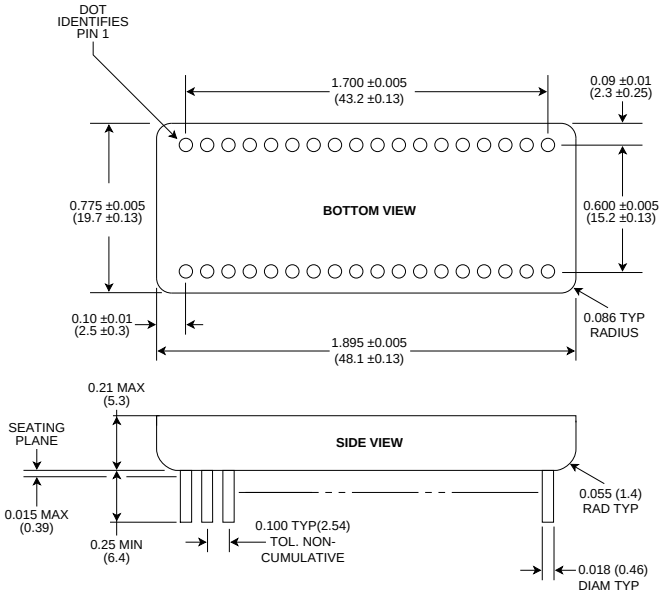


FIGURE 4. ENABLE TIMING



Notes:
1. Dimensions are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead clusters shall be centered within ±0.01 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.
5. Case is electrically floating.

FIGURE 5. SDC-14610/15 MECHANICAL OUTLINE

$\overline{\text{BIT}}$, BUILT-IN-TEST (OPTIONAL)

This output is a logic line that will flag an internal fault condition, or LOS (Loss-Of-Signal). The internal fault detector monitors the internal error and, when it exceeds ±100 LSBs, will set the line to a logic 0; this condition will occur during a large-step input and will reset to a logic 1 after the converter settles out. (The error voltage is filtered with a 500 µs filter) $\overline{\text{BIT}}$ will set for an overvelocity condition because the converter loop can't maintain input/output sync. $\overline{\text{BIT}}$ will also be set if a total LOS (loss of all signals) occurs.

NO FALSE 180° HANGUP

This feature eliminates the "false 180° reading" during instantaneous 180° step changes; this condition most often occurs when the input is "electronically switched" from a digital-to-synchro converter. If the "MSB" (or 180° bit) is "toggled" on and off, a converter without the "false 180° hangup" feature may fail to respond.

The condition is artificial, as a "real" synchro or resolver can not change its output 180° instantaneously. The condition is most often noticed during wraparound verification tests, simulations, or troubleshooting.

TABLE 2. PINOUTS (36 PIN)*

1	S1A(S)	S1A(R)	N.C.	36	VEL A (Velocity Output)**
2	S2A(S)	S2A(R)	+COSA(D)	36	$\overline{\text{EM A}}$ (Enable MSBs)
3	S3A(S)	S3A(R)	+SINA(D)	34	$\overline{\text{EL A}}$ (Enable LSBs)
4	N.C.	S4A(R)	N.C.	33	$\overline{\text{INH}}$ (Inhibit)
5	GND (Ground)			32	VEL B (Velocity Output)**
6	A GND (Analog Ground)			31	$\overline{\text{EM B}}$ (Enable MSBs)
7	S1B(S)	S1B(R)	N.C.	30	$\overline{\text{EL B}}$ (Enable LSBs)
8	S2B(S)	S2B(R)	+COSB(D)	29	Bit 8/Bit 16***
9	S3B(S)	S3B(R)	+SINB(D)	28	Bit 7/Bit 15***
10	N.C.	S4B(R)	N.C.	27	Bit 6/Bit 14
11	-5 V (Power Supply)			26	Bit 5/Bit 13
12	+5 V (Power Supply)			25	Bit 4/Bit 12
13	S1C(S)	S1C(R)	N.C.	24	Bit 3/Bit 11
14	S2C(S)	S2C(R)	+COSC(D)	23	Bit 2/Bit 10
15	S3C(S)	S3C(R)	+SINC(D)	22	Bit 1/Bit 9
16	N.C.	S4C(R)	N.C.	21	VEL C (Velocity Output)**
17	-REF (-Reference Input)			20	$\overline{\text{EL C}}$ (Enable LSBs)
18	+REF (+Reference Input)			19	$\overline{\text{EM C}}$ (Enable MSBs)

Notes: * (S) = Synchro; (R) = Resolver; (D) = 2 V Resolver Direct
** Replaced with BIT - "T" option.
*** Note: SDC-14615 Series only

ORDERING INFORMATION

SD-1461XT-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

Accuracy:
- 2 = ±4 + 1 LSB
- 4 = ±2 minutes + 1 LSB (Not available with 14-bit units.)

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Output Option:
- Blank = Standard Velocity Output (VEL)
- T = Built-In-Test Output, instead of VEL

Input Option:
- 0 = 11.8 V, Synchro, 14 bit, 400 Hz
- 1 = 11.8 V, Resolver, 14 bit, 400 Hz
- 2 = 90 V, Synchro, 14 bit, 400 Hz
- 3 = 2 V, Direct, 14 bit, 400 Hz
- 4 = 90 V, Synchro, 14 bit, 60 Hz
- 5 = 11.8 V, Synchro, 16 bit, 400 Hz
- 6 = 11.8 V, Resolver, 16 bit, 400 Hz
- 7 = 90 V, Synchro, 16 bit, 400 Hz
- 8 = 2 V, Direct 16 bit, 400 Hz
- 9 = 90 V, Synchro, 16 bit, 60 Hz

*Standard DDC Processing with burn-in and full temperature test—see table below.

STANDARD DDC PROCESSING		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

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