TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

Overview

The Direct Rambus DRAM™ (Direct RDRAM™) is a general-purpose high performance memory device suitable for use in a broad range of applications including computer memory, graphics, video and any other applications where high bandwidth and low latency are required.

The 288-Mbit Direct Rambus DRAMs (RDRAMs) are extremely high-speed CMOS DRAMs that are organized as 16M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600-MHz to 800-MHz transfer rates while still using conventional system and board design technologies. Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10 ns per 16 bytes).

The architecture of Direct RDRAMs allows the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAM's thirty-two banks can support up to four simultaneous transactions.

System-oriented features for mobile, graphics and large memory systems include power management, byte masking and ×18 organization. The two data bits in the ×18 organization can be used either for additional storage and bandwidth or for error correction.

Features

- Highest sustained bandwidth of any DRAM device:
  - 1.6 GB/s sustained data transfer rate
  - Separate control and data buses for maximized efficiency
  - Separate row and column control buses for easy scheduling and maximum performance
  - 32 banks: four transaction can take place simultaneously at full-bandwidth data rates

- Low latency features:
  - Write buffer to reduce read latency
  - Three precharge mechanisms for controller flexibility
  - Interleaved transactions

- Advanced power management:
  - Multiple low power states allows flexibility in power consumption versus time to transition to active state
  - Power-down Self-Refresh

- Uses Rambus Signaling Levels (RSL) for operation at up to 800 MHz.

- Organization: 2-Kbyte pages, and 32 banks ×18
  - ×18 organization allows ECC configurations or increased storage/bandwidth
  - Inter leaved Device Mode (IDM) for enhanced system reliability.

Note: Direct Rambus DRAM and Direct RDRAM are trademarks of Rambus Inc.

The 288-Mbit RDRAM is offered in a CSP horizontal package suitable for desktop as well as low-profile add-in card and mobile applications.

Direct RDRAMs operate from a 2.5 volt supply.

Key Timing Parameters/Part Numbers

Organization[a]	I/O Freg. (MHz)	Core Access Time (ns)	Part Number
512K ×18 ×32s	600	53	TC59RM818MB-6
512K ×18 ×32s	711	50	TC59RM818MB-7
512K ×18 ×32s	800	45	TC59RM818MB-8

a. The “32s” designation indicates that this RDRAM core is composed of 32 banks which use a “split” bank architecture.

PIN OUT and Definition (Top View)

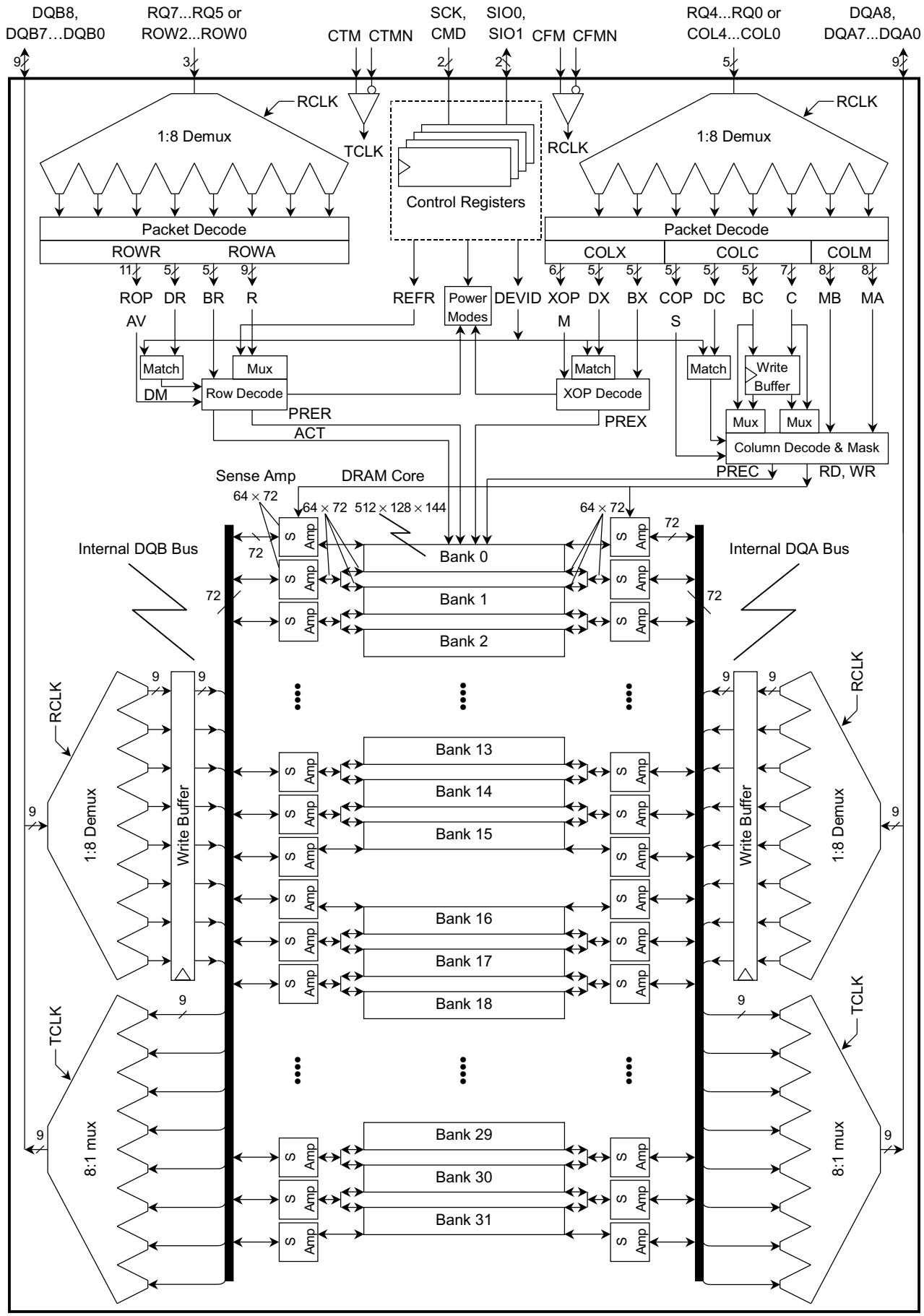
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	
10	—	V_{DD}	GND	—	V_{DD}	GND	V_{DD}	—	—	—	—	V_{DD}	V_{DD}	V_{DD}	—	GND	V_{DD}	—	10
9	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	9
8	GND	V_{DD}	CMD	V_{DD}	GND	GNDa	GNDa	V_{DD}	V_{DD}	GND	GND	V_{DD}	V_{DD}	GND	GND	V_{CMOS}	V_{DD}	GND	8
7	V_{DD}	DQA8	DQA7	DQA5	DQA3	DQA1	CTMN	CTM	RQ7	RQ5	RQ3	RQ1	DQB1	DQB3	DQB5	DQB7	DQB8	V_{DD}	7
6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	6
5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	5
4	GND	GND	DQA6	DQA4	DQA2	DQA0	CFM	CFMN	RQ6	RQ4	RQ2	RQ0	DQB0	DQB2	DQB4	DQB6	GND	GND	4
3	V_{DD}	GND	SCK	V_{CMOS}	GND	V_{DD}	GND	V_{DD}a	VREF	GND	V_{DD}	GND	GND	V_{DD}	SIO0	SIO1	GND	V_{DD}	3
2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	2
1	—	V_{DD}	GND	—	GND	V_{DD}	GND	—	—	—	—	GND	GND	GND	—	GND	V_{DD}	—	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	S	T	U	

Figure 1. TC59RM818MB(P-TFBGA92-1018-0.80AZ)

Table 1. Pin Descriptions

SIGNAL	I/O	TYPE	DESCRIPTION
SIO1, SIO0	I/O	CMOS	Serial input/output. Pins for reading from and writing to the control registers using a serial access protocol. Also used for power management.
CMD	I	CMOS	Command input. Pins used in conjunction with SIO0 and SIO1 for reading from and writing to the control register. Also used for power management.
SCK	I	CMOS	Serial clock input. Clock source used for reading from and writing to the control registers.
VDD			Supply voltage for the RDRAM core and interface logic.
VDDa			Supply voltage for the RDRAM analog circuitry.
VCMOS			Supply voltage for the CMOS input/output pins.
GND			Ground reference for RDRAM core and interface.
GNDa			Ground reference for RDRAM analog circuitry.
DQA8…DQA0	I/O	RSL	Data byte A. Nine pins which carry a byte of read or write data between the Channel and the RDRAM. DQA8 is not used by RDRAMs with a ×16 organization.
CFM	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CFMN	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
VREF			Logic threshold reference voltage for RSL signals.
CTMN	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
CTM	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RQ7…RQ5 or ROW2…ROW0	I	RSL	Row access control. Three pins containing control and address information for row accesses.
RQ4…RQ0 or COL4…COL0	I	RSL	Column access control. Five pins containing control and address information for column accesses.
DQB8…DQB0	I/O	RSL	Data byte B. Nine pins which carry a byte of read or write data between the Channel and the RDRAM.

Figure 2. 288-Mbit Direct RDRAM Block Diagram



General Description

Figure 2 is a block diagram of the 288-Mbit Direct RDRAM. It consists of two major blocks: a "core" block built from banks and sense amps similar to those found in other types of DRAM, and a Direct Rambus interface block which permits an external controller to access this core at up to 1.6 GB/s.

Control Registers:

The CMD, SCK, SIO0 and SIO1 pins appear in the upper center of the Figure 2. They are used to write and read a block of control registers. These registers supply RDRAM configuration information to a controller and they select the operating modes of the device. The 9-bit REFR value is used for tracking the last refreshed row. Most importantly, the 5-bit DEVID value specifies the device address of the RDRAM on the Channel.

Clocking:

The CTM and CTMN (Clock-to-Master) pins generate TCLK (Transmit Clock), the internal clock signal used to transmit read data. The CFM and CFMN (Clock-from-Master) pins generate RCLK (Receive Clock), the internal clock signal used to receive write data and receiving the ROW and COL pins.

DQA, DQB Pins:

These 18 pins carry read (Q) and write (D) data across the Channel. They are multiplexed/de-multiplexed from/to two 72-bit data paths (running at one-eighth the data frequency) inside the RDRAM.

Banks:

The 32-Mbyte core of the RDRAM is divided into 32 1-Mbyte banks, each organized as 512 rows, with each row containing 128 dualocts and each dualoct containing 16 bytes. A dualoct is the smallest unit of data which can be addressed.

Sense Amps:

The RDRAM contains two sets of 17 sense amps. Each sense amp consists of 1024 bytes of fast storage and can hold one-half of one row of one bank of the RDRAM. The sense amp may hold any of the 512 half-rows of an associated bank. However, each sense amp is shared between two adjacent banks of the RDRAM (except for sense amp numbers 0, 15, 16 and 31). This introduces the restriction that adjacent banks may not be simultaneously accessed.

RQ Pins:

These pins carry control and address information. They are divided into two groups. RQ7…RQ5 also called ROW2…ROW0, and are used primarily for controlling row accesses. RQ4…RQ0 also called COL4…COL0, and are used primarily for controlling column accesses.

ROW Pins:

The principle use of these three pins is to manage the transfer of data between the banks and the sense amps of the RDRAM. These pins are demultiplexed into a 24-bit ROWA (row-activate) or ROWR (row-operation) packet.

COL Pins:

The principle use of these five pins is to manage the transfer of data between the DQA/DQB pins and the RDRAM's sense amps. These pins are demultiplexed into a 23-bit COLC (column-operation) packet and either a 17-bit COLM (mask) packet or a 17-bit COLX (extended-operation) packet.

ACT Command:

An ACT (Active) command from a ROWA packet causes one of the 512 rows of the selected bank to be loaded into to its associated sense amps (two 512 byte sense amps for DQA and two for DQB).

PRER Command:

A PRER (Precharge) command from a ROWR packet causes the selected bank to release its two associated sense amps, permitting a different row in that bank to be activated, or permitting adjacent banks to be activated.

RD Command:

The RD (Read) command causes one of the 128 dualocts in one of the sense amps to be transmitted on the DQA/DQB pins of the Channel.

WR Command:

The WR (Write) command causes a dualoct received from the DQA/DQB data pins of the Channel to be loaded into the write buffer. There is also space in the write buffer for the BC bank address and C column address information. The data in the write buffer is automatically retired (written with optional byte mask) to one of the 128 dualocts of one of the sense amps during a subsequent COP command. A retire can take place during a RD or WR or NOCOP to another device, or during a WR or NOCOP to the same device. The write buffer will not retire during a RD operation to the same device. The write buffer reduces the delay needed for the internal DQA/DQB data path turn-around.

PREC Precharge:

The PREC, RDA and WRA commands are similar to NOCOP, RD and WR, except that a precharge operation is scheduled at the end of the data transfer. These command provide a second mechanism for performing precharge.

PREX Precharge:

After a RD command, or after a WR command with no byte masking (M = 0), a COLX packet may be used to specify an extended operation (XOP). The most important XOP command is PREX. This command provides a third mechanism for performing precharge.

Packet Format

Figure 3 shows the formats of the ROWA and ROWR packets on the ROW pins. Table 2 describes the fields which comprise these packets. The DR4T and DR4F bits are encoded to contain both the DR4 device address bit and a framing bit which allows the ROWA or ROWR packet to be recognized by the RDRAM.

The AV (ROWA/ROWR packet selection) bit distinguishes between the two packet types. Both the ROWA and ROWR packets provide a 5-bit device address and a 5-bit bank address. A ROWA packet uses the remaining bits to specify a 9-bit row address, and the ROWR packet uses the remaining bits for an 11-bit op-code field. Note the use of the "RsvX" notation to reserve bits for future extension of the address field.

Table 2. Field Description of ROWA and ROWR Packets

Field	Description
DR4T, DR4F	Bits for framing (recognizing) a ROWA or ROWR packet. Also encodes highest device address bit.
DR3…DR0	Device address for ROWA or ROWR packet.
BR4…BR0	Bank address for ROWA or ROWR packet. RsvB denotes bits ignored by the RDRAM.
AV	Selects between ROWA packet (AV = 1) or ROWR packet (AV = 0).
R8…R0	Row address for ROWA packet. RsvR denotes bits reserved for future row address extension.
ROP10…ROP0	Op-code field for ROWR packet. Specifies precharge, refresh, and power management functions.

Figure 3 also shows the formats of the COLC, COLM and COLX packets on the COL pins. Table 3 describes the fields which comprise these packets.

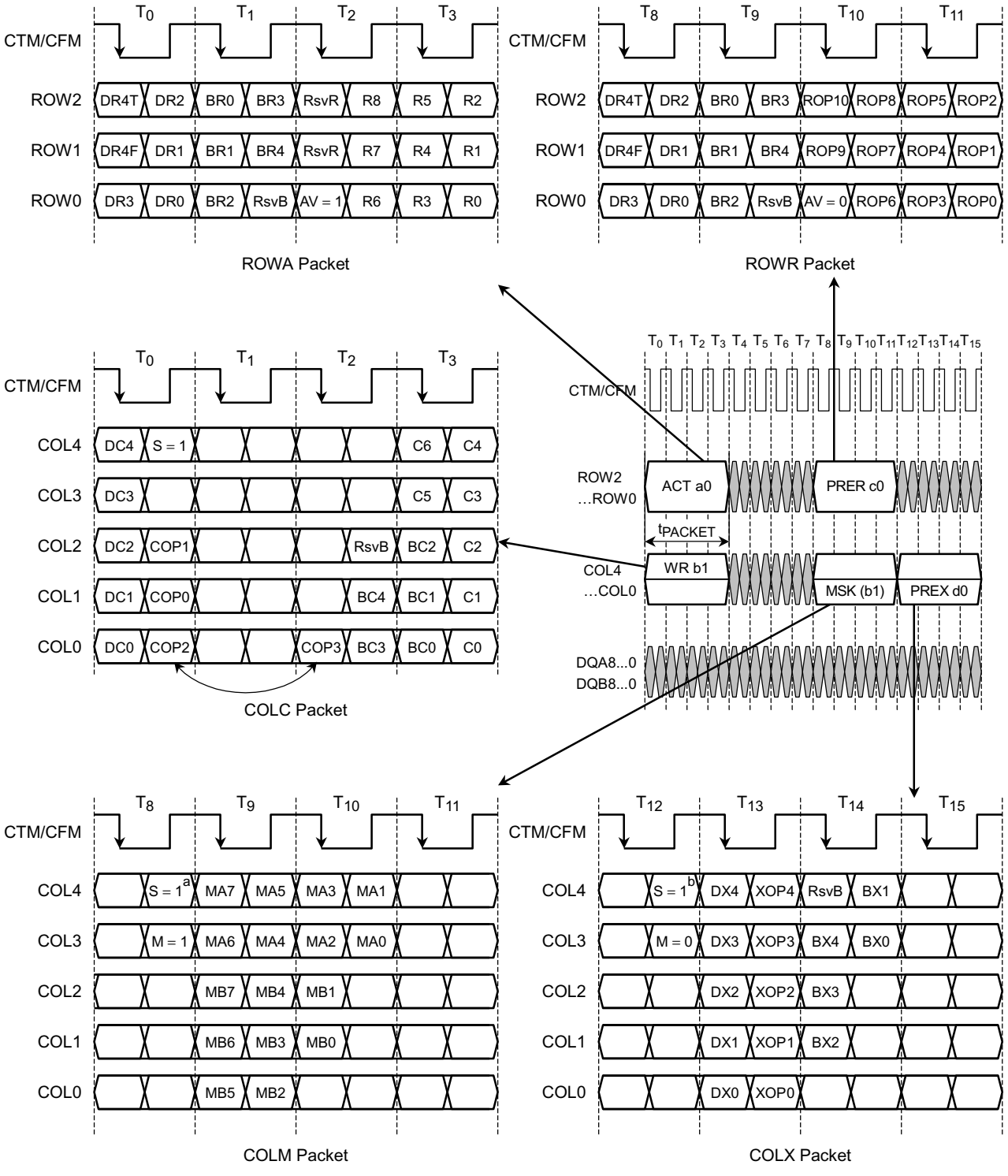
The COLC packet uses the S (Start) bit for framing. A COLM or COLX packet is aligned with this COLC packet, and is also framed by the S bit.

The 23-bit COLC packet has a 5-bit device address, a 5-bit bank address, a 7-bit column address and a 4-bit op-code. The COLC packet can specifies a Read or Write command, as well as some power management commands.

The remaining 17-bits are interpreted as a COLM (M = 1) or COLX (M = 0) packet. A COLM packet is used for a COLC Write command which needs byte mask control. The COLM packet is associated with the COLC packet from a time t_{RTR} earlier. A COLX packet may be used to specify an independent precharge command. It contains a 5-bit device address, a 5-bit bank address and a 5-bit op-code. The COLX packet may also be used to specify some housekeeping and power management commands. The COLX packet is framed within a COLC packet but is not otherwise associated with any other packet.

Table 3. Field Description for COLC Packet, COLM Packet and COLX Packet

Field	Description
S	Bit for framing (recognizing) a COLC packet and indirectly for framing a COLM or COLX packet.
DC4…DC0	Device address for COLC packet.
BC4…BC0	Bank address for COLC packet. RsvB denotes bits reserved for future extension (controller drives 0's).
C6…C0	Column address for COLC packet.
COP3…COP0	Op-code field for COLC packet. Specifies read, write, precharge, and power management functions.
M	Select between COLM packet (M = 1) or COLX packet (M = 0).
MA7…MA0	Byte mask write control bits. 1 = Write, 0 = No-Write. MA0 controls first byte on DQA8…0.
MB7…MB0	Byte mask write control bits. 1 = Write, 0 = No-Write. MB0 controls first byte on DQB8…0.
DX4…DX0	Device address for COLX packet.
BX4…BX0	Bank address for COLX packet. RsvB denotes bits reserved for future extension (controller drives 0's).
XOP4…XOP0	Op-code field for COLX packet. Specifies precharge, I_{OL} control, and power management functions.



a: The COLM is associated within a previous COLC, and is aligned within the present COLC, indicated by the Start bit (S = 1) position.

b: The COLM is aligned with the present COLC, indicated by the Start bit (S = 1) position.

Figure 3. Packet Formats

Field Encoding Summary

Table 4 shows how the six device address bits are decoded for the ROWA and ROWR packets. The DR4T and DR4F encoding merges a fifth device bit with a framing bit. When neither bit is asserted, the device is not selected. Note that a broadcast operation is indicated when both bits are set. Broadcast operation would typically be used for refresh and power management commands. If the device is selected, the DM (Device Match) signal is asserted and an ACT or ROP command is performed.

Table 4. Device Field Encodings for ROWA Packet and ROWR Packet

DR4T	DR4F	Selects One Device	Device Match Signal (DM)[a]
1	1	All devices (broadcast)	DM = 1
0	1	One device selected	DM = 1 if {DEVID4…DEVID0} = = {0, DR3…DR0} else DM = 0
1	0	One device selected	DM = 1 if {DEVID4…DEVID0} = = {1, DR3…DR0} else DM = 0
0	0	No devices selected	DM = 0

a. "/ =" means "not equal to", "= =" means "equal to".

Table 5 shows the encodings of the remaining fields of the ROWA and ROWR packets. An ROWA packet is specified by asserting the AV bit. This causes the specified row of the specified bank of this device to be loaded into the associated sense amps.

An ROWA packet is specified, when AV is not asserted. An 11-bit opcode field encodes a command for one of the banks of this device. The PRER command causes a bank and its two associated sense amps to precharge, so another row or an adjacent bank may be activated.

The REFA (Refresh-Activate) command is similar to the ACT command, except the row address comes from an internal register REFR, and REFR is incremented at the largest bank address. The REFP (Refresh-Precharge) command is identical to a PRER command.

The NAPR, NAPRC, PDNR, ATTN and RLXR commands are used for managing the power dissipation of the RDRAM and are described in more detail in "Power State Management" on page 46.

The TCEN and TCAL commands are used to adjust the output driver slew rate and they are described in more detail in "Current and Temperature Control" on page 53.

Table 5. ROWA Packet and ROWR Packet Field Encodings

DM[a]	AV	ROP10…ROP0 Field									Name	Description
		10	9	8	7	6	5	4	3	2:0		
0	—	—	—	—	—	—	—	—	—	—	—	No operation.
1	1	Row address									ACT	Activate row R8…R0 of bank BR4….BR0 of the device and move device to ATTN[b].
1	0	1	1	0	0	0	X[c]	X	X	000	PRER	Precharge bank BR4…BR0 of this device.
1	0	0	0	0	1	1	0	0	X	000	REFA	Refresh (activate) row REFR8…REFR0 of bank BR4…BR0 of device. Increment REFR if BR4…BR0 = 1111 (see Figure 37).
1	0	1	0	1	0	1	0	0	X	000	REFP	Precharge bank BR4…BR0 of the device after REFA (see Figure 37).
1	0	X	X	0	0	0	0	1	X	000	PDNR	Move this device into the Power Down (PDN) power state (see Figure 34).
1	0	X	X	0	0	0	1	0	X	000	NAPR	Move this device into the nap (NAP) power state (see Figure 34).
1	0	X	X	0	0	0	1	1	X	000	NAPRC	Move this device into the nap (NAP) power state conditionally.
1	0	X	X	X	X	X	X	X	0	000	ATTN[b]	Move this device into the attention (ATTN) power state (see Figure 32).
1	0	X	X	X	X	X	X	X	1	000	RLXR	Move this device into the standby (STBY) power state (see Figure 33).
1	0	0	0	0	0	0	0	0	X	001	TCAL	Temperature calibrate this device (see Figure 39).
1	0	0	0	0	0	0	0	0	X	010	TCEN	Temperature calibrate/enable this device (see Figure 39).
1	0	0	0	0	0	0	0	0	0	000	NOROP	No operation.

a. The DM (Device Match signal) value is determined by the DR4T, DR4F, DR3…DR0 field of the ROWA and ROWR packets. See Table 4.

b. The device's power state remains unchanged for a broadcast operation (DR4T/DR4F = 1/1).

c. An "X" entry indicates which commands may be combined. For instance, the three commands PRER/NAPRC/RLXR may be specified in one ROP value (011000111000).

Table 6 shows the COP field encoding. The device must be in the ATTN power state in order to receive COLC packets. The COLC packet is used primarily to specify RD (Read) and WR (Write) commands. Retire operations (moving data from the write buffer to a sense amp) happen automatically. See Figure 17 for a more detailed description.

The COLC packet can also specify a PREC command, which precharges a bank and its associated sense amps. The RDA/WRA commands are equivalent to combining RD/WR with a PERC. RLXC (Relax) performs a power mode transition. See "Power State Management" on page 46.

Table 6. COLC Packet Field Encodings

S	DC4…DC0 (selects one device) [a]	COP3	COP2	COP1	COP0	Command Name	Command Description
0	———————	—	—	—	—	—	No operation.
1	/ = (DEVID4…D EVID0)	—	—	—	—	—	Retire write buffer of the device.
1	= = (DEVID4…DEVID0)	X [b]	0	0	0	NOCOP	Retire write buffer of the device.
1	= = (DEVID4…DEVID0)	X	0	0	1	WR	Retire write buffer of the device, then write column C6…C0 of bank BC4…BC0 to the write buffer.
1	= = (DEVID4…DEVID0)	X	0	1	0	RSRV	Reserved, no operation.
1	= = (DEVID4…DEVID0)	X	0	1	1	RD	Read column C6…C0 of bank BC4…BC0 of the device.
1	= = (DEVID4…DEVID0)	X	1	0	0	PREC	Retire write buffer of the device, then precharge bank BC4…BC0.
1	= = (DEVID4…DEVID0)	X	1	0	1	WRA	Same as WR, but precharge bank BC4…BC0 after the write buffer (with new data) is retired.
1	= = (DEVID4…DEVID0)	X	1	1	0	RSRV	Reserved, no operation.
1	= = (DEVID4…DEVID0)	X	1	1	1	RDA	Same as RD, but precharge bank BC4…BC0 afterwards.
1	= = (DEVID4…DEVID0)	1	X	X	X	RLXC	Move this device into the standby (STBY) power state.

a. "/ =" means "not equal to", "= =" means "equal to".
b. An "x" entry indicates which commands may be combined. For instance, the two commands WR/RLXC may be specified in one COP value (1001).

Table 7 shows the COLM and COLX field encodings. The M bit is asserted to specify a COLM packet with two 8-bit byte mask fields MA and MB. If the M bit is not asserted, an COLX is specified.

It has device and bank address fields, and an opcode field. The primary use of a COLX packet is to permit an independent PREX (Precharge) command to be specified without consuming control bandwidth on the ROW pins. It is also used for the CAL (Calibrate) and SAM (Sample) current control commands (see "Current and Temperature Control" on page 53), and for the RLXX Power Mode command (see "Power State Management" on page 46).

Table 7. COLM Packet and COLX Packet Field Encodings

M	DX4…DX0 (selects one device) [a]	XOP4	XOP3	XOP2	XOP1	XOP0	Command Name	Command Description
1	———————	—	—	—	—	—	MSK	MB/MA bytemasks used by WR/WRA.
0	/ = (DEVID4…DEVID0)	—	—	—	—	—	—	No operation.
0	= = (DEVID4…DEVID0)	0	0	0	0	0	NOXOP	No operation.
0	= = (DEVID4…DEVID0)	1	X [b]	X	X	0	PREX	Precharge bank BX4…BX0 of the device.
0	= = (DEVID4…DEVID0)	X	1	X	X	0	CAL	Calibrate (drive) I_{OL} current for the device.
0	= = (DEVID4…DEVID0)	X	1	1	X	0	CAL/SAM	Calibrate (drive) and sample (update) I_{OL} current for the device.
0	= = (DEVID4…DEVID0)	X	X	X	1	0	RLXX	Move this device into the standby (STBY) power state.
0	= = (DEVID4…DEVID0)	X	X	X	X	1	RSRV	Reserved, no operation.

a. "/ =" means "not equal to", "= =" means "equal to".
b. An "x" entry indicates which commands may be combined. For instance, the two commands PREX/RLXX may be specified in one XOP value (10010).

DQ Packet Timing

Figure 4 shows the timing relationship of COLC packets with D and Q data packets. This document uses a specific convention for measuring time intervals between packets: all packets on the ROW and COL pins (ROWA, ROWR, COLC, COLM and COLX) use the trailing edge of the packet as a reference point, and all packets on the DQA/DQB pins (D and Q) use the leading edge of the packet as a reference point.

An RD or RDA command will transmit a dualoct of read data Q a time t_{CAC} later. This time includes one to five cycle of round-trip propagation delay on the Channel. The t_{CAC} parameter may be programmed to a one of a range of values (7, 8, 9, 10, 11, or 12 t_{CYCLE}). The value chosen depends upon the number of RDRAM devices on the Channel and the RDRAM timing bin. See Figure 30 for more information.

An WR or WRA command will receive a dualoct of write data D a time t_{CWD} later point. This time does not need to include the round-trip propagation time for the Channel since the COLC and D packets are traveling in the same direction.

When a Q packet follows a D packet (shown in the top of the figure), a gap ($t_{CAC} - t_{CWD}$) will automatically appear between them because the t_{CWD} value is always less than the t_{CAC} value. There will be no gap between the two COLC packets with the WR and RD commands which schedule the D and Q packets.

When a D packet follows a Q packet (shown in the bottom of the figure), no gap is needed between them because the t_{CWD} value is less than the t_{CAC} value. However, a gap of $t_{CAC} - t_{CWD}$ or greater must be inserted between the COLC packets with the RD and WR commands by the controller so the Q and D packets do not overlap.

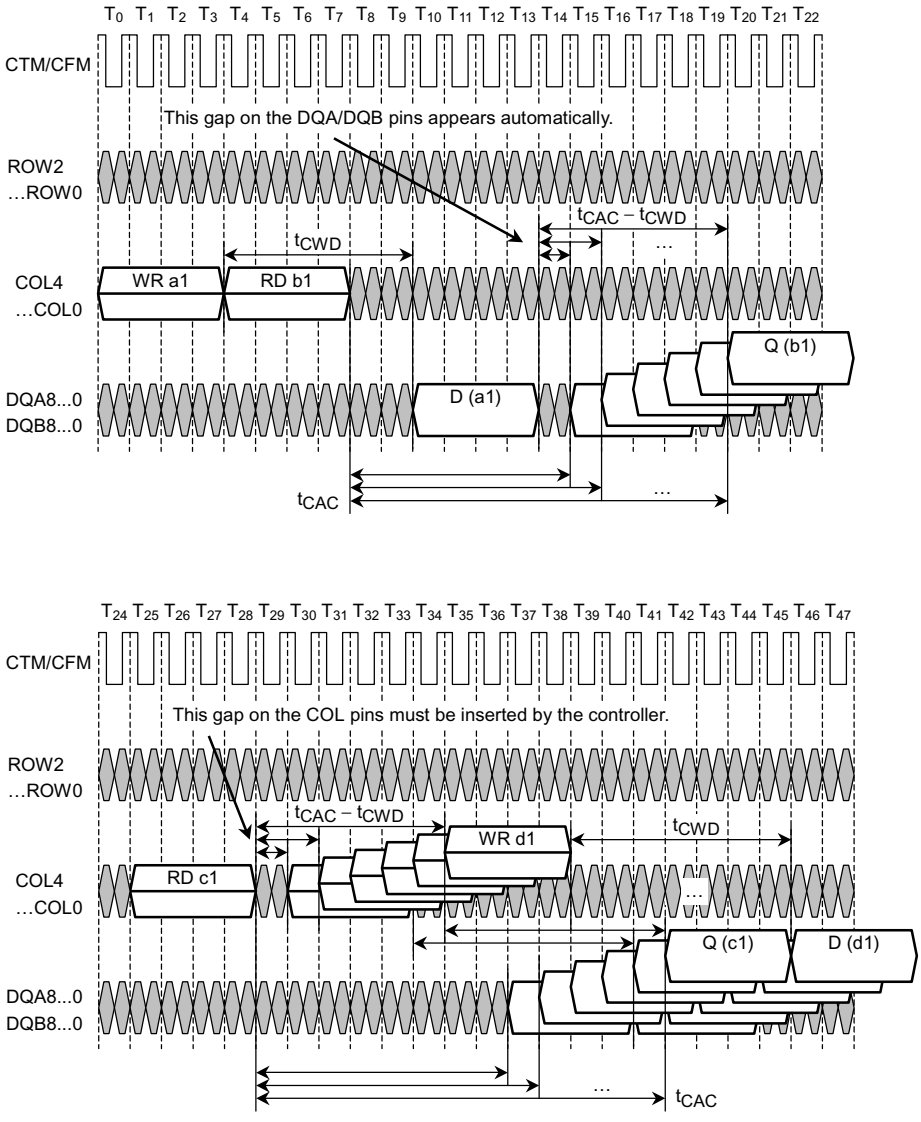


Figure 4. Read (Q) and Write (D) Data Packets-Timings for t_{CAC} = 7, 8, 9, 10, 11 or 12 t_{CYCLE}

COLM Packet to D Packet Mapping

Figure 5 shows a write operation initiated by a WR command in a COLC packet. If a subset of the 16 bytes of write data are to be written, then a COLM packet is transmitted on the COL pins a time t_{RTR} after the COLC packet containing the WR command. The M bit of the COLM packet is set to indicate that it contains the MA and MB mask fields. Note that this COLM packet is aligned with the COLC packet which causes the write buffer to be retired. See Figure 17 for more details.

If all 16 bytes of the D data packet are to be written, then no further control information is required. The packet slot which would have been used by the COLM packet (t_{RTR} after the COLC packet) is available to be used as an COLX packet. This could be used for a PREX precharge command or for a housekeeping command (this case is not shown). The M bit is not asserted in a COLX packet and causes all 16 bytes of the previous WR command to be written unconditionally. Note that a RD command will never need a COLM packet, and will always be able to use the COLX packet option (a read operation has no need for the byte-write-enable control bits).

Figure 5 also shows the mapping between the MA and MB fields of the COLM packet and the bytes of the D packet on the DQA and DQB pins. Each mask bit controls whether a byte of data is written (= 1) or not written (= 0).

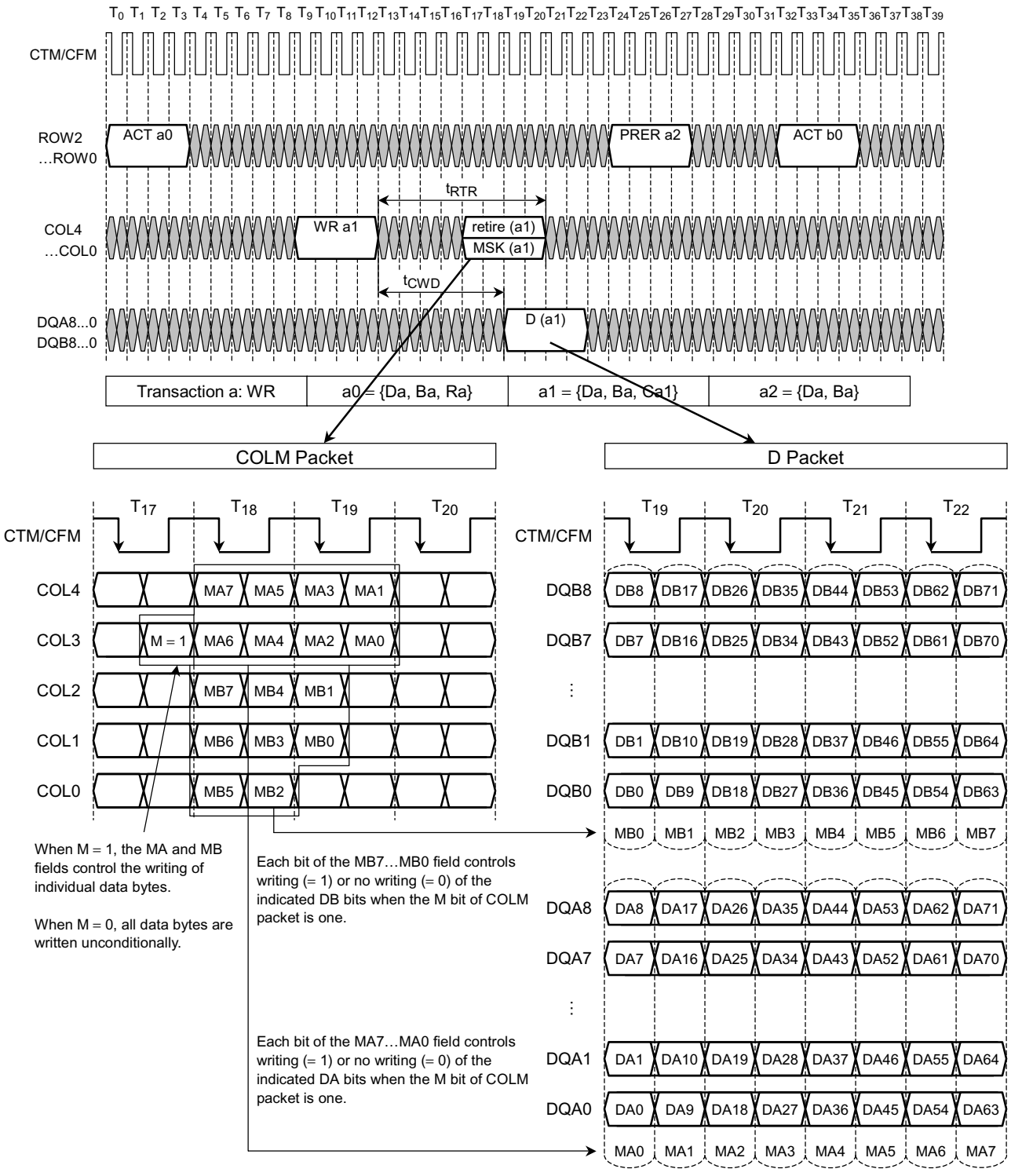
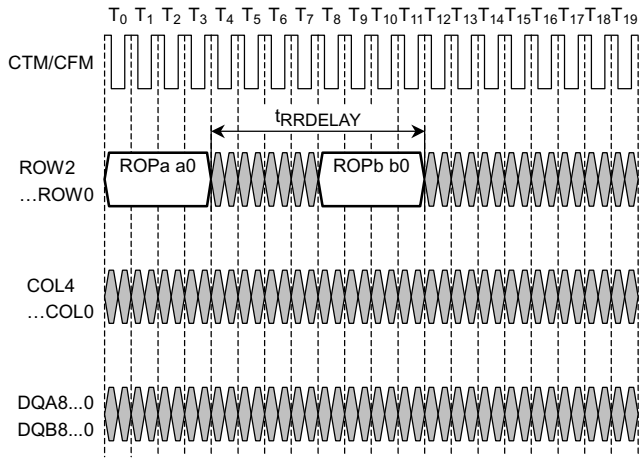


Figure 5. Mapping Between COLM Packet and D Packet for WR Command

ROW-to-ROW Packet Interaction



Transaction a: ROPa	a0 = {Da, Ba, Ra}
Transaction b: ROPb	b0 = {Db, Bb, Rb}

Figure 6. ROW-to-ROW Packet interaction-Timing

Figure 6 shows two packets on the ROW pins separated by an interval $t_{RRDELAY}$ which depends upon the packet contents. No other ROW packets are sent to banks {Ba, Ba + 1, Ba – 1} between packet "a" and packet "b" unless noted otherwise. Table 8 summarizes the $t_{RRDELAY}$ values for all possible cases.

Cases RR1 through RR4 show two successive ACT commands. In case RR1, there is no restriction since the ACT commands are to different devices. In case RR2 the t_{RR} restriction applies to the same device with non-adjacent banks. Cases RR3 and RR4 are illegal (as shown) since bank Ba needs to be precharged. If a PRER to Ba, Ba + 1, or Ba – 1 is inserted, $t_{RRDELAY}$ is t_{RC} (t_{RAS} to the PRER command, and t_{RP} to the next ACT).

Cases RR5 through RR8 show an ACT command followed by a PRER command. In cases RR5 and RR6, there are no restrictions since the commands are to different devices or to non-adjacent banks of the same device. In cases RR7 and RR8, the t_{RAS} restriction means the activated bank must wait before it can be precharged.

Cases RR9 through RR12 show a PRER command followed by an ACT command. In case RR9 and RR10, there are essentially no restrictions since the commands are to different devices or to non-adjacent banks of the same device. RR10a and RR10b depend upon whether a bracketed bank (Ba ± 1) is precharged or activated. In cases RR11 and RR12, the same and adjacent banks must all wait t_{RP} for the sense amp and bank to precharge before being activated.

Cases RR13 through RR16 summarize the combinations of two successive PRER commands. In case RR13 there is no restriction since two devices are addressed. In RR14, the t_{PP} applies, since the same device is addressed. In RR15 and RR16, the same bank or an adjacent bank may be given repeated PRER commands with only the t_{PP} restriction.

Two adjacent banks can't be activated simultaneously. A precharge command to one bank will thus affect the state of adjacent banks (and sense amps). If bank Ba is activated and a PRER is directed to Ba, then bank Ba will be precharged along with sense amps Ba – 1/Ba and Ba/Ba + 1. If bank Ba + 1 is activated and PRER is directed to Ba, then bank Ba + 1 will be precharged along with sense amps Ba/Ba + 1 and Ba + 1/ Ba + 2. If bank Ba – 1 is activated and a PRER is directed to Ba, then bank Ba – 1 will be precharged along with sense amps Ba/Ba – 1 and Ba – 1/ Ba – 2.

A ROW packet may contain commands other than ACT and PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, NAPRC, PDNR, RLXR, ATTN, TCAL, and TCEN commands are discussed in later sections.

Table 8. ROW-to-ROW Packet Interaction Rules

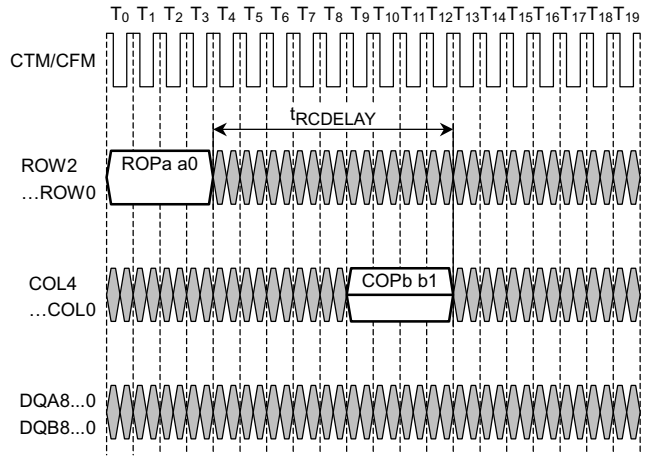
Case #	ROPa	Da	Ba	Ra	ROPb	Db	Bb	Rb	$t_{RRDELAY}$	Example
RR1	ACT	Da	Ba	Ra	ACT	/ = Da[a]	XXXX	X…X	t_{PACKET}	Figure 11
RR2	ACT	Da	Ba	Ra	ACT	= = Da	/ = {Ba, Ba + 1, Ba – 1}	X…X	t_{RR}	Figure 11
RR3	ACT	Da	Ba	Ra	ACT	= = Da	= = {Ba + 1, Ba – 1}	X…X	t_{RC} – illegal unless PRER to Ba/Ba + 1/Ba – 1	Figure 10
RR4	ACT	Da	Ba	Ra	ACT	= = Da	= = {Ba}	X…X	t_{RC} – illegal unless PRER to Ba/Ba + 1/Ba – 1	Figure 10
RR5	ACT	Da	Ba	Ra	PRER	/ = Da	XXXX	X…X	t_{PACKET}	Figure 11
RR6	ACT	Da	Ba	Ra	PRER	= = Da	/ = {Ba, Ba + 1, Ba – 1}	X…X	t_{PACKET}	Figure 11
RR7	ACT	Da	Ba	Ra	PRER	= = Da	= = {Ba + 1, Ba – 1}	X…X	t_{RAS}	Figure 10
RR8	ACT	Da	Ba	Ra	PRER	= = Da	= = {Ba}	X…X	t_{RAS}	Figure 15
RR9	PRER	Da	Ba	Ra	ACT	/ = Da	XXXX	X…X	t_{PACKET}	Figure 12
RR10	PRER	Da	Ba	Ra	ACT	= = Da	/ = {Ba, Ba ± 1, Ba ± 2}	X…X	t_{PACKET}	Figure 12
RR10a	PRER	Da	Ba	Ra	ACT	= = Da	= = {Ba + 2}	X…X	t_{PACKET}/t_{RP} – if Ba + 1 is precharged/ activated.	
RR10b	PRER	Da	Ba	Ra	ACT	= = Da	= = {Ba – 2}	X…X	t_{PACKET}/t_{RP} – if Ba – 1 is precharged/ activated.	
RR11	PRER	Da	Ba	Ra	ACT	= = Da	= = {Ba + 1, Ba – 1}	X…X	t_{RP}	Figure 10
RR12	PRER	Da	Ba	Ra	ACT	= = Da	= = {Ba}	X…X	t_{RP}	Figure 10
RR13	PRER	Da	Ba	Ra	PRER	/ = Da	XXXX	X…X	t_{PACKET}	Figure 12
RR14	PRER	Da	Ba	Ra	PRER	= = Da	/ = {Ba, Ba + 1, Ba – 1}	X…X	t_{PP}	Figure 12
RR15	PRER	Da	Ba	Ra	PRER	= = Da	= = {Ba + 1, Ba – 1}	X…X	t_{PP}	Figure 12
RR16	PRER	Da	Ba	Ra	PRER	= = Da	= = {Ba}	X…X	t_{PP}	Figure 12

a. "/ =" means "not equal to", "= =" means "equal to".

ROW-to-COL Packet Interaction

Figure 7 shows two packets on the ROW and COL pins. They must be separated by an interval $t_{RCDELAY}$ which depends upon the packet contents. Table 9 summarizes the $t_{RCDELAY}$ values for all possible cases. Note that if the COL packet is earlier than the ROW packet, it is considered a COL-to-ROW packet interaction.

Cases RC1 through RC5 summarize the rules when the ROW packet contains an ACT command. Figure 15 and Figure 16 show examples of RC5-an activation followed by a read or write. RC4 is an illegal situation, since a read or write of a precharged banks is being attempted (remember that for a bank to be activated, adjacent banks must be precharged). In cases RC1, RC2 and RC3, there is no interaction of the ROW and COL packets.



Transaction a: ROPa	a0 = {Da, Ba, Ra}
Transaction b: COPb	b1 = {Db, Bb, Cb1}

Figure 7. ROW-to-COL Packet Interaction Timing

Cases RC6 through RC9 summarize the rules when the ROW packet has a PRER command. There is either no interaction (RC6 through RC8), or an illegal situation with a read or write of a precharged bank (RC9).

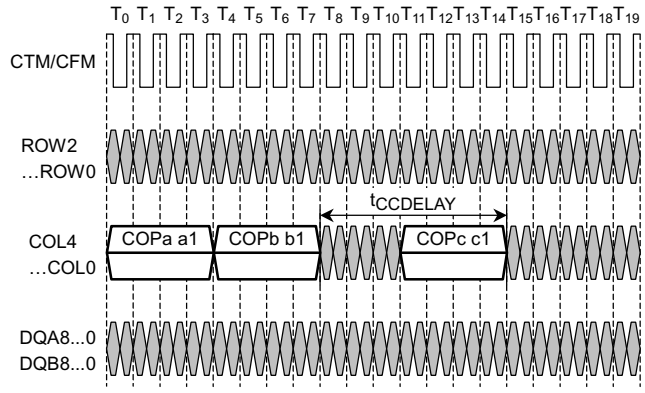
The COL pins can also schedule a precharge operation with a RDA, WRA or PREC command in a COLC packet or a PREX command in a COLX packet. The constraints of these precharge operations may be converted to equivalent PRER command constraints using the rules summarized in Figure 14.

Table 9. ROW-to-COL Packet Interaction Rules

Case #	ROPa	Da	Ba	Ra	COPb	Db	Bb	Cb1	$t_{RCDELAY}$	Example
RC1	ACT	Da	Ba	Ra	NOCOP, RD, retire	/ = Da[a]	XXXX	X…X	0	
RC2	ACT	Da	Ba	Ra	NOCOP	= = Da	XXXX	X…X	0	
RC3	ACT	Da	Ba	Ra	RD, retire	= = Da	/ = {Ba, Ba + 1, Ba – 1}	X…X	0	
RC4	ACT	Da	Ba	Ra	RD, retire	= = Da	= = {Ba + 1, Ba – 1}	X…X	Illegal	
RC5	ACT	Da	Ba	Ra	RD, retire	= = Da	= = Ba	X…X	t_{RCD}	Figure 15
RC6	PRER	Da	Ba	Ra	NOCOP, RD, retire	/ = Da	XXXX	X…X	0	
RC7	PRER	Da	Ba	Ra	NOCOP	= = Da	XXXX	X…X	0	
RC8	PRER	Da	Ba	Ra	RD, retire	= = Da	/ = {Ba, Ba + 1, Ba – 1}	X…X	0	
RC9	PRER	Da	Ba	Ra	RD, retire	= = Da	= = {Ba + 1, Ba – 1}	X…X	Illegal	

a. "/ =" means "not equal to", "= =" means "equal to".

COL-to-COL Packet Interaction



Transaction a: COPa	a1 = {Da, Ba, Ca1}
Transaction b: COPb	b1 = {Db, Bb, Cb1}
Transaction c: COPc	c1 = {Dc, Bc, Cc1}

Figure 8. COL-to-COL Packet Interaction Timing

Figure 8 shows three arbitrary packets on the COL pins. Packets "b" and "c" must be separated by an interval $t_{CCDELAY}$ which depends upon the command and address values in all three packets. Table 10 summarizes the $t_{CCDELAY}$ values for all possible cases.

Cases CC1 through CC5 summarize the rules for every situation other than the case when COPb is a WR command and COPc is a RD command. In CC3, when a RD command is followed by a WR command, a gap of $t_{CAC} - t_{CWD}$ must be inserted between the two COL packets. See Figure 4 for more explanation of why this gap is needed. For cases CC1, CC2, CC4, and CC5, there is no restriction ($t_{CCDELAY}$ is t_{CC}).

In case CC6 through CC10, COPb is a WR command and COPc is a RD command. The $t_{CCDELAY}$ value needed between these two packets depends upon the command and address in the packet with COPa. In particular, in case CC6 when there is WR-WR-RD command sequence directed to the same device, a gap will be needed between the packets with COPb and COPc. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place. Figure 18 (right) provides a more detailed explanation of this case.

In case CC10, there is a RD-WR-RD sequence directed to the same device. If a prior write to the same device is unretired when COPa is issued, then a gap will be needed between the packets with COPb and COPc as in case CC6. The gap will need a COLC packet with a NOCOP command directed to any device in order to force an automatic retire to take place.

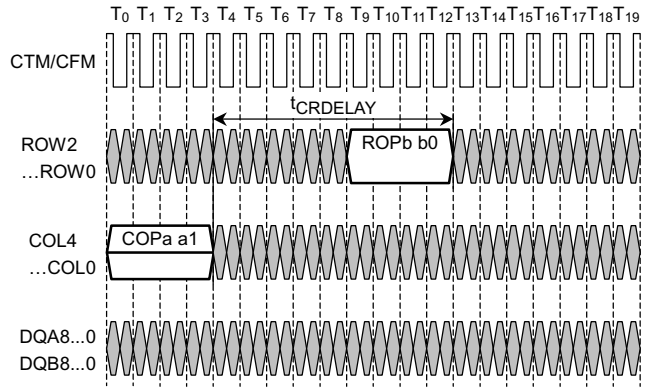
Cases CC7, CC8, and CC9 have no restriction ($t_{CCDELAY}$ is t_{CC}).

Table 10. COL-to-COL Packet Interaction Rules

Case #	COPa	Da[a]	Ba	Ca1	COPb	Db	Bb	Cb1	COPc	Dc[a]	Bc	Cc1	$t_{CCDELAY}$	Example
CC1	XXXX	XXXXX	X…X	X…X	NOCOP	Db	Bb	Cb1	XXXX	XXXXX	X…X	X…X	t_{CC}	
CC2	XXXX	XXXXX	X…X	X…X	RD, WR	Db	Bb	Cb1	NOCOP	XXXXX	X…X	X…X	t_{CC}	
CC3	XXXX	XXXXX	X…X	X…X	RD	Db	Bb	Cb1	WR	XXXXX	X…X	X…X	$t_{CC} + t_{CAC} - t_{CWD}$	Figure 4
CC4	XXXX	XXXXX	X…X	X…X	RD	Db	Bb	Cb1	RD	XXXXX	X…X	X…X	t_{CC}	Figure 15
CC5	XXXX	XXXXX	X…X	X…X	WR	Db	Bb	Cb1	WR	XXXXX	X…X	X…X	t_{CC}	Figure 16
CC6	WR	= = Db	X	X…X	WR	Db	Bb	Cb1	RD	= = Db	X…X	X…X	t_{RTR}	Figure 18
CC7	WR	= = Db	X	X…X	WR	Db	Bb	Cb1	RD	/ = Db	X…X	X…X	t_{CC}	
CC8	WR	/ = Db	X	X…X	WR	Db	Bb	Cb1	RD	= = Db	X…X	X…X	t_{CC}	
CC9	NOCOP	= = Db	X	X…X	WR	Db	Bb	Cb1	RD	= = Db	X…X	X…X	t_{CC}	
CC10	RD	= = Db	X	X…X	WR	Db	Bb	Cb1	RD	= = Db	X…X	X…X	t_{CC}	

a. "/ =" means "not equal to", "= =" means "equal to".

COL-to-ROW Packet Interaction



Transaction a: COPa	a1 = {Da, Ba, Ca1}
Transaction b: ROPb	b0 = {Db, Bb, Rb}

Figure 9. COL-to-ROW Packet Interaction Timing

Figure 9 shows arbitrary packets on the COL and ROW pins. They must be separated by an interval $t_{CRDELAY}$ which depends upon the command and address values in the packets. Table 11 summarizes the $t_{CRDELAY}$ value for all possible cases.

Cases CR1, CR2, CR3, and CR9 show no interaction between the COL and ROW packets, either because one of the commands is a NOP or because the packets are directed to different devices or to non-adjacent banks.

Case CR4 is illegal because an already-activated bank is to be re-activated without being precharged. Case CR5 is illegal because an adjacent bank can't be activated or precharged until bank Ba is precharged first.

In case CR6, the COLC packet contains a RD command, and the ROW packet contains a PRER command for the same bank. The t_{RDP} parameter specifies the required spacing. Likewise, in case CR7, the COLC packet causes an automatic retire to take place, and the ROW packet contains a PRER command for the same bank. The t_{RTP} parameter specifies the required spacing.

Case CR8 is labeled "Hazardous" because a WR command should always be followed by an automatic retire before a precharge is scheduled. Figure 19 shows an example of what can happen when the retire is not able to happen before the precharge.

For the purposes of analyzing COL-to-ROW interactions, the PREC, WRA, and RDA commands of the COLC packet are equivalent to the NOCOP, WR, and RD commands. These commands also cause a precharge operation to take place. This precharge may converted to an equivalent PRER command on the ROW pins using the rules summarized in Figure 14.

A ROW packet may contain commands other than ACT or PRER. The REFA and REFP commands are equivalent to ACT and PRER for interaction analysis purposes. The interaction rules of the NAPR, PDNR, and RLXR commands are discussed in a later section.

Table 11. COL-to-ROW Packet Interaction Rules

Case #	COPa	Da	Ba	Ca1	ROPb	Db[a]	Bb	Rb	$t_{CRDELAY}$	Example
CR1	NOCOP	Da	Ba	Ca1	X…X	XXXX	XXXX	X…X	0	
CR2	RD/WR	Da	Ba	Ca1	X…X	/ = Da	XXXX	X…X	0	
CR3	RD/WR	Da	Ba	Ca1	X…X	= = Da	/ = {Ba, Ba + 1, Ba – 1}	X…X	0	
CR4	RD/WR	Da	Ba	Ca1	ACT	= = Da	= = {Ba}	X…X	Illegal	
CR5	RD/WR	Da	Ba	Ca1	ACT	= = Da	= = {Ba + 1, Ba – 1}	X…X	Illegal	
CR6	RD	Da	Ba	Ca1	PRER	= = Da	= = {Ba, Ba + 1, Ba – 1}	X…X	t_{RDP}	Figure 15
CR7	retire[b]	Da	Ba	Ca1	PRER	= = Da	= = {Ba, Ba + 1, Ba – 1}	X…X	t_{RTP}	Figure 16
CR8	WR[c]	Da	Ba	Ca1	PRER	= = Da	= = {Ba, Ba + 1, Ba – 1}	X…X	0	Figure 19
CR9	XXXX	Da	Ba	Ca1	NOROP	XXXX	XXXX	X…X	0	

a. "/ =" means "not equal to", "= =" means "equal to".

b. This is any command which permits the write buffer of device Da to retire. "Ba" is the bank address in the write buffer.

c. This situation is hazardous because the write buffer will be left unretired while the targeted bank is precharged.

ROW-to-ROW Examples

Figure 10 shows examples of some of the ROW-to-ROW packet spacings from Table 8. A complete sequence of activate and precharge commands is directed to a bank. The RR8 and RR12 rules apply to this sequence. In addition to satisfying the t_{RAS} and t_{RP} timing parameters, the separation between ACT commands to the same bank must also satisfy the t_{RC} timing parameter (RR4).

When a bank is activated, it is necessary for adjacent banks to remain precharged. As a result, the adjacent banks will also satisfy parallel timing constraints; in the example the RR11 and RR3 rules are analogous to the RR12 and RR4 rules.

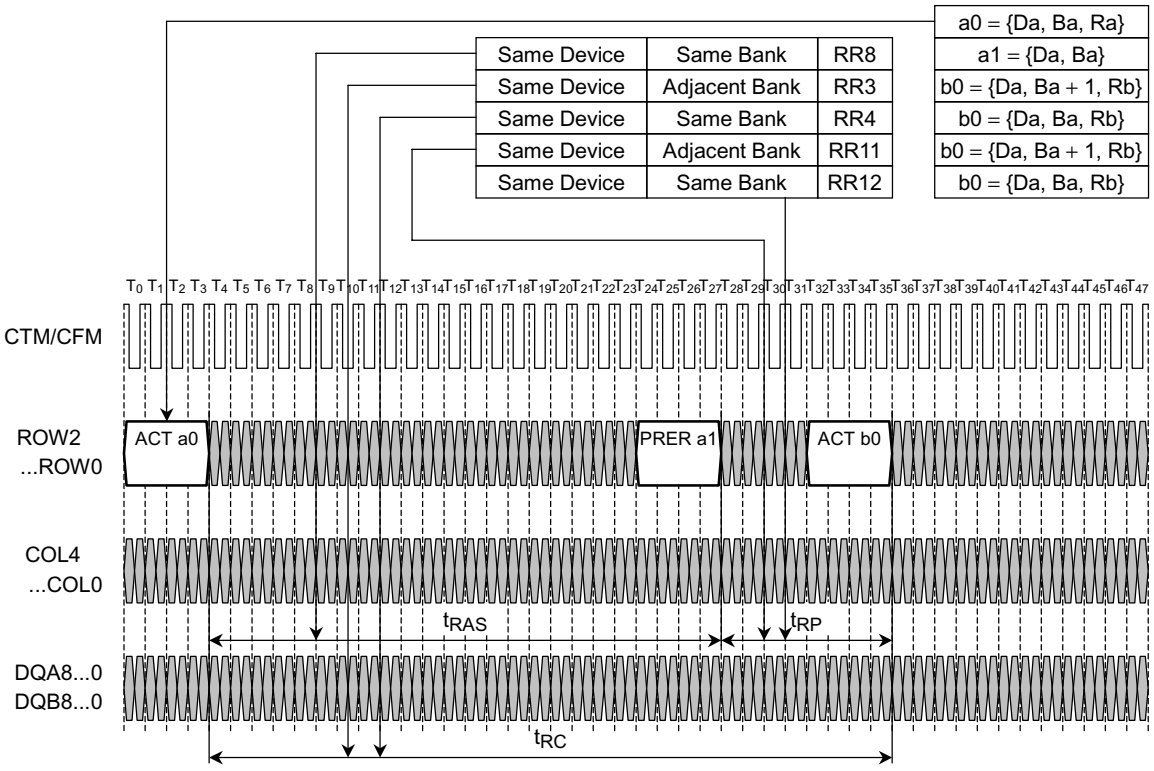


Figure 10. ROW Packet Example

Figure 11 shows examples of the ACT-to-ACT (RR1, RR2) and ACT-to-PRER (RR5, RR6) command spacings from Table 8. In general, the commands in ROW packets may be spaced an interval t_{PACKET} apart unless they are directed to the same or adjacent banks, or unless they are of a similar command type (both PRER or both ACT) and directed to the same device.

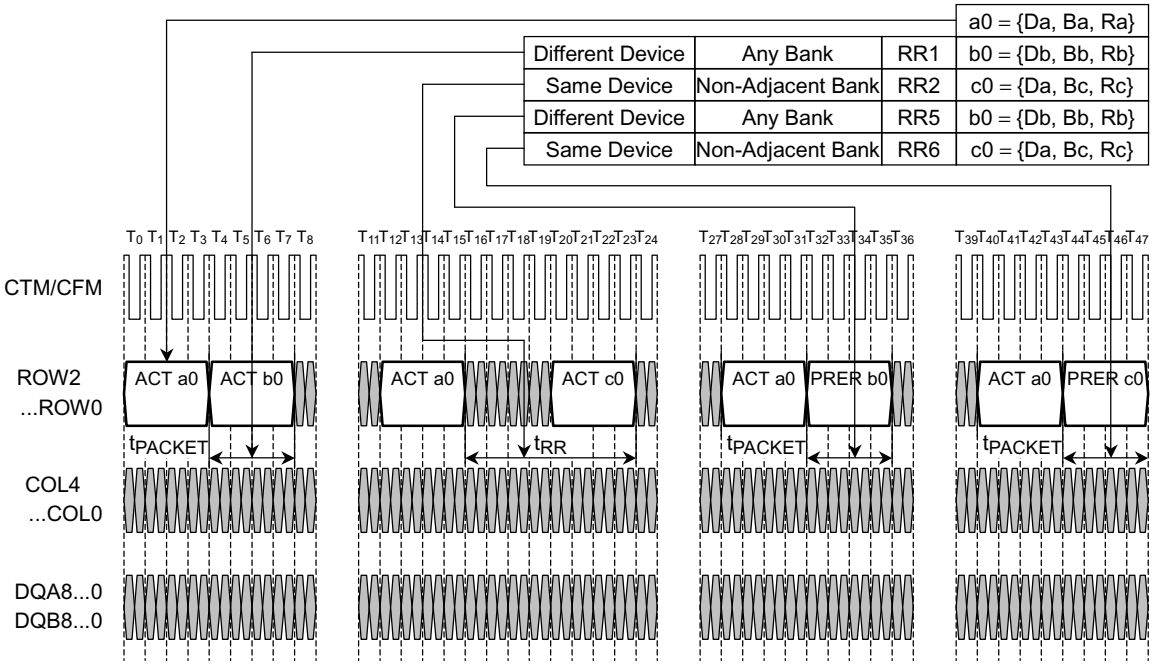


Figure 11. ROW Packet Examples

Figure 12 shows an example of the PRER-to-PRER (RR13, RR14) and PRER-to-ACT (RR9, RR10) command spacings from Table 8. The RR15 and RR16 cases (PRER-to-PRER to same or adjacent banks) are not shown, but are similar to RR14. In general, the commands in ROW packets may be spaced an interval t_{PACKET} apart unless they are directed to the same or adjacent banks, or unless they are of a similar command type (both PRER or both ACT) and directed to the same device.

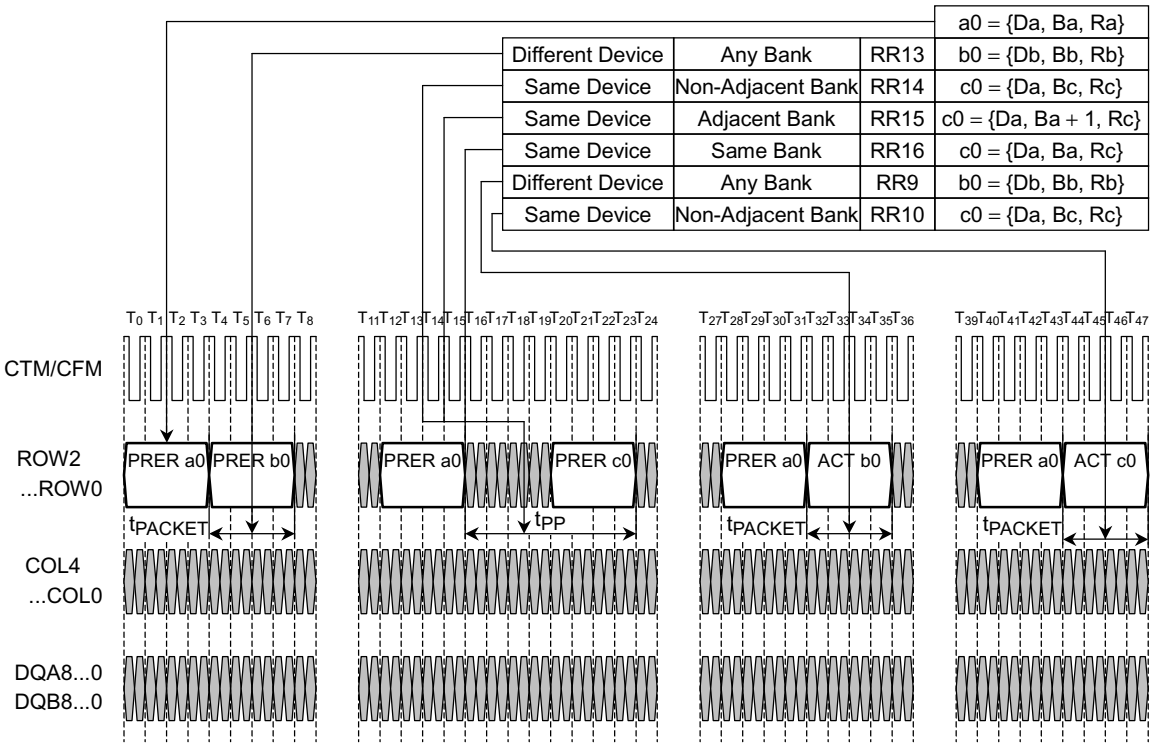


Figure 12. ROW Packet Examples

ROW and Column Cycle Description

Activate:

A row cycle begins with the activate (ACT) operation. The activation process is destructive; the act of sensing the value of a bit in a bank's storage cell transfers the bit to the sense amp, but leaves the original bit in the storage cell with an incorrect value.

Restore:

Because the activation process is destructive, a hidden operation called restore is automatically performed. The restore operation rewrites the bits in the sense amp back into the storage cells of the activated row of the bank.

Read/Write:

While the restore operation takes place, the sense amp may be read (RD) or written (WR) using column operations. If new data is written into the sense amp, it is automatically forwarded to the storage cells of the bank so that the data in the activated row and the data in the sense amp remain identical.

Precharge:

When both the restore operation and the column operations are completed, the sense amp and bank are precharged (PRE). This leaves them in the proper state to begin another activate operation.

Intervals:

The activate operation requires the interval $t_{RCD,MIN}$ to complete. The hidden restore operation requires the interval $t_{RAS,MIN} - t_{RCD,MIN}$ to complete. Column read and write operations are also performed during the $t_{RAS,MIN} - t_{RCD,MIN}$ interval (if more than about four column operations are performed, this interval must be increased). The precharge operation requires the interval $t_{RP,MIN}$ to complete.

Adjacent Banks:

A RDRAM with a "s" designation (512K ×32s ×18) indicates it contains "split banks". This means that the sense amps are shared between two adjacent banks. The only exception is that sense amp 0, 15, 16, 31 which are not shared. When a row in a bank is activated, the two adjacent sense amps are connected to (associated with) that bank and are not available for use by the two adjacent banks. These two adjacent banks must remain precharged while the selected bank goes through its activate, restore, read/write and precharge operations.

For example (referring to the block diagram of Figure 2), if bank 5 is accessed, sense amp 4/5 and sense amp 5/6 will both be loaded with one of the 512 rows (with 1024 bytes loaded into each sense amp from the 2K byte row-512 bytes to the DQA side and 512 bytes to the DQB side). While this row from bank 5 is being accessed, no rows may be accessed in banks 4 or 6 because of the sense amp sharing.

Precharge Mechanisms

Figure 13 shows an example of precharge using the ROWR packet mechanism. The PRER command must occur t_{RAS} after the ACT command and t_{RP} before the next ACT command. This timing will serve as a baseline against which the other precharge mechanisms can be compared.

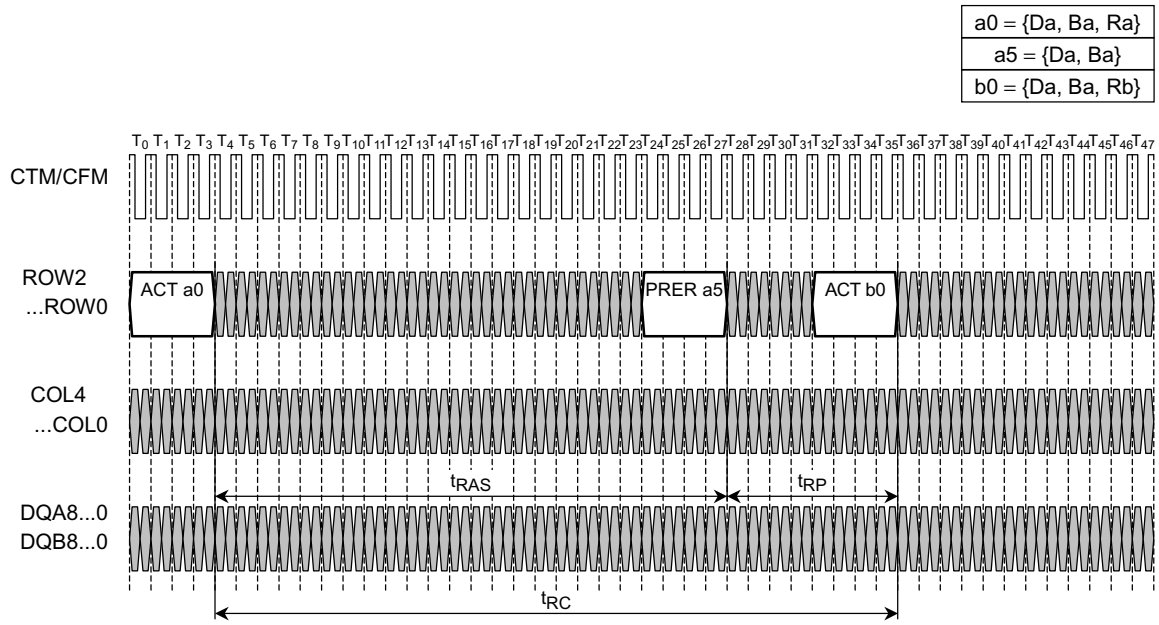


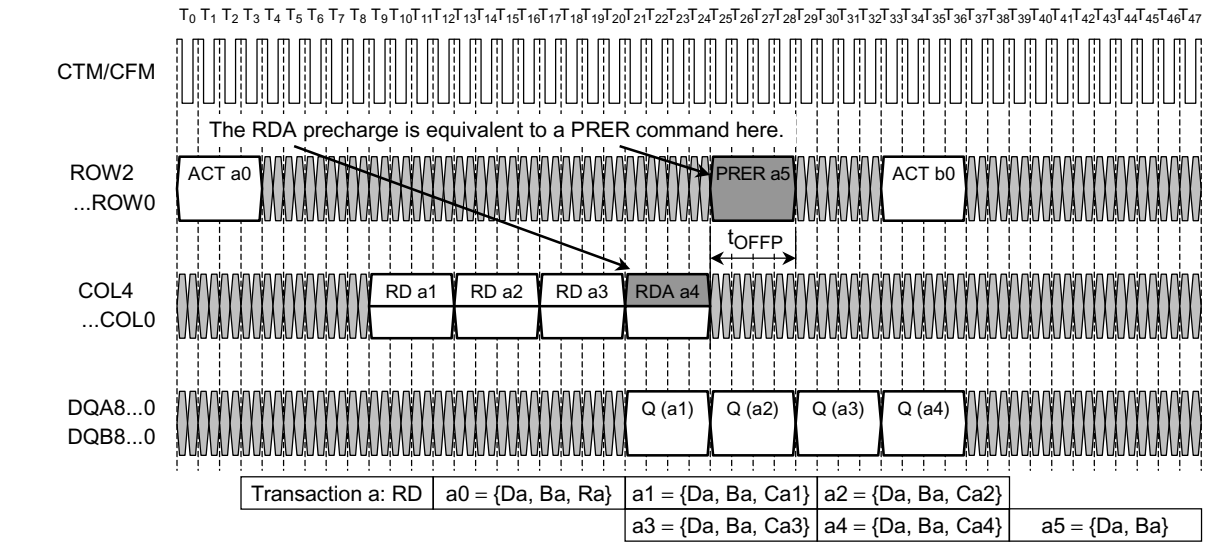
Figure 13. Precharge with PRER Command in ROWR Packet

Figure 14 (top) shows an example of precharge with a RDA command. A bank is activated with a ROWA packet on the ROW pins. Then, a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these commands is a RDA, which causes the bank to automatically precharge when the final Read has finished. The timing of this automatic precharge is equivalent to a PRER command in a ROWR packet on the ROW pins that is offset t_{OFFP} from the COLC packet with the RDA command. The RDA command should be treated as a RD command in a COLC packet as well as a simultaneous (but offset) PRER command in a ROWR packet when analyzing interactions with other packets.

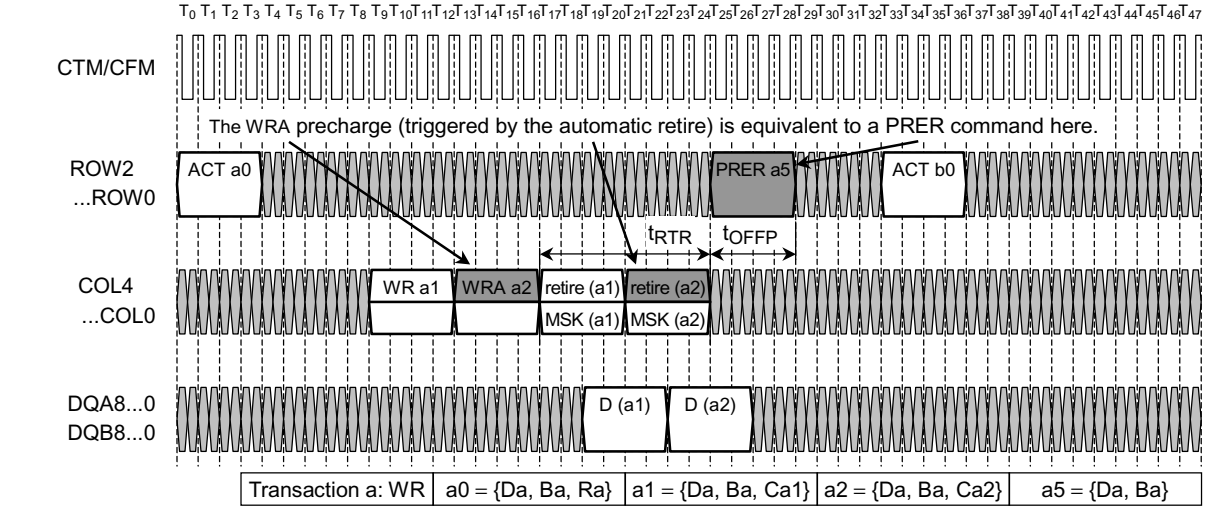
Figure 14 (middle) shows an example of precharge with a WRA command. As in the RDA example, a bank is activated with a ROWA packet on the ROW pins. Then, two dualocts are written with WR commands in COLC packets on the COL pins. The second of these commands is a WRA, which causes the bank to automatically precharge when the final write has been retired. The timing of this automatic precharge is equivalent to a PRER command in a ROWR packet on the ROW pins that is offset t_{OFFP} from the COLC packet that causes the automatic retire. The WRA command should be treated as a WR command in a COLC packet as well as a simultaneous (but offset) PRER command in a ROWR packet when analyzing interactions with other packets. Note that the automatic retire is triggered by a COLC packet t_{RTR} after the COLC packet with the WR command unless the second COLC contains a RD command to the same device. This is described in more detail in Figure 17.

Figure 14 (bottom) shows an example of precharge with a PREX command in a COLX packet. A bank is activated with a ROWA packet on the ROW pins. Then a series of four dualocts are read with RD commands in COLC packets on the COL pins. The fourth of these COLC packets includes a COLX packet with a PREX command. This causes the bank to precharge with timing equivalent to a PRER command in a ROWR packet on the ROW pins that is offset t_{OFFP} from the COLX packet containing the PREX command.

COLC Packet: RDA Precharge Offset



COLC Packet: WDA Precharge Offset



COLX Packet: PREX Precharge Offset

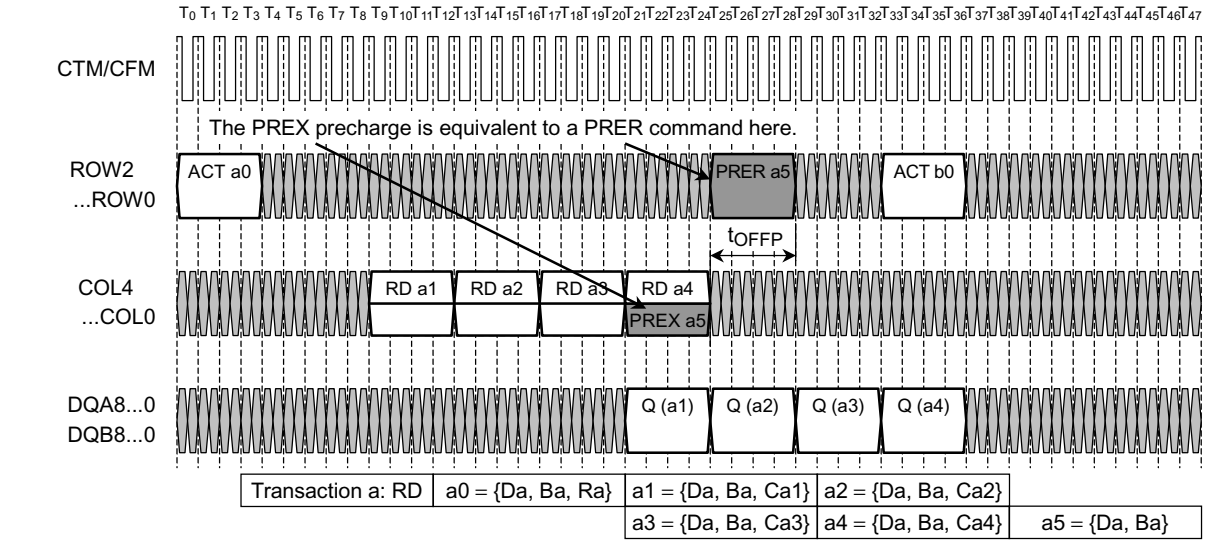


Figure 14. Offsets for Alternative Precharge Mechanisms

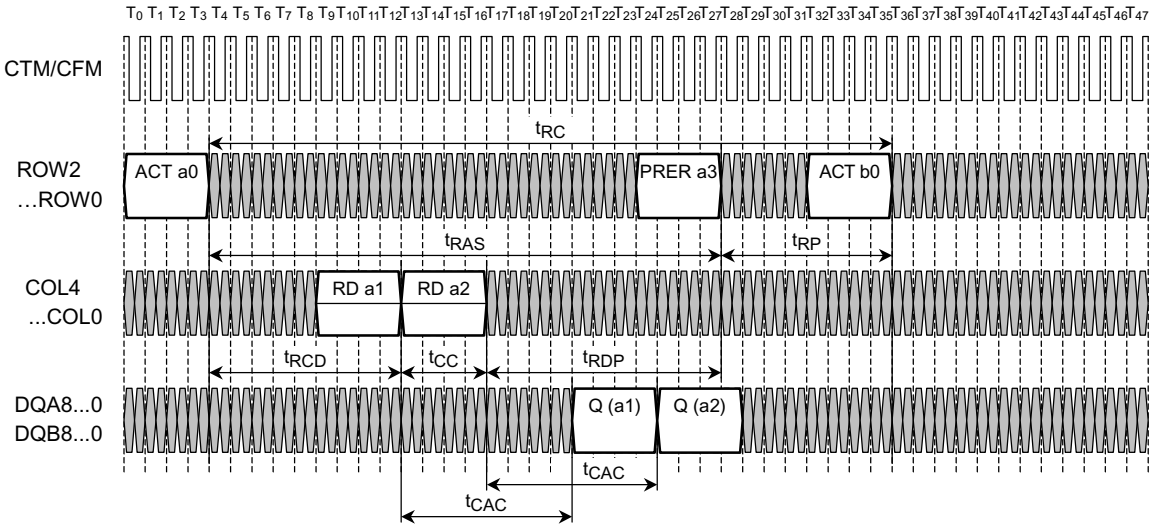
Read Transaction Example

Figure 15 shows an example of a read transaction. It begins by activating a bank with an ACT a0 command in a ROWA packet. A time t_{RCD} later a RD a1 command is issued in a COLC packet. Note that the ACT command includes the device, bank, and row address (abbreviated as a0) while the RD command includes device, bank, and column address (abbreviated as a1). A time t_{CAC} after the RD command the read data dualoct Q (a1) is returned by the device. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA/DQB pins use the beginning of the packet as a timing reference point.

A time t_{CC} after the first COLC packet on the COL pins a second COLC packet is issued. It contains a RD a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. t_{CAC} after the second RD command a second read data dualoct Q (a2) is returned by the device.

Next, a PRER a3 command is issued in a ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction or so that an adjacent bank may be activated. The a3 address includes the same device and bank address as the a0, a1 and a2 addresses. The PRER command must occur a time t_{RAS} or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the t_{RAS} interval). The PRER command must also occur t_{RDP} or more after the last RD command. Note that the t_{RDP} value shown is greater than $t_{RDP,MIN}$ specified in page 64. This transaction example reads two dualocts, but there is actually enough time to read three dualocts before t_{RDP} becomes the limiting parameter rather than t_{RAS}. If four dualocts were read, the packet with PRER would need to shift right (be delayed) by one t_{CYCLE} (note-this case is not shown).

Finally, an ACT b0 command is issued in a ROWR packet on the ROW pins. The second ACT command must occur t_{RC} or more after the first ACT command and a time t_{RP} or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be started until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.



Transaction a: RD	a0 = {Da, Ba, Ra}	a1 = {Da, Ba, Ca1}	a2 = {Da, Ba, Ca2}	a3 = {Da, Ba}
Transaction b: XX	b0 = {Da, Ba, Rb}			

Figure 15. Read Transaction Example

Write Transaction Example

Figure 16 shows an example of a write transaction. It begins by activating a bank with an ACT a0 command in a ROWA packet. A time $t_{RCD} - t_{RTR}$ later a WR a1 command is issued in a COLC packet (note that the t_{RCD} interval is measured to the end of the COLC packet with the first retire command). Note that the ACT command includes the device bank and row address (abbreviated as a0) while the WR command includes device, bank and column address (abbreviated as a1). A time t_{CWD} after the WR command the write data dualoct D (a1) is issued. Note that the packets on the ROW and COL pins use the end of the packet as a timing reference point, while the packets on the DQA/DQB pins use the beginning of the packet as a timing reference point.

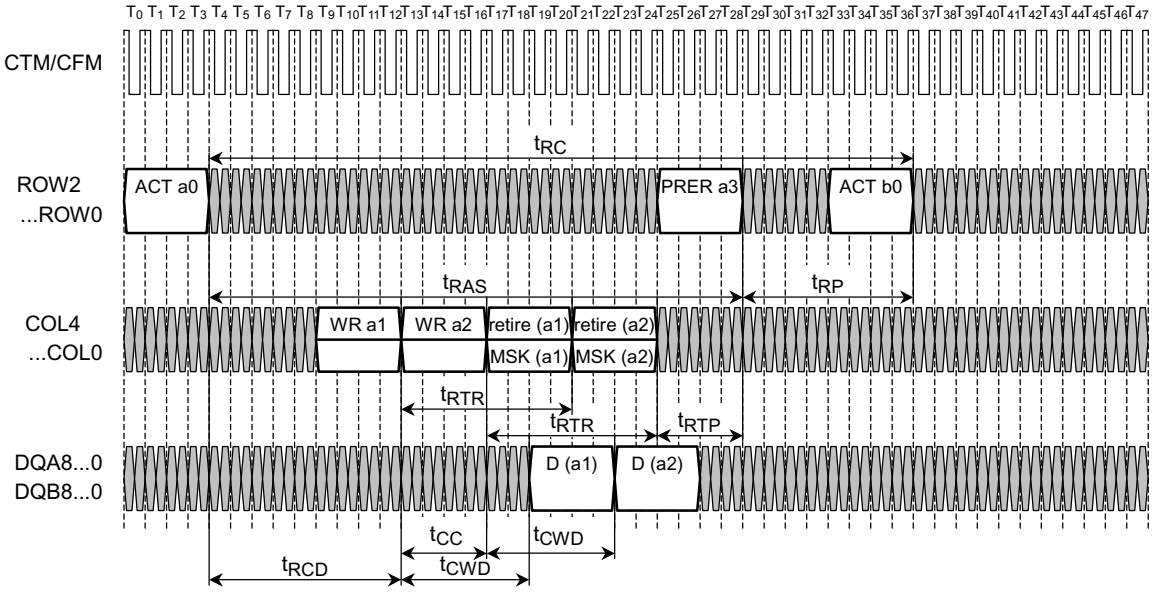
A time t_{CC} after the first COLC packet on the COL pins a second COLC packet is issued. It contains a WR a2 command. The a2 address has the same device and bank address as the a1 address (and a0 address), but a different column address. A time t_{CWD} after the second WR command a second write data dualoct D (a2) is issued.

A time t_{RTR} after each WR command an optional COLM packet MSK (a1) is issued at the same time a COLC packet is issued causing the write buffer to automatically retire. See Figure 17 for more details on the write/retire mechanism. If a COLM packet is not used, all data bytes are unconditionally written. If the COLC packet which causes the write buffer to retire is delayed, then the COLM packet (if used) must also be delayed.

Next, a PRER a3 command is issued in a ROWR packet on the ROW pins. This causes the bank to precharge so that a different row may be activated in a subsequent transaction or so that an adjacent bank may be activated. The a3 address includes the same device and bank address as the a0, a1, and a2 addresses. The PRER command must occur a time t_{RAS} or more after the original ACT command (the activation operation in any DRAM is destructive, and the contents of the selected row must be restored from the two associated sense amps of the bank during the t_{RAS} interval).

A PRER a3 command is issued in a ROWR packet on the ROW pins. The PRER command must occur a time t_{RTP} or more after the last COLC which causes an automatic retire.

Finally, an ACT b0 command is issued in a ROWR packet on the ROW pins. The second ACT command must occur a time t_{RC} or more after the first ACT command and a time t_{RP} or more after the PRER command. This ensures that the bank and its associated sense amps are precharged. This example assumes that the second transaction has the same device and bank address as the first transaction, but a different row address. Transaction b may not be stated until transaction a has finished. However, transactions to other banks or other devices may be issued during transaction a.



Transaction a: WR	a0 = {Da, Ba, Ra}	a1 = {Da, Ba, Ca1}	a2 = {Da, Ba, Ca2}	a3 = {Da, Ba}
Transaction b: XX	b0 = {Da, Ba, Rb}			

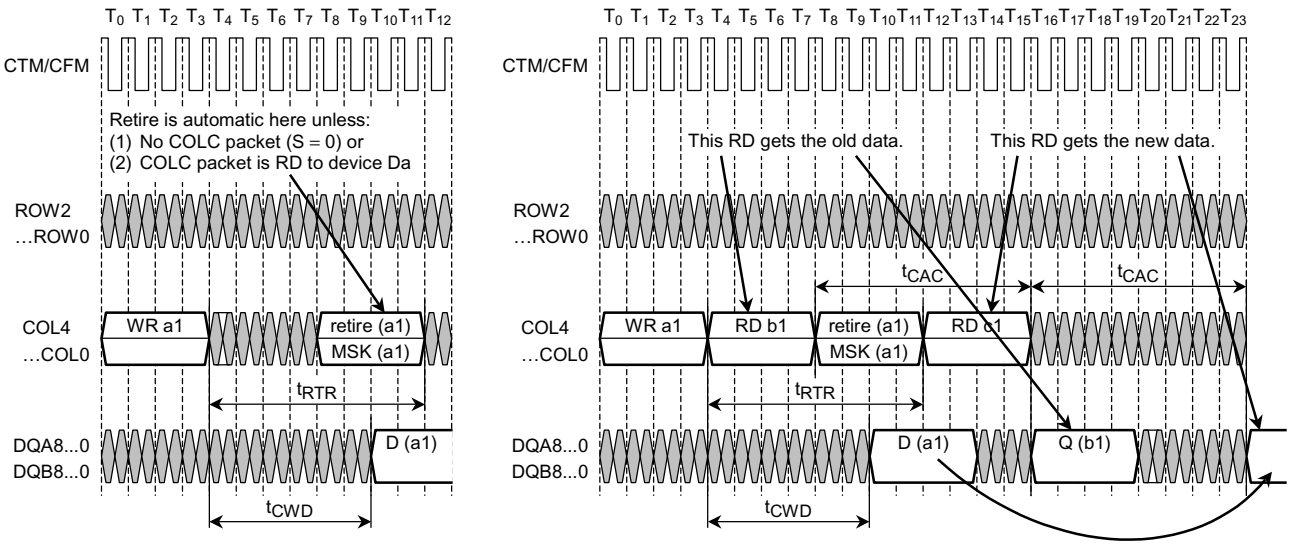
Figure 16. Write Transaction Example

Write/Retire Examples

The process of writing a dualoct into a sense amp in a RDRAM bank occurs in two steps. The first step consists of transporting the write command, write address, and write data into the write buffer. The second step happens when the RDRAM automatically retires the write buffer (with an optional byte mask) into the sense amp. This two-step write process reduces the natural turn-around delay due to the internal bidirectional data pins.

Figure 17 (left) shows an example of this two-step process. The first COLC packet contains the WR command and an address specifying the device, bank and column. The write data dualoct follows a time t_{CWD} later. This information is loaded into the write buffer of the specified device. The COLC packet which follows a time t_{RTR} later will retire the write buffer. The retire will happen automatically unless (1) a COLC packet is not framed (no COLC packet is present and the S bit is zero), or (2) the COLC packet contains a RD command to the same device. If the retire does not take place at a time t_{RTR} after the original WR command, then the device continues to frame COLC packets, looking for the first that is not a RD directed to itself. A byte mask MSK (a1) may be supplied in a COLM packet aligned with the COLC that retires the write buffer a time t_{RTR} after the WR command.

The memory controller must be aware of this two-step write/retire process. Controller performance can be improved, but only if the controller design accounts for several side effects.



Transaction a: WR	a1 = {Da, Ba, Ca1}

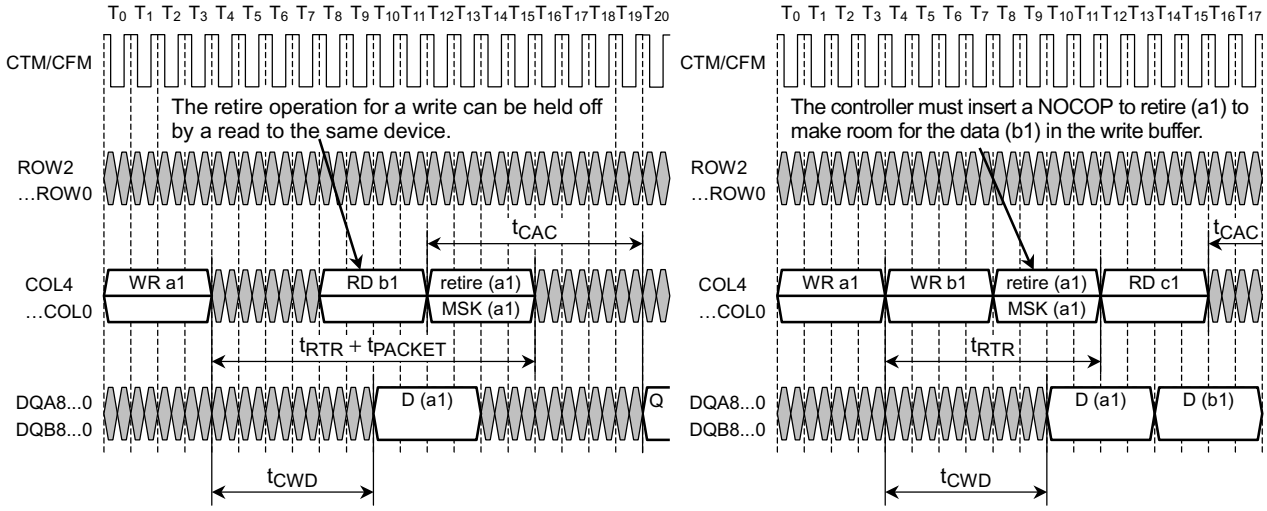
Transaction a: WR	a1 = {Da, Ba, Ca1}
Transaction b: RD	b1 = {Da, Ba, Ca1}
Transaction c: RD	c1 = {Da, Ba, Ca1}

Figure 17. Normal Retire (left) and Retire/Read Ordering (right)

Figure 17 (right) shows the first of these side effects. The first COLC packet has a WR command which loads the address and data into the write buffer. The third COLC causes an automatic retire of the write buffer to the sense amp. The second and fourth COLC packets (which bracket the retire packet) contain RD commands with the same device, bank and column address as the original WR command. In other words, the same dualoct address that is written is read both before and after it is actually retired. The first RD returns the old dualoct value from the sense amp before it is overwritten. The second RD returns the new dualoct value that was just written.

Figure 18 (left) shows the result of performing a RD command to the same device in the same COLC packet slot that would normally be used for the retire operation. The read may be to any bank and column address; all that matters is that it is to the same device as the WR command. The retire operation and MSK (a1) will be delayed by t_{PACKET} as a result. If the RD command used the same bank and column address as the WR command, the old data from the sense amp would be returned. If many RD commands, to the same device were issued instead of the single one that is shown, then the retire operation would be held off an arbitrarily long time. However, once a RD to another device or a WR or NOCOP to any device is issued, the retire will take place. Figure 18 (right) illustrates a situation in which the controller wants to issue a WR-WR-RD COLC packet sequence, with all commands addressed to the same device, but addressed to any combination of banks and columns.

The RD will prevent a retire of the first WR from automatically happening. But the first dualoct D (a1) in the write buffer will be overwritten by the second WR dualoct D (b1) if the RD command is issued in the third COLC packet. Therefore, it is required in this situation that the controller issue a NOCOP command in the third COLC packet, delaying the RD command by a time t_{PACKET}. This situation is explicitly shown in Table 10 for cases in which $t_{CCDELAY}$ is equal to t_{RTR}.

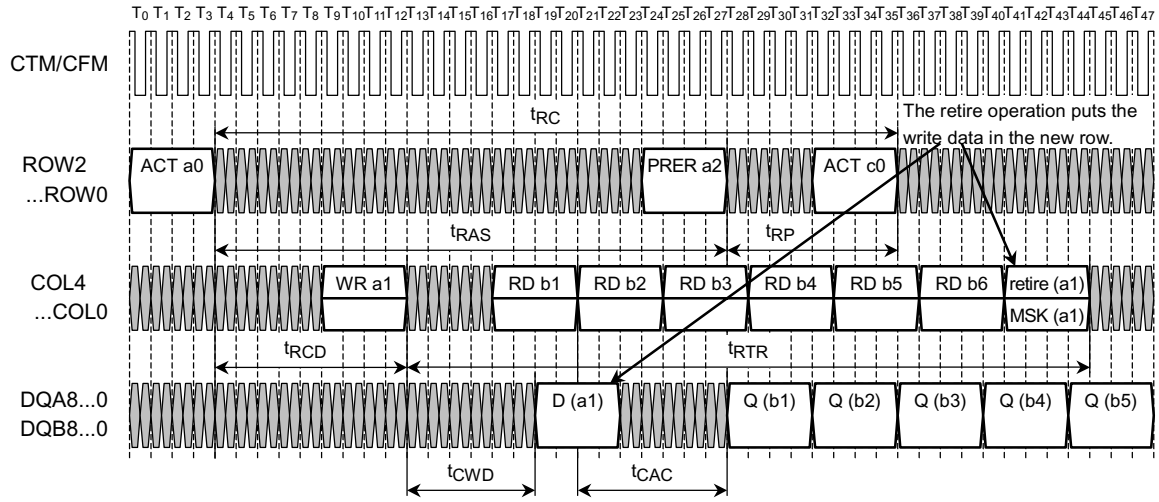


Transaction a: WR	a1 = {Da, Ba, Ca1}
Transaction b: RD	b1 = {Da, Bb, Cb1}

Transaction a: WR	a1 = {Da, Ba, Ca1}
Transaction b: WR	b1 = {Da, Bb, Cb1}
Transaction c: RD	c1 = {Da, Bc, Cc1}

Figure 18. Retire Held off by Read (left) and Controller Forcing WWR Gap (right)

Figure 19 shows a possible result when a retire is held off for a long time (an extended version of Figure 18 (left)). After a WR command, a series of six RD commands are issued to the same device (but to any combination of bank and column addresses). In the meantime, the bank Ba to which the WR command was originally directed is precharged, and a different row Rc is activated. When the retire is automatically performed, it is made to this new row, since the write buffer only contains the bank and column address, not the row address. The controller can ensure that this does not happen by never precharging a bank with an unretired write buffer. Note that in a system with more than one RDRAM, there will never be more than two RDRAMs with unretired write buffers. This is because a WR command issued to one device automatically retires the write buffers of all other devices written a time t_{RTR} before or earlier.



Transaction a: WR	a0 = {Da, Ba, Ra}	a1 = {Da, Ba, Ca1}	a2 = {Da, Ba}
Transaction b: RD	b0 = {Da, Bb, Cb1}	b2 = {Da, Bb, Cb2}	b3 = {Da, Bb, Cb3}
	b4 = {Da, Bb, Cb4}	b5 = {Da, Bb, Cb5}	b6 = {Da, Bb, Cb6}
Transaction c: WR	c0 = {Da, Ba, Rc}		

WARNING
This sequence is hazardous and must be used with caution.

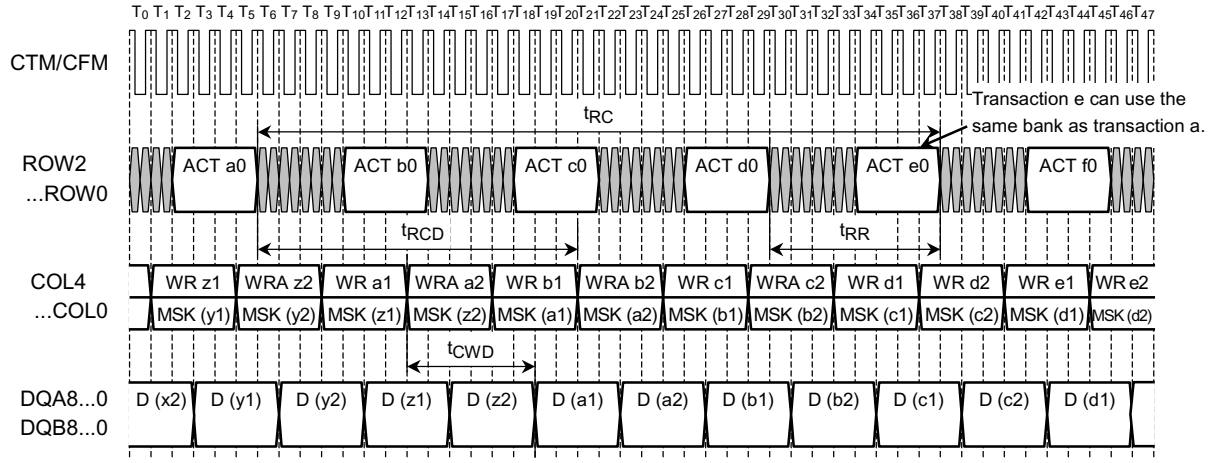
Figure 19. Retire Held off by Reads to Same Device, Write Buffer Retired to New Row

Interleaved Write Example

Figure 20 shows an example of an interleaved write transaction. Transactions similar to the one presented in Figure 16 are directed to non-adjacent banks of a single RDRAM. This allows a new transaction to be issued once every t_{RR} interval rather than once every t_{RC} interval (four times more often). The DQ data pin efficiency is 100% with this sequence.

With two dualocts of data written per transaction, the COL, DQA and DQB pins are fully utilized. Banks are precharged using the WRA autoprecharge option rather than the PRER command in a ROWR packet on the ROW pins.

In this example, the first transaction is directed to device Da and bank Ba. The next three transactions are directed to the same device Da, but need to use different, non-adjacent banks Bb, Bc and Bd so there is no bank conflict. The fifth transaction could be redirected back to bank Ba without interference, since the first transaction would have completed by then (t_{RC} has elapsed). Each transaction may use any value for row address (Ra, Rb, · · ·) and column address (Ca1, Ca2, Cb1, Cb2, · · ·).



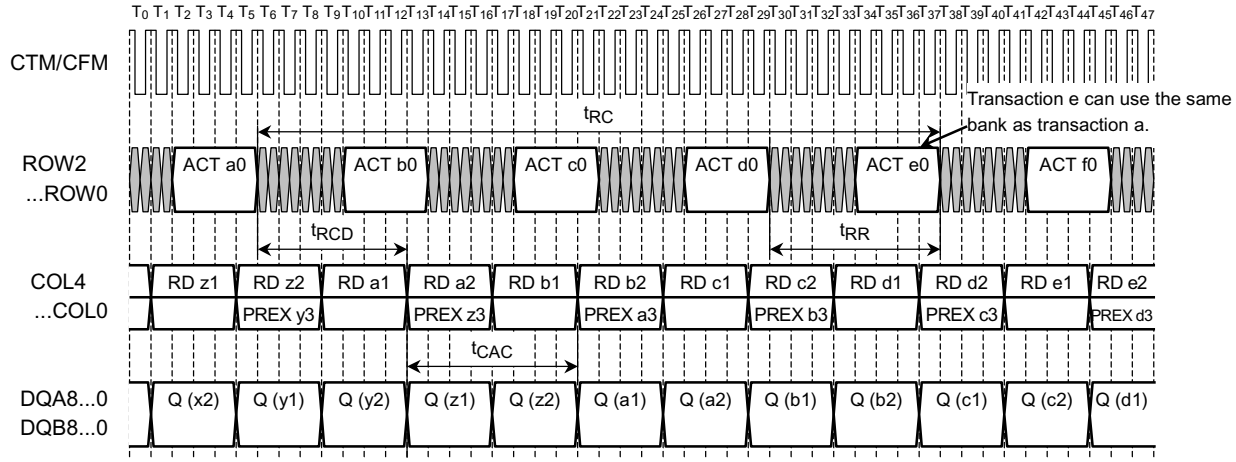
Transaction y: WR	y0 = {Da, Ba + 4, Ry}	y1 = {Da, Ba + 4, Cy1}	y2 = {Da, Ba + 4, Cy2}	y3 = {Da, Ba + 4}
Transaction z: WR	z0 = {Da, Ba + 6, Rz}	z1 = {Da, Ba + 6, Cz1}	z2 = {Da, Ba + 6, Cz2}	z3 = {Da, Ba + 6}
Transaction a: WR	a0 = {Da, Ba, Ra}	a1 = {Da, Ba, Ca1}	a2 = {Da, Ba, Ca2}	a3 = {Da, Ba}
Transaction b: WR	b0 = {Da, Ba + 2, Rb}	b1 = {Da, Ba + 2, Cb1}	b2 = {Da, Ba + 2, Cb2}	b3 = {Da, Ba + 2}
Transaction c: WR	c0 = {Da, Ba + 4, Rc}	c1 = {Da, Ba + 4, Cc1}	c2 = {Da, Ba + 4, Cc2}	c3 = {Da, Ba + 4}
Transaction d: WR	d0 = {Da, Ba + 6, Rd}	d1 = {Da, Ba + 6, Cd1}	d2 = {Da, Ba + 6, Cd2}	d3 = {Da, Ba + 6}
Transaction e: WR	e0 = {Da, Ba, Re}	e1 = {Da, Ba, Ce1}	e2 = {Da, Ba, Ce2}	e3 = {Da, Ba}
Transaction f: WR	f0 = {Da, Ba + 2, Rf}	f1 = {Da, Ba + 2, Cf1}	f2 = {Da, Ba + 2, Cf2}	f3 = {Da, Ba + 2}

Figure 20. Interleaved Write Transaction with Two Dualocts Data Length

Interleaved Read Example

Figure 21 shows an example of an interleaved read transaction. Transactions similar to the one presented in Figure 15 are directed to non-adjacent banks of a single RDRAM. The address sequence is identical to the one used in the previous write example. The DQ data pins efficiency is also 100%.

The only difference with the write example (aside from the use of the RD command rather than the WR command) is the use of the PREX command in a COLX packet to precharge the banks rather than the RDA command. This is done because the PREX is available for a read transaction but is not available for a masked write transaction.



Transaction y: RD	y0 = {Da, Ba + 4, Ry}	y1 = {Da, Ba + 4, Cy1}	y2 = {Da, Ba + 4, Cy2}	y3 = {Da, Ba + 4}
Transaction z: RD	z0 = {Da, Ba + 6, Rz}	z1 = {Da, Ba + 6, Cz1}	z2 = {Da, Ba + 6, Cz2}	z3 = {Da, Ba + 6}
Transaction a: RD	a0 = {Da, Ba, Ra}	a1 = {Da, Ba, Ca1}	a2 = {Da, Ba, Ca2}	a3 = {Da, Ba}
Transaction b: RD	b0 = {Da, Ba + 2, Rb}	b1 = {Da, Ba + 2, Cb1}	b2 = {Da, Ba + 2, Cb2}	b3 = {Da, Ba + 2}
Transaction c: RD	c0 = {Da, Ba + 4, Rc}	c1 = {Da, Ba + 4, Cc1}	c2 = {Da, Ba + 4, Cc2}	c3 = {Da, Ba + 4}
Transaction d: RD	d0 = {Da, Ba + 6, Rd}	d1 = {Da, Ba + 6, Cd1}	d2 = {Da, Ba + 6, Cd2}	d3 = {Da, Ba + 6}
Transaction e: RD	e0 = {Da, Ba, Re}	e1 = {Da, Ba, Ce1}	e2 = {Da, Ba, Ce2}	e3 = {Da, Ba}
Transaction f: RD	f0 = {Da, Ba + 2, Rf}	f1 = {Da, Ba + 2, Cf1}	f2 = {Da, Ba + 2, Cf2}	f3 = {Da, Ba + 2}

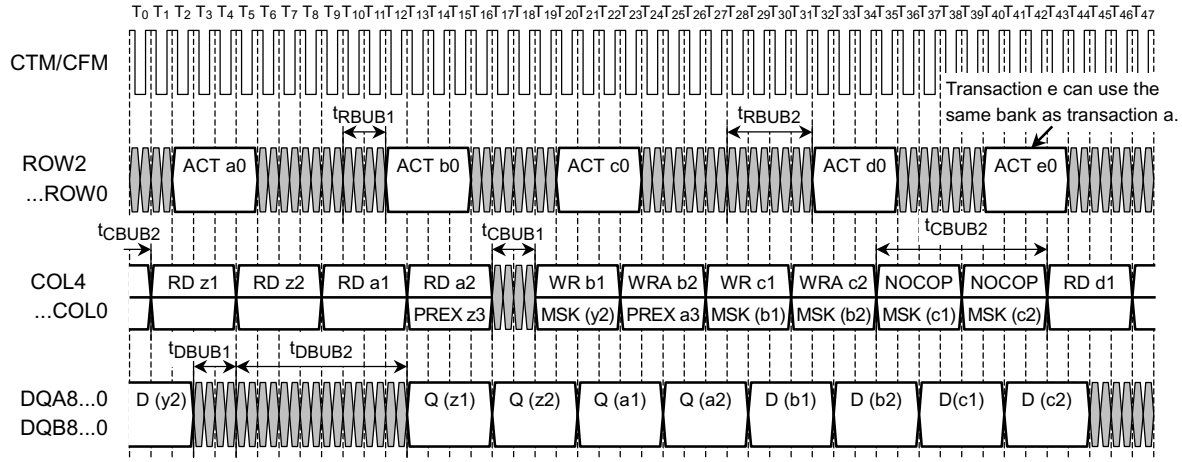
Figure 21. Interleaved Read Transaction with Two Dualocts Data Length

Interleaved RRWW Example

Figure 22 shows a steady-state sequence of two-dualoct RD/RD/WR/WR… transactions directed to non-adjacent banks of a single RDRAM. This is similar to the interleaved write and read examples in Figure 20 and Figure 21, except that bubble cycles need to be inserted by the controller at read/write boundaries. The DQ data pin efficiency for the example in Figure 22 is 32/42 or 76%. If there were more RDRAMs on the Channel, the DQ pin efficiency would approach 32/34 or 94% for the two-dualoct RRWW sequence (this case is not shown).

In Figure 22, the first bubble-type t_{CBUB1} is inserted by the controller between a RD and a WR command on the COL pins. This bubble accounts for the round-trip propagation delay that is seen by read data, and is explained in detail in Figure 4. This bubble appears on the DQA and DQB pins as t_{DBUB1} between a write data dualoct D and a read data dualoct Q. This bubble also appears on the ROW pins as t_{RBUB1}.

The second bubble-type t_{CBUB2} is inserted (as a NOCOP command) by the controller between a WR command and a RD command on the COL pins when there is a WR-WR-RD sequence directed at a single device. This bubble enables write data to be retired from the write buffer without being lost, and is explained in detail in Figure 18. There would be no bubble if address c0 and address d0 were directed at different devices. This bubble appears on the DQA and DQB pins as t_{DBUB2} between a write data dualoct D and a read data dualoct Q. This bubble also appears on the ROW pins as t_{RBUB2}.



Transaction y: WR	y0 = {Da, Ba + 4, Ry}	y1 = {Da, Ba + 4, Cy1}	y2 = {Da, Ba + 4, Cy2}	y3 = {Da, Ba + 4}
Transaction z: RD	z0 = {Da, Ba + 6, Rz}	z1 = {Da, Ba + 6, Cz1}	z2 = {Da, Ba + 6, Cz2}	z3 = {Da, Ba + 6}
Transaction a: RD	a0 = {Da, Ba, Ra}	a1 = {Da, Ba, Ca1}	a2 = {Da, Ba, Ca2}	a3 = {Da, Ba}
Transaction b: WR	b0 = {Da, Ba + 2, Rb}	b1 = {Da, Ba + 2, Cb1}	b2 = {Da, Ba + 2, Cb2}	b3 = {Da, Ba + 2}
Transaction c: WR	c0 = {Da, Ba + 4, Rc}	c1 = {Da, Ba + 4, Cc1}	c2 = {Da, Ba + 4, Cc2}	c3 = {Da, Ba + 4}
Transaction d: RD	d0 = {Da, Ba + 6, Rd}	d1 = {Da, Ba + 6, Cd1}	d2 = {Da, Ba + 6, Cd2}	d3 = {Da, Ba + 6}
Transaction e: RD	e0 = {Da, Ba, Re}	e1 = {Da, Ba, Ce1}	e2 = {Da, Ba, Ce2}	e3 = {Da, Ba}
Transaction f: WR	f0 = {Da, Ba + 2, Rf}	f1 = {Da, Ba + 2, Cf1}	f2 = {Da, Ba + 2, Cf2}	f3 = {Da, Ba + 2}

Figure 22. Interleaved RRWW Sequence with Two Dualocts Data Length

Control Register Transactions

The RDRAM has two CMOS input pins SCK and CMD, and two CMOS input/output pins SIO0 and SIO1. These provide serial access to a set of control registers in the RDRAM. These control registers provide configuration information to the controller during the initialization process. They also allow an application to select the appropriate operating mode for the RDRAM.

SCK (Serial Clock) and CMD (Command) are driven by the controller to all RDRAMs in parallel. SIO0 and SIO1 are connected (in a daisy chain fashion) from one RDRAM to the next. In normal operation, the data on SIO0 is repeated on SIO1, which connects to SIO0 of the next RDRAM (the data is repeated from SIO1 to SIO0 for a read data packet). The controller connects to SIO0 of the first RDRAM.

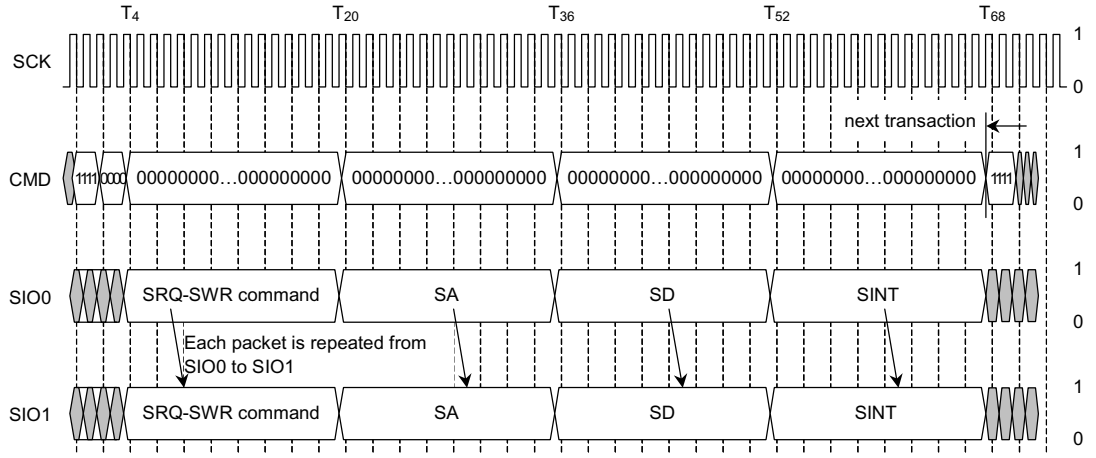


Figure 23. Serial Write (SWR) Transaction to Control Register

Write and read transactions are each composed of four packets, as shown in Figure 23 and Figure 24.

Each packet consists of 16 bits, as summarized in Table 12 and Table 13. The packet bits are sampled on the falling edge of SCK. A transaction begins with a SRQ (Serial Request) packet. This packet is framed with a 11110000 pattern on the CMD input (note that the CMD bits are sampled on both the falling and rising edges of SCK). The SRQ packet contains the SOP3…SOP0 (Serial Op-code) field, which selects the transaction type. The SDEV5…SDEV0 (Serial Device address) selects one of the 32 RDRAMs. If SBC (Serial Broadcast) is set, then all RDRAMs are selected. The SA (Serial Address) packet contains a 12 bit address for selecting a control register.

A write transaction has a SD (Serial Data) packet next. This contains 16 bits of data that is written into the selected control register. An SINT (serial interval) packet is last, providing some delay for any side-effects to take place. A read transaction has a SINT packet, then a SD packet. This provides a delay for the selected RDRAM to access the control register. The SD read data packet travels in the opposite direction (towards the controller) from the other packet types. The SCK cycle time will accommodate the total delay.

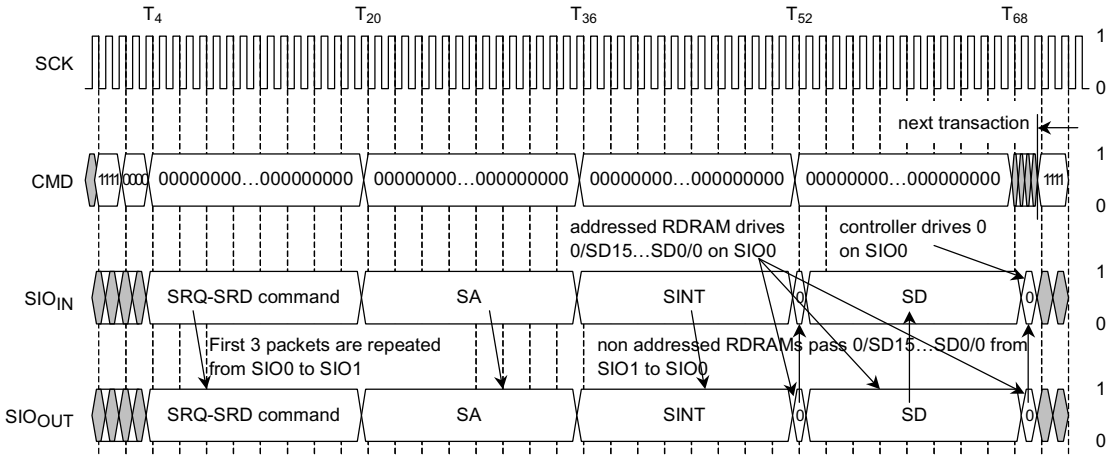


Figure 24. Serial Read (SRD) Transaction to Control Register

Control Register Packets

Table 12 summarizes the formats of the four packet types for control register transactions. Table 13 summarizes the fields that are used within the packets.

Figure 25 shows the transaction format for the SETR, CLRR, and SETF commands. These transactions consist of a single SRQ packet, rather than four packets like the SWR and SRD commands. The same framing sequence on the CMD input is used, however. These commands are used during initialization prior to any control register read or write transactions.

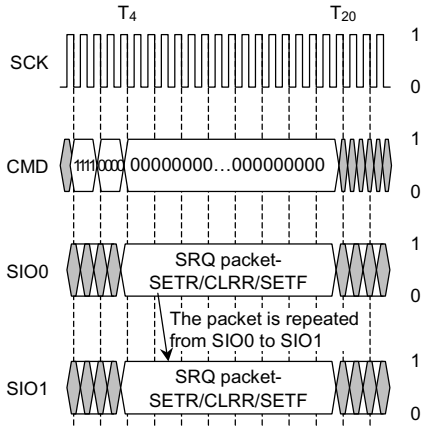


Figure 25. SETR, CLRR, SETF Transaction

Table 12. Control Register Packet Formats

SCK Cycle	SIO0 or SIO1 for SRQ	SIO0 or SIO1 for SA	SIO0 or SIO1 for SINT	SIO0 or SIO1 for SD	SCK Cycle	SIO0 or SIO1 for SRQ	SIO0 or SIO1 for SA	SIO0 or SIO1 for SINT	SIO0 or SIO1 for SD
0	rsrv	rsrv	0	SD15	8	SOP1	SA7	0	SD7
1	rsrv	rsrv	0	SD14	9	SOP0	SA6	0	SD6
2	rsrv	rsrv	0	SD13	10	SBC	SA5	0	SD5
3	rsrv	rsrv	0	SD12	11	SDEV4	SA4	0	SD4
4	rsrv	SA11	0	SD11	12	SDEV3	SA3	0	SD3
5	SDEV5	SA10	0	SD10	13	SDEV2	SA2	0	SD2
6	SOP3	SA9	0	SD9	14	SDEV1	SA1	0	SD1
7	SOP2	SA8	0	SD8	15	SDEV0	SA0	0	SD0

Table 13. Field Description for Control Register Packets

Field	Description
rsrv	Reserved. Should be driven as “0” by controller.
SOP3…SOP0	0000-SRD. Serial read of control register {SA11..SA0} of RDRAM {SDEV5..SDEV0}.
	0001-SWR. Serial write of control register {SA11..SA0} of RDRAM {SDEV5..SDEV0}.
	0010-SETR. Set Reset bit; all control registers assume their reset values. [a] 16 t_{SCYCLE} delay until CLRR command.
	0100-SETF. Set Fast (Normal) Clock Mode. [a] 4 t_{SCYCLE} delay until next command.
	1011-CLRR. Clear Reset bit; all control registers retain their reset values. [a] 4 t_{SCYCLE} delay until next command.
	1111-NOP. No serial operation.
	0011, 0101-1010, 1100-1110-RSRV. Reserved encodings.
SDEV5…SDEV0	Serial device. Compared to SDEVID5..SDEVID0 field of INIT control register field to select the RDRAM to which the transaction is directed.
SBC	Serial broadcast. When set, RDRAMs ignore {SDEV5..SDEV0} for RDRAM selection.
SA11…SA0	Serial address. Selects which control register of the selected RDRAM is read or written.
SD15…SD0	Serial data. The 16 bits of data written to or read from the selected control register of the selected RDRAM.

a. The SETR and CLRR commands must always be applied in two successive transactions to RDRAMs; i.e. they may not be used in isolation. This is called “SETR/CLRR Reset”.

Initialization

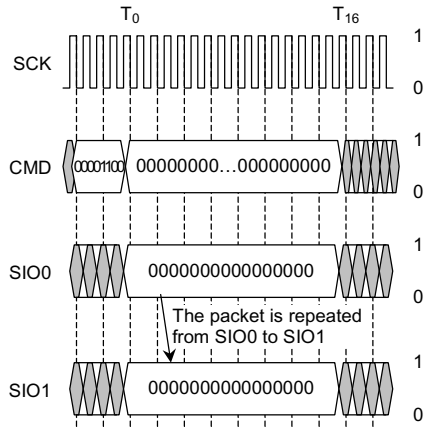


Figure 26. SIO Reset Sequence

Initialization refers to the process that a controller must go through after power is applied to the system or the system is reset. The controller prepares the RDRAM sub-system for normal Channel operation by using a sequence of control register transactions on the serial CMOS pins.

The following steps outline the sequence seen by the various memory subsystem components (including the RDRAM components) during initialization. This sequence is available in the form of reference code. Contact Rambus Inc. for more information.

1.0 Start Clocks

This step calculates the proper clock frequencies for PClk (controller logic), SynClk (RAC block), RefClk (DRCG component), CTM (RDRAM component), and SCK (SIO block).

2.0 RAC Initialization

This step causes the INIT block to generate a sequence of pulses which resets the RAC, performs RAC maintenance operations, and measures timing intervals in order to ensure clock stability.

3.0 RDRAM Initialization

This stage performs most of the steps needed to initialize the RDRAMs. The rest are performed in stages 5.0, 6.0, and 7.0. All of the steps in 3.0 are carried out through the SIO block interface.

- 3.1/3.2 SIO Reset
  After a delay of t_{PAUSE} from step 1.0, this reset operation is performed before any SIO control register read or write transactions. It clears six registers (TEST34, CCA, CCB, SKIP, TEST78, and TEST79) and places the INIT register into a special state (all bits cleared except SKP and SDEVID fields are set to ones). CMD and SIO must be held low until SIO Reset.

- 3.3 Write TEST77 Register
  The TEST77 register must be explicitly written with zeros before any other registers are read or written.

- 3.4 Write TCYCLE Register
  The TCYCLE register is written with the cycle time t_{CYCLE} of the CTM clock (for Channel and RDRAMs) in units of 64 ps. The t_{CYCLE} value is determined in stage 1.0.

- 3.5 Write SDEVID Register
  The SDEVID (serial device identification) register of each RDRAM is written with a unique address value so that directed SIO read and write transactions can be performed. This address value increases from 0 to 31 according to the distance a RDRAM is from the ASIC component on the SIO bus (the closest RDRAM is address 0).

- 3.6 Write DEVID Register
  The DEVID (device identification) register of each RDRAM is written with a unique address value so that directed memory read and write transactions can be performed. This address value increases from 0 to 31. The DEVID value is not necessarily the same as the SDEVID value. RDRAMs are sorted into regions of the same core configuration (number of bank, row, and column address bits and core type).

- 3.7 Write PDNX, PDNXA Registers
  The PDNX and PDNXA registers are written with values that are used to measure the timing intervals connected with an exit from the PDN (Powerdown) power state.

- 3.8 Write NAPX Register
  The NAPX register is written with values that are used to measure the timing intervals connected with an exit from the NAP power state.

- 3.9 Write TPARM Register
  The TPARM register is written with values which determine the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The values written set each RDRAM to the minimum value permitted for the system. This will be adjusted later in stage 6.0.

- 3.10 Write TCDLY1 Register
  The TCDLY1 register is written with values which determine the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The values written set each RDRAM to the minimum value permitted for the system. This will be adjusted later in state 6.0.

- 3.11 Write TFRM Register
  The TFRM register is written with a value that is related to the t_{RCD} parameter for the system. The t_{RCD} parameter is the time interval between a ROW packet with an activate command and the COL packet with a read or write command.

- 3.12 SETR/CLRR-First write the following registers with the indicated values:
  TEST78 $\Leftarrow 0004_{16}$
  TEST34 $\Leftarrow 0040_{16}$
  Next, each RDRAM is given a SETR command and a CLRR command through the SIO block. This sequence performs a second reset operation on the RDRAMs. Then the TEST34 and TEST78 registers are rewritten with zero, in that order.

- 3.13 Write CCA and CCB Register
  These registers are written with a value halfway between their minimum and maximum values. This shortens the time needed for the RDRAMs to reach their steady-state current control values in state 5.0.

- 3.14 Powerdown Exit
  The RDRAMs are in the PDN power state at this point. A broadcast PDN Exit command is performed by the SIO block to place the RDRAMs in the RLX (relax) power state in which they are ready to receive ROW packets.

- 3.15 SETF
  Each RDRAM is given a SETF command through the SIO block. One of the operations performed by this step is to generate a value for the AS (autoskip) bit in the SKIP register and fix the RDRAM to a particular read domain.

4.0 Controller Configuration

This stage initializes the controller block. Each step of this stage will set a field of the ConfigRMC[63:0] bus to the appropriate value. Other controller implementations will have similar initialization requirements, and this stage may be used as a guide.

- 4.1 Initial Read Data Offset
  The ConfigRMC bus is written with a value which determines the time interval between a COL packet with a memory read command and the Q packet with the read data on the Channel. The value written sets RMC.d1 to the minimum value permitted for the system. This will be adjusted later in stage 6.0.

- 4.2 Configure Row/Column Timing
  This step determines the values of the $t_{RAS,MIN}$, $t_{RP,MIN}$, $t_{RC,MIN}$, $t_{RCD,MIN}$, $t_{RR,MIN}$, and $t_{PP,MIN}$ RDRAM timing parameters that are present in the system. The ConfigRMC busies written with values that will be compatible with all RDRAM devices that are present.

- 4.3 Set Refresh Interval
  This step determines the values of the $t_{REF,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

- 4.4 Set Current Control Interval
  This step determines the values of the $t_{CCTRL,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

- 4.5 Set Slew Rate Control Interval
  This step determines the values of the $t_{TEMP,MAX}$ RDRAM timing parameter that are present in the system. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

- 4.6 Set Bank/Row/Col Address Bits
  This step determines the number of RDRAM bank, row, and column address bits that are present in the system. It also determines the RDRAM core types (independent, doubled, or split) that are present. The ConfigRMC bus is written with a value that will be compatible with all RDRAM devices that are present.

5.0 RDRAM Current Control

This step causes the INIT block to generate a sequence of pulses which performs RDRAM maintenance operations.

6.0 RDRAM Core, Read Domain Initialization

This stage completes the RDRAM initialization.

- 6.1 RDRAM Core Initialization
  A sequence of 192 memory refresh transactions is performed in order to place the cores of all RDRAMs into the proper operating state.

- 6.2 RDRAM Read Domain Initialization
  A memory write and memory read transaction is performed to each RDRAM to determine which read domain each RDRAM occupies. The programmed delay of each RDRAM is then adjusted so the total RDRAM read delay (propagation delay plus programmed delay) is constant. The TPARM and TCDLY1 registers of each RDRAM are rewritten with the appropriate read delay values. The ConfigRMC bus is also rewritten with an updated value.

7.0 Other RDRAM Register Fields

This stage rewrites the INIT register with the final values of the LSR, NSR, and PSR fields.

In essence, the controller must read all the read-only configuration registers of all RDRAMs (or it must read the SPD device present on each RIMM), it must process this information, and then it must write all the read-write registers to place the RDRAMs into the proper operating mode.

Initialization Note [1]:

During the initialization process, it is necessary for the controller to perform 128 current control operations (3 × CAL, 1 × CAL/SAM) and one temperature calibrate operation (TCEN/TCAL) after reset or after Powerdown (PDN) exit.

Initialization Note [2]:

Does not apply to this RDRAM type; this note had been generated for earlier 64M and 128M devices, but does not apply to this device.

Initialization Note [3]:

After the step of equalizing the total read delay of each RDRAM has been completed (i.e. after the TCDLY0 and TCDLY1 fields have been written for the final time), a single final memory read transaction should be made to each RDRAM in order to ensure that the output pipeline stages have been cleared.

Initialization Note [4]:

The SETF command (in the serial SRQ packet) should only be issued once during the Initialization process, as should the SETR and CLRR commands.

Initialization Note [5]:

The CLRR command (in the serial SRQ packet) leaves some of the contents of the memory core in an indeterminate state.

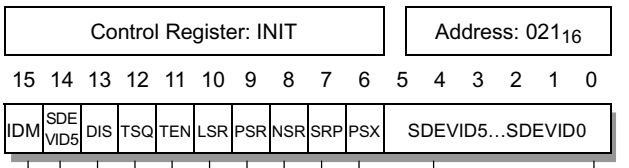
Control Register Summary

Table 14 summarizes the RDRAM control registers. Detail is provided for each control register in Figure 27 through Figure 31. Read-only bits which are shaded gray are unused and return zero. Read-write bits which are shaded gray are reserved and should always be written with 0. The RIMM SPD Application Note (Rambus Inc. Document DL0054) describes additional read-only configuration registers which are present on Direct RIMMS.

The state of the register fields are potentially affected by the SIO Reset operation or the SETR/CLRR operation. This is indicated in the text accompanying each register diagram.

Table 14. Control Register Summary

SA11…SA0	Register	Field	Read-write, or read-only	Description
021_{16}	INIT	SDEVID	read-write, 6 bits	Serial device ID. Device address for control register read/write.
		PSX	read-write, 1 bit	Power Select exit. PDN/NAP exit with device address on DQA5…0.
		SRP	read-write, 1 bit	SIO repeater. Used to initialize RDRAM.
		NSR	read-write, 1 bit	NAP Self-Refresh. Enables Self-Refresh in NAP Mode.
		PSR	read-write, 1 bit	PDN Self-Refresh. Enables Self-Refresh in PDN Mode.
		LSR	read-write, 1 bit	Low-power Self-Refresh. Enables low-power Self-Refresh.
		TEN	read-write, 1 bit	Temperature sensing enable.
		TSQ	read-write, 1 bit	Temperature sensing output.
		DIS	read-write, 1 bit	RDRAM disable.
		IDM	read-write, 1 bit	Interleaved Device Mode enable.
022_{16}	TEST34	TEST34	read-write, 16 bits	Test register. Do not read or write after SIO reset.
023_{16}	CNFGA	REFBIT	read-only, 3 bits	Refresh bank bits. Used for Multi-Bank refresh.
		DBL	read-only, 1 bit	Double. Specifies Doubled-Bank architecture.
		MVER	read-only, 6 bits	Manufacturer version. Manufacturer identification number.
		PVER	read-only, 6 bits	Protocol version. Specifies version of Direct protocol supported.
024_{16}	CNFGB	BYT	read-only, 1 bit	Byte. Specifies an 8-bit or 9-bit byte size.
		DEVTYP	read-only, 3 bits	Device type. Device can be RDRAM or some other device category.
		SPT	read-only, 1 bit	Split-core. Each core half is an individual dependent core.
		CORG	read-only, 5 bits	Core organization. Bank, row, column address field sizes.
		SVER	read-only, 6 bits	Stepping version. Mask version number.
040_{16}	DEVID	DEVID	read-write, 5 bits	Device ID. Device address for memory read/write.
041_{16}	REFB	REFB	read-write, 5 bits	Refresh bank. Next bank to be refreshed by Self-Refresh.
042_{16}	REFR	REFR	read-write, 9 bits	Refresh row. Next row to be refreshed by REFA, Self-Refresh.
043_{16}	CCA	CCA	read-write, 7 bits	Current control A. Control I_{OL} output current for DQA.
		ASYMA	read-write, 1 bits	Asymmetry control. Controls asymmetry of V_{OL}/V_{OH} swing for DQA.
044_{16}	CCB	CCB	read-write, 7 bits	Current control B. Control I_{OL} output current for DQB.
		ASYMB	read-write, 1 bits	Asymmetry control. Controls asymmetry of V_{OL}/V_{OH} swing for DQB.
045_{16}	NAPX	NAPXA	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A.
		NAPX	read-write, 5 bits	NAP exit. Specifies length of NAP exit phase A + phase B.
		DQS	read-write, 1 bit	DQ select. Selects CMD framing for NAP/PDN exit.
046_{16}	PDNXA	PDNXA	read-write, 6 bits	PDN exit. Specifies length of PDN exit phase A.
047_{16}	PDNX	PDNX	read-write, 3 bits	PDN exit. Specifies length of PDN exit phase A + phase B.
048_{16}	TPARM	TCAS	read-write, 2 bits	t_{CAS-C} core parameter. Determines t_{OFFP} datasheet parameter.
		TCLS	read-write, 2 bits	t_{CLS-C} core parameter. Determines t_{CAC} and t_{OFFP} datasheet parameter.
		TCDLY0	read-write, 3 bits	$t_{CDLY0-C}$ core parameter. Programmable delay for read data.
049_{16}	TFRM	TFRM	read-write, 4 bits	t_{FRM-C} core parameter. Determines ROW-to-COL packet framing interval.
$04a_{16}$	TCDLY1	TCDLY1	read-write, 2 bits	$t_{CDLY1-C}$ datasheet parameter. Programmable delay for read data.
$04c_{16}$	TCYCLE	TCYCLE	read-write, 6 bits	t_{CYCLE} datasheet parameter. Specifies cycle time in 64 ps units.
$04b_{16}$	SKIP	AS	read-only, 1 bit	Autoskip value established by the SETF command.
		MSE	read-write, 1 bit	Manual skip enable. Allows the MS value to override the AS value.
		MS	read-write, 1 bit	Manual skip value.
$04d_{16}$	TEST77	TEST77	read-write, 16 bits	Test register. Write with zero after SIO reset.
$04e_{16}$	TEST78	TEST78	read-write, 16 bits	Test register. Do not read or write after SIO reset.
$04f_{16}$	TEST79	TEST79	read-write, 16 bits	Test register. Do not read or write after SIO reset.
080_{16}-off$_{16}$	reserved	reserved	vendor-specific	Vendor-specific test registers. Do not read or write after SIO reset.



Read/write register.
Reset values are undefined except as affected by SIO Reset as noted below. SETR/CLRR Reset does not affect this register.

SDEVID5…0-Serial Device Identification. Compared with SDEV5…0, serial address field of serial request packet for register read/write transactions. This determines which RDRAM is selected for the register read or write operation. **SDEVID resets to $3f_{16}$**.

PSX-Power Exit Select. PDN and NAP are exited with (= 0) or without (= 1) a device address on the DQA5…0 pins. PDEV5 (on DQA5) selects broadcast (1) or directed (0) exit. For a directed exit, PDEV4…0 (on DQA4…0) is compared to DEVID4…0 to select a device.

SRP-SIO Repeater. Controls value on SIO1; SIO1 = SIO0 if SRP = 1; SIO1 = 1 if SRP = 0. **SRP resets to 1**.

NAP Self-Refresh. NSR = 1 enables Self-Refresh in NAP Mode. NSR can't be set while in NAP mode. **NSR resets to 0.**

PDN Self-Refresh. PSR = 1 enables Self-Refresh in PDN Mode. PSR can't be set while in PDN mode. **PSR resets to 0.**

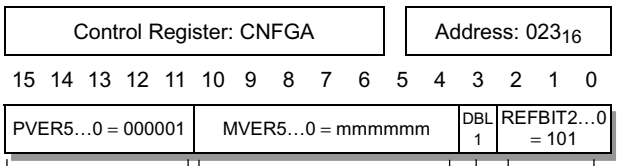
Low-Power Self-Refresh. LSR = 1 enables longer self-refresh interval. The self-refresh supply current is reduced. Longer self-refresh is not supported in this RDRAM. **Do not set LSR to 1**.

Temperature Sensing Enable. TEN = 1 enables temperature sensing circuitry, permitting the TSQ bit to be read to determine if a thermal trip point has been exceeded. **TEN resets to 0**.

Temperature Sensing Output. TSQ = 1 when a temperature trip point has been exceeded, TSQ = 0 when it has not. TSQ is available during a current control operation (see Figure 38).

RDRAM Disable. DIS = 1 causes RDRAM to ignore NAP/PDN exit sequence, DIS = 0 permits normal operation. This mechanism disables an RDRAM. **DIS resets to 0**.

Interleaved Device Mode. IDM = 1 causes 8 RDRAMs interleave read/write data, IDM = 0 permits normal operation (see Figure 48). **IDM resets to 0**.



Read-only register.

REFBIT2…0-Refresh Bank Bits. Specifies the number of bank address bits used by REFA and REFP commands. Permits multi-bank refresh in future RDRAMs.

DBL-Doubled-Bank. DBL = 1 means the device uses a doubled-bank architecture with adjacent-Bank dependency. DBL = 0 means no dependency.

MVER5…0-Manufacturer Version. Specifies the manufacturer identification number.

PVER5…0-Protocol Version. Specifies the Direct protocol version used by this device:

0-Compliant with version 0.62.
1-Compliant with version 0.7 through this version.
2~63-Reserved

Note: In RDRAMs with protocol version 1 PVER[5:0] = 000001, the range of the PDNX field (PDNX[2:0] in the PDNX register) may not be large enough to specify the location of the restricted interval in Figure 35. In this case, the effective t_{H4} parameter must increase and no row or column packets may overlap the restricted interval. See Figure 35 and page 54.

Figure 27. Control Registers

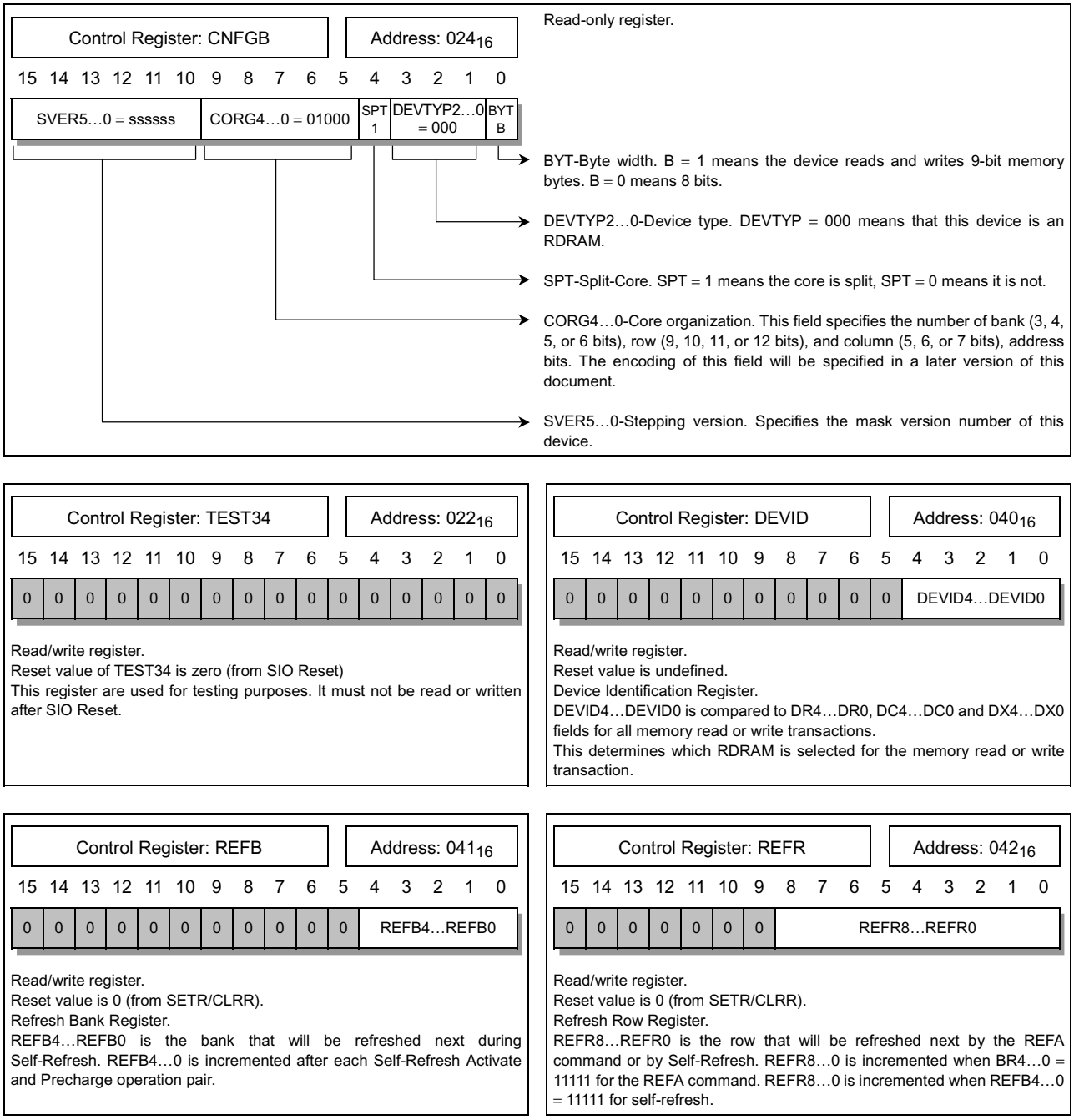


Figure 28. Control Registers

Control Register: CCA — Address: 043_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ASYMA 0		CCA6…CCA0					

Read/write register.
Reset value is 0 (SETR/CLRR or SIO Reset).
CCA6…CCA0-Current Control A. Controls the I_{OL} output current for the DQA8…DQA0 pins.

ASYMA control the asymmetry of the V_{OL}/V_{OH} voltage swing about the V_{REF} reference voltage for the DQA8…0 pins.

Control Register: CCB — Address: 044_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ASYMB 0		CCB6…CCB0					

Read/write register.
Reset value is 0 (SETR/CLRR or SIO Reset).
CCB6…CCB0-Current Control B. Controls the I_{OL} output current for the DQB8…DQB0 pins.

ASYMB control the asymmetry of the V_{OL}/V_{OH} voltage swing about the V_{REF} reference voltage for the DQB8…0 pins.

Control Register: NAPX — Address: 045_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	DQS	NAPX4…0					NAPXA4…0				

Read/write register.
Reset value is undefined.
Note-t_{SCYCLE} is t_{CYCLE1} (SCK cycle time).

NAPXA4…0-NAP Exit Phase A. This field specifies the number of SCK cycles during the first phase for exiting NAP Mode.
NAPXA × $t_{SCYCLE} \geq t_{NAPXA,MAX}$. Do not set this field to 0.

NAPX4…0-NAP Exit Phase B. This field specifies the number of SCK cycles during the second phase for exiting NAP Mode.
NAPX × $t_{SCYCLE} \geq$ NAPXA × $t_{SCYCLE} + t_{NAPXB,MAX}$. Do not set this field to 0.

DQS-DQ Select. This field specifies the number of SCK cycles (0 → 0.5 cycles, 1 → 1.5 cycles) between the CMD pin framing sequence and the device selection on DQ5…0. See Figure 35-This field must be written with a "1" for this RDRAM.

Control Register: PDNXA — Address: 046_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	PDNXA5…0					

Read/write register.
Reset value is undefined.
PDNXA4…0-PDX Exit Phase A. This field specifies the number of (64 × SCK cycle) units during the first phase for exiting PDN mode. It must satisfy:
PDNXA × 64 × $t_{SCYCLE} \geq t_{PDNXA,MAX}$
Do not set this field to 0.
Note-only PDNXA5…0 are implemented.
Note-t_{SCYCLE} is t_{CYCLE1} (SCK Cycle time).

Control Register: PDNX — Address: 047_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	PDNX2…0		

Read/write register.
Reset value is undefined.
PDNX4…0-PDX Exit Phase A plus B. This field specifies the number of (256 × SCK cycle) units during the first plus second phase for exiting PDN mode. It must satisfy:

PDNX × 256 × $t_{SCYCLE} \geq$ PDNXA × 64 × $t_{SCYCLE} + t_{PDNXB,MAX}$

If this equation can't be satisfied, then the maximum PDNX value should be written, and the tS4/tH4 timing window will be modified (see Figure 35).
Do not set this field to 0.
Note-only PDNX2…0 are implemented.
Note-t_{SCYCLE} is t_{CYCLE1} (SCK Cycle time).

Figure 29. Control Registers

Control Register: TPARM — Address: 048_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	TCDLY0			TCLS		TCAS	

Read/write register.
Reset value is undefined.

TCAS1…0-Specifies the t_{CAS-C} core parameter in t_{CYCLE} units. This should be “10” (2 t_{CYCLE}).

TCLS1…0-Specifies the t_{CLS-C} core parameter in t_{CYCLE} units. This should be “10” (2 t_{CYCLE}).

TCDLY0-Specifies the $t_{CDLY0-C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to Q (read data) packets, permitting round trip read delay to all devices to be equalized. This field may be written with the values “010” (2 · t_{CYCLE}) through “101” (5 · t_{CYCLE}).

The equations relating the core parameters to the datasheet parameters follow:

$t_{CAS-C} = 2\ t_{CYCLE}$
$t_{CLS-C} = 2\ t_{CYCLE}$
$t_{CPS-C} = 1\ t_{CYCLE}$ Not programmable

$t_{OFFP} = t_{CPS-C} + t_{CAS-C} + t_{CLS-C} - 1\ t_{CYCLE}$
$= 4\ t_{CYCLE}$

$t_{RCD} = t_{RCD-C} + 1\ t_{CYCLE} - t_{CLS-C}$
$= t_{RCD-C} - 1\ t_{CYCLE}$

$t_{CAC} = 3 \cdot t_{CYCLE} + t_{CLS-C} + t_{CDLY0-C} + t_{CDLY1-C}$
(see table below for programming ranges)

TCDLY0	$t_{CDLY0-C}$	TCDLY1	$t_{CDLY0-C}$	t_{CAC}@t_{CYCLE} = 3.3 ns	t_{CAC}@t_{CYCLE} = 2.5 ns
010	2 · t_{CYCLE}	000	0 · t_{CYCLE}	7 · t_{CYCLE}	not allowed
011	3 · t_{CYCLE}	000	0 · t_{CYCLE}	8 · t_{CYCLE}	8 · t_{CYCLE}
011	3 · t_{CYCLE}	001	1 · t_{CYCLE}	9 · t_{CYCLE}	9 · t_{CYCLE}
011	3 · t_{CYCLE}	010	2 · t_{CYCLE}	10 · t_{CYCLE}	10 · t_{CYCLE}
100	4 · t_{CYCLE}	010	2 · t_{CYCLE}	11 · t_{CYCLE}	11 · t_{CYCLE}
101	5 · t_{CYCLE}	010	2 · t_{CYCLE}	12 · t_{CYCLE}	12 · t_{CYCLE}

Control Register: TFRM — Address: 049_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TFRM3…0			

Read/write register.
Reset value is undefined.

TFRM3…0-Specifies the position of the framing point in t_{CYCLE} units. This value must be greater than or equal to the $t_{FRM,MIN}$ parameter. This is the minimum offset between a ROW packet (which places a device at ATTN) and the first COL packet (directed to that device) which must be framed. This field may be written with the values “0111” (7 · t_{CYCLE}) through “1010” (10 · t_{CYCLE}). TFRM is usually set to the value which matches the largest $t_{RCD,MIN}$ parameter (modulo 4 · t_{CYCLE}) that is present in an RDRAM in the memory system. Thus, if an RDRAM with $t_{RCD,MIN}$ = 11 · t_{CYCLE} were present, then TFRM would be programmed to 7 t_{CYCLE}.

Control Register: TCDLY1 — Address: $04a_{16}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCDLY1	

Read/write register.
Reset value is undefined.

TCDLY1-Specifies the value of the $t_{CDLY1-C}$ core parameter in t_{CYCLE} units. This adds a programmable delay to Q (read data) packets, permitting round trip read delay to all devices to be equalized. This field may be written with the values “000” (0 t_{CYCLE}) through “010” (2 t_{CYCLE}). Refer to table above for more details.

Figure 30. Control Registers

Control Register: SKIP	Address: $04b_{16}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	AS	MSE	MS	0	0	0	0	0	0	0	0	0	0

Read/write register (except AS field).
Reset value is zero (SIO Reset).

AS-Autoskip. Read-only value determined by autoskip circuit and stored when SETF serial command is received by RDRAM during initialization. In Figure 46, AS = 1 corresponds to the early Q (a1) packet and AS = 0 to the Q (a1) packet one t_{CYCLE} later for the four uncertain cases.

MSE-Manual skip enable (0 = auto, 1 = manual).

MS-Manual skip (MS must be 1 when MSE = 1). During initialization, the RDRAMs at the furthest point in the fifth read domain may have selected the AS = 0 value, placing them at the closest point in a sixth read domain. Setting the MSE/MS fields to 1/1 overrides the autoskip value and returns them to the furthest point of the fifth read domain.

Control Register: TCYCLE	Address: $04c_{16}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	TCYCLE5…0					

Read/write register.
Reset value is undefined.

TCYCLE5…0-Specifies the value of the t_{CYCLE} datasheet parameter in 64 ps units. For the $t_{CYCLE,MIN}$ of 2.5 ns (2500 ps), this field should be written with the value "00027_{16}" (39*64 ps).

Control Register: TEST77	Address: $04d_{16}$
Control Register: TEST78	Address: $04e_{16}$
Control Register: TEST79	Address: $04f_{16}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/write register.

Reset value of TEST78, 79 is zero (SIO Reset).

Do not read or write TEST78, 79 after SIO reset. TEST77 must be written with zero after SIO reset. These registers must only be used for testing purposes.

Figure 31. Control Registers

Power State Management

Table 15 summarizes the power states available to a Direct RDRAM. In general, the lowest-power states have the longest operational latencies. For example, the relative power levels of PDN state and STBY have a ratio of about 1:110, and the relative access latencies to get read data have a ratio of about 250:1.

PDN state is the lowest power state available. The information in the RDRAM core is maintained with self-refresh; an internal timer automatically refreshes all rows of all banks. PDN has a relatively long exit latency because the TCLK/RCLK block must resynchronize itself to the external clock signal.

NAP state is another low-power state in which either self-refresh or REFA-refresh are used to maintain the core. See "Refresh" on page 51 for a description of the two refresh mechanisms. NAP state has a shorter exit latency than PDN because the TCLK/RCLK block maintains its synchronization state relative to the external clock signal. This imposes a limit (t_{NLIMIT}) on how long an RDRAM may remain in NAP state before briefly returning to STBY or ATTN to update this synchronization state.

Table 15. Power State Summary

Power State	Description	Blocks Consuming Power	Power State	Description	Blocks Consuming Power
PDN	Powerdown state.	Self-refresh	NAP	Nap state. Similar to PDN state except for lower wake-up latency	Self-refresh or REFA-refresh TCLK/RCLK-Nap
STBY	Standby state Ready for ROW packets.	REFA-refresh TCLK/RCLK ROW demux receiver	ATTN	Attention state Ready for ROW and COL packets	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver
ATTNR	Attention Read state Ready for ROW and COL packets. Sending Q (read data) packets	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ mux transmitter Core power	ATTNW	Attention Write state Ready for ROW and COL packets Ready for D (write data) packets	REFA-refresh TCLK/RCLK ROW demux receiver COL demux receiver DQ demux receiver Core power

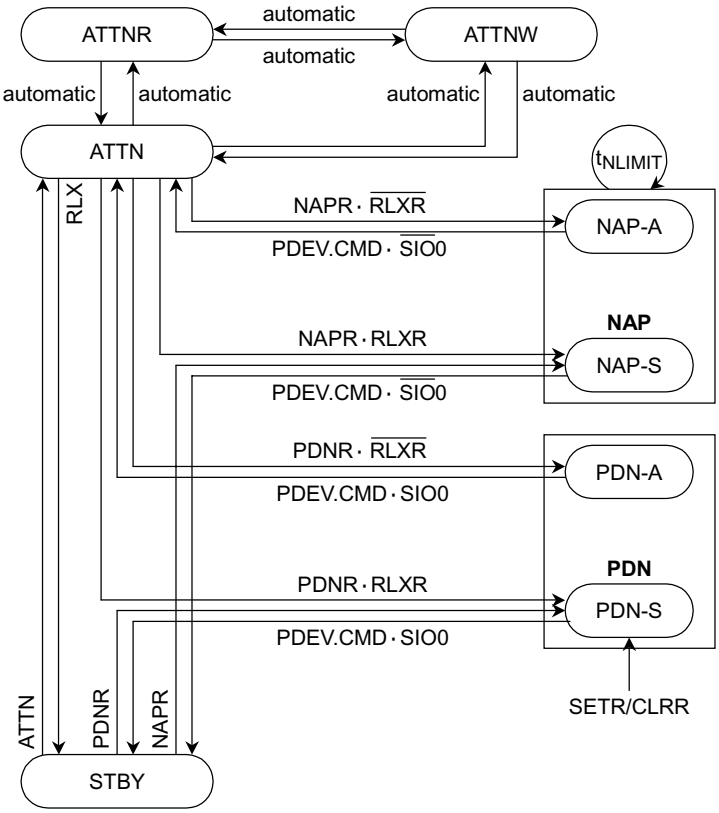
Figure 32 summarizes the transition conditions needed for moving between the various power states.

Note that NAP and PDN have been divided into two sub-states (NAP-A/NAP-S and PDN-A/PDN-S) to account for the fact that a NAP or PDN exit may be made to either ATTN to STBY states.

At initialization the SETR/CLRR Reset sequence will put the RDRAM into PDN-S state. The PDN exit sequence involves an optional PDEV specification and bits on the CMD and SIO0 pins.

Once the RDRAM is in STBY, it will move to the ATTN/ATTNR/ATTNW state when it receives a non-broadcast ROWR packet with the ATTN command. The RDRAM returns to STBY from these three states when it receives a RLX command. Alternatively, it may enter NAP or PDN state from ATTN or STBY states with a NAPR or PDNR command in an ROWR packet. The PDN or NAP exit sequence involves an optional PDEV specification and bits on the CMD and SIO0 pins. The RDRAM returns to the ATTN or STBY state it was originally in when it first entered NAP or PDN.

An RDRAM may only remain in NAP state for a time t_{NLIMIT}. It must periodically return to ATTN or STBY.



Notation:

SETR/CLRR-SETR/CLRR Reset sequence in SRQ packets
PDNR-PDNR command in ROWR packet
NAPR-NAPR command in ROWR packet
RLXR-RLX command in ROWR packet
RLX-RLX command in ROWR, COLC or COLX packet
ROW-ROWA packet or POWR packet (non-broadcast)
PDEV.CMD-(PDEV = DEVID) · (CMD = 01)
SIO0-SIO0 input value
ATTN-ROWA packet (non-broadcast) or ROWR packet (non-broadcast) with ATTN command

Figure 32. Power State Transition Diagram

The NAPRC command causes a nap-down operation if the RDRAM's NCBIT is set. The NCBIT is not directly visible. It is undefined on reset. It is set by a NAPR command to the RDRAM and it is cleared by an ACT command to the RDRAM. It permits a controller to manage a set of RDRAMs in a mixture of power states.

STBY state is the normal idle state of the RDRAM. In this state all banks and sense amps have usually been left precharged and ROWA and ROWR packets on the ROW pins are being monitored. When a non-broadcast ROWA packet or non-broadcast ROWR packet (with the ATTN command) addressed to the RDRAM is seen, the RDRAM enters ATTN state (see the right-hand side of Figure 33).

This requires t_{SA} during which time the RDRAM activates the specified row of the specified bank. A time TFRM t_{CYCLE} after the ROW packet, the RDRAM will be able to frame COL packets (TFRM is a control register field-see Figure 30). Once in ATTN state, the RDRAM will automatically transition to the ATTNW and ATTNR states as it receives WR and RD commands.

Once the RDRAM is in ATTN, ATTNW or ATTNR states, it will remain there until it is explicitly returned to the STBY state with an RLX command. An RLX command may be given in an ROWR, COLC or COLX packet (see the left-hand side of Figure 33). It is usually given after all banks of the RDRAM have been precharged; if other banks are still activated, then the RLX command would probably not be given. If a broadcast ROWA packet (with the ATTN command) is received, the RDRAM's power state doesn't change. If a broadcast ROWR packet with RLXR command is received, the RDRAM goes to STBY.

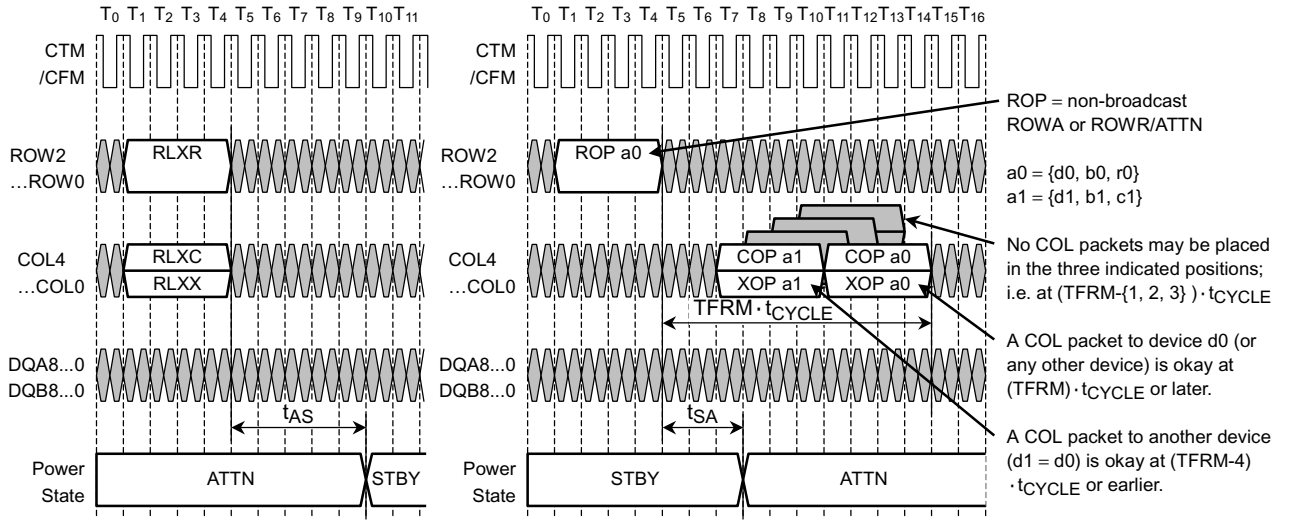
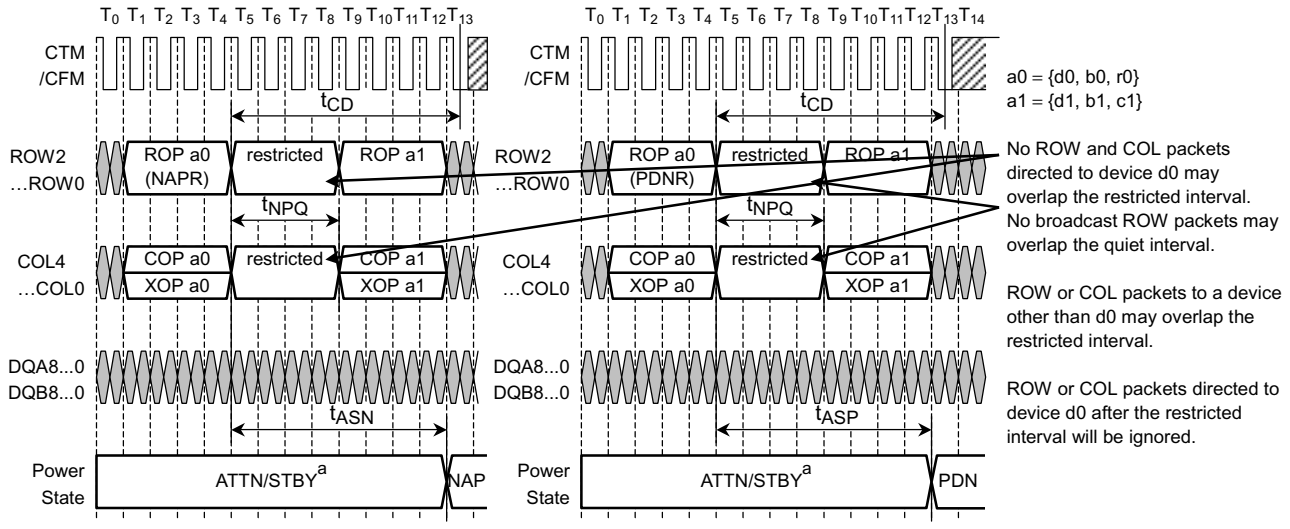


Figure 33. STBY Entry (left) and STBY Exit (right)

Figure 34 shows the NAP entry sequence (left). NAP state is entered by sending a NAPR command in a ROW packet. t_{ASN} is required to enter NAP state (this specification is provided for power calculation purposes). The clock on CTM/CFM must remain stable for t_{CD} after the NAPR command.



a. The (eventual) NAP/PDN exit will be to the same ATTN/STBY state the RDRAM was in prior to NAP/PDN entry

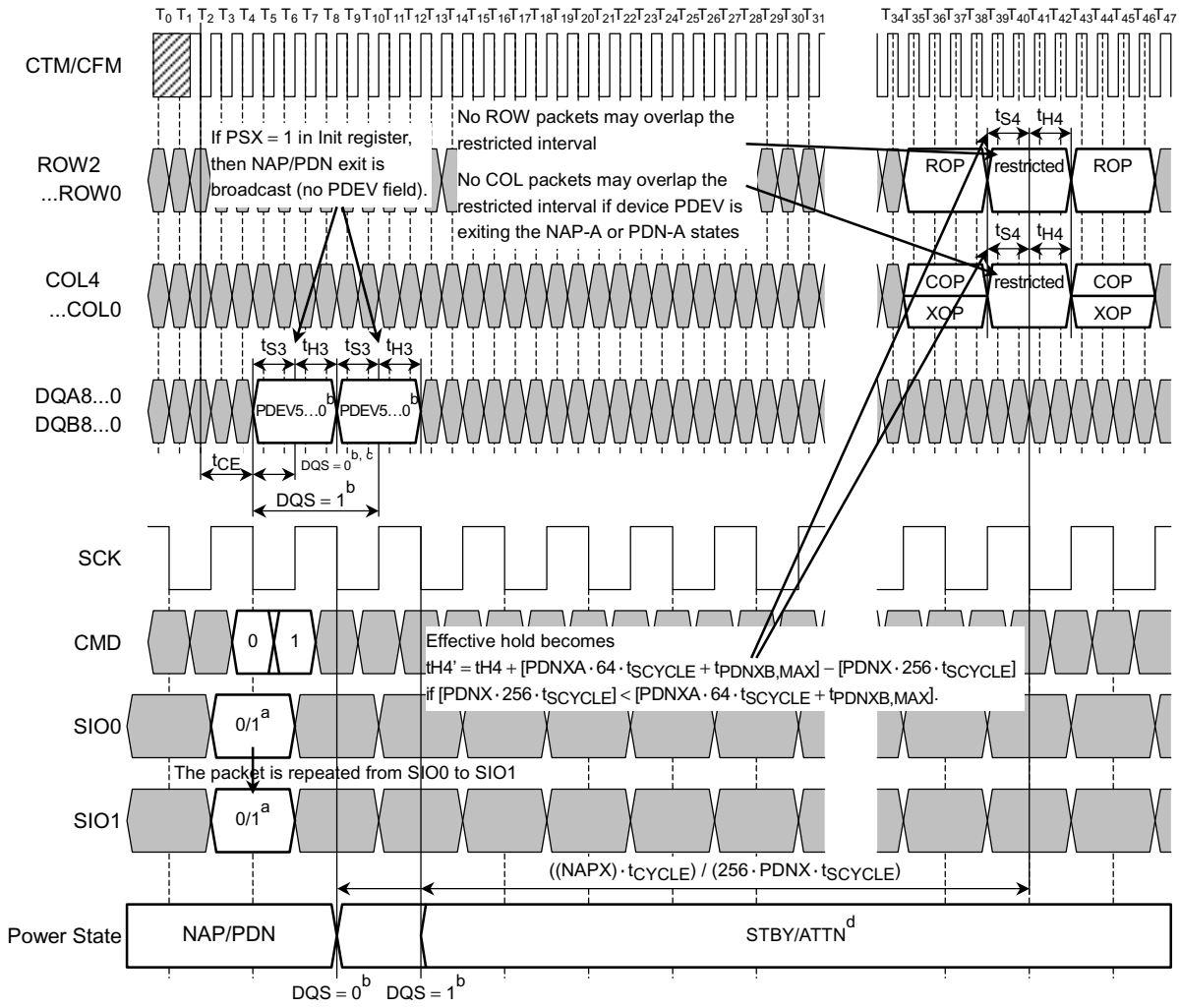
Figure 34. NAP Entry (left) and PDN Entry (right)

The RDRAM may be in ATTN or STBY state when the NAPR command is issued. When NAP state is exited, the RDRAM will return to the original starting state (ATTN or STBY). If it is in ATTN state and an RLXR command is specified with a NAPR, the RDRAM will return to STBY state when NAP is exited.

Figure 34 also shows the PDN entry sequence (right). PDN state is entered when a PDNR command in a ROW packet. t_{ASP} is required to enter PDN state (this specification is provided for power calculation purposes). The clock on CTM/CFM must remain stable for a t_{CD} after the PDNR command.

The RDRAM may be in ATTN or STBY state when the PDNR command is issued. When PDN state is exited, the RDRAM will return to the original starting state (ATTN or STBY). If it is in ATTN state and an RLXR command is specified with a PDNR, then the RDRAM will return to STBY state when PDN is exited. The current-and slew-rate-control levels are re-established.

The RDRAM's write buffer must be retired with the appropriate COP command before NAP or PDN are entered. Also, all the RDRAM's banks must be precharged before NAP or PDN are entered. The exception to this is if NAP is entered with the NSR bit of the INIT register cleared (disabling self-refresh in NAP). The commands for relaxing, retiring, and precharging may be given to the RDRAM as late as the ROPa0, COPa0, and XOPa0 packets in Figure 34. No broadcast packets nor packets directed to the RDRAM entering NAP or PDN may overlay the quiet window. This window extends for a time t_{NPQ} after the packet with the NAPR or PDNR command.



a: Use 0 for NAP exit, 1 for PDN exit.

b: Device selection timing slot is selected by DQS field of NAPX register.

c: The DQS field must be written with "1" for this RDRAM.

d: Exit to STBY or ATTN depends upon whether RLXR was asserted at NAP or PDN entry time

Figure 35. NAP and PDN Exit

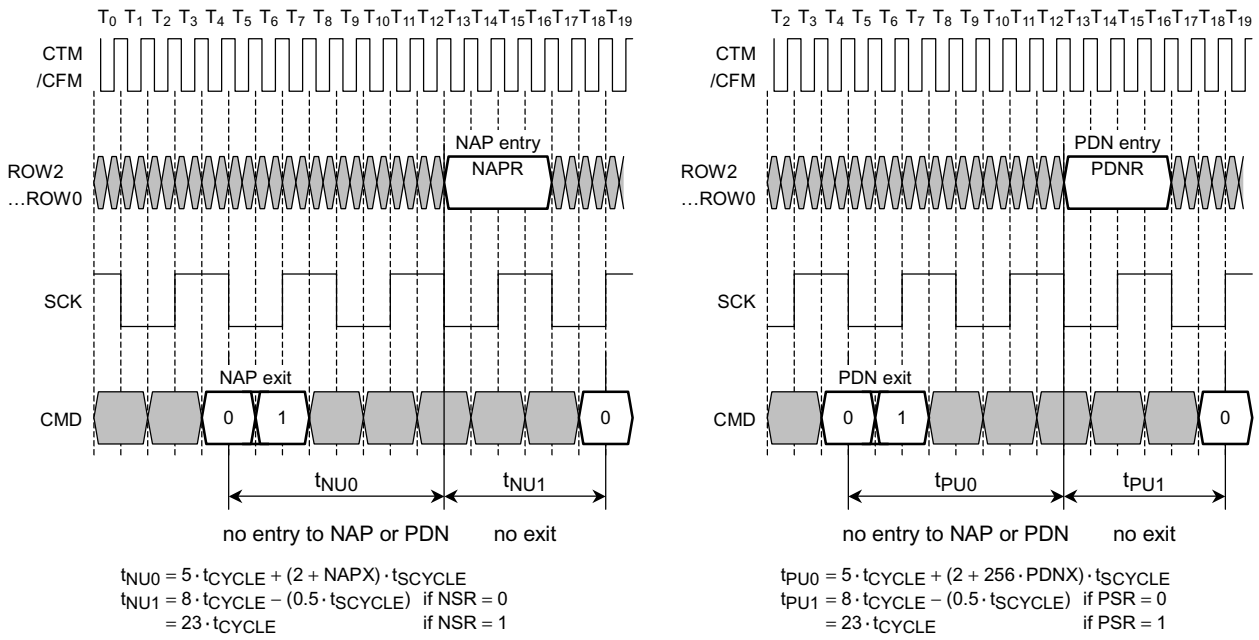


Figure 36. NAP Entry/Exit Windows (left) and PDN Entry/Exit Window (right)

Figure 35 shows the NAP and PDN exit sequences. These sequence are virtually identical; the minor differences will be highlighted in the following description.

Before a NAP or PDN exit, the CTM/CFM clock must be stable for a time t_{CE}. Then, on a falling and rising edge of SCK, if there is a "01" on the CMD input, NAP or PDN state will be exited. Also, on the falling SCK edge the SIO0 input must be 0 for a NAP exit and 1 for a PDN exit.

If the PSX bit of the INIT register is 0, then a device PDEV5…0 is specified for the NAP or PDN exit on the DQA5…0 pins. This value is driven on the rising SCK edge 0.5 or 1.5 SCK cycles after the original falling edge, depending upon the value of the DQS bit of the NAPX register. If the PSX bit of the INIT register is 1, then the RDRAM ignores the PDEV5…0 address packet and exits NAP or PDN when the wake-up sequence is presented on the CMD wire.

The ROW and COL pins must be quiet at t_{S4}/t_{H4} around the indicated falling SCK edge (timed with the PDNX or NAPX register fields). After that, ROW and COL packets may be directed to the RDRAM which is now in ATTN or STBY state.

Figure 36 shows the constraints for entering and exiting NAP and PDN states. On the left side, a RDRAM exits NAP state at the end of cycle T_4. This RDRAM may not re-enter NAP or PDN state for an interval of t_{NU0}. The RDRAM enters NAP state at the end of cycle T_{12}. This RDRAM may not re-exit NAP state for an interval of t_{NU1}. The equations for these two parameters depend upon a number of factors, and are shown at the bottom of the figure. NAPX is the value in the NAPX field in the NAPX register.

On the right side of Figure 36, a RDRAM exits PDN state at the end of cycle T_4. This RDRAM may not re-enter PDN or NAP state for an interval of t_{PU0}. The RDRAM enters PDN state at the end of cycle T_{12}. This RDRAM may not re-exit PDN state for an interval of t_{PU1}. This equations for these two parameters depend upon a number of factors, and are shown at the bottom of the figure. PDNX is the value in the PDNX field in the PDNX register.

Refresh

RDRAMs, like any other DRAM technology, use volatile storage cells which must be periodically refreshed. This is accomplished with the REFA command. Figure 37-(1) shows an example of this.

The REFA command in the transaction is typically a broadcast command (DR4T and DR4F are both set in the ROWR packet), so that in all devices bank number Ba is activated with row number REFR, where REFR is a control register in the RDRAM. When the command is broadcast and ATTN is set, the power state of the RDRAMs (ATTN or STBY) will remain unchanged. The controller increments the bank address Ba for the next REFA command. When Ba is equal to its maximum value, the RDRAM automatically increments REFR for the next REFA command.

On average, these REFA command are sent once every $t_{REF}/2^{BBIT + RBIT}$ (where BBIT are the number of bank address bits and RBIT are the number of row address bits) so that each row of each bank is refreshed once every t_{REF} interval.

The REFA command is equivalent to an ACT command, in terms of the way that it interacts with other packets (see Table 8). In the example, an ACT command is sent after t_{RR} to address b0, a different (non-adjacent) bank than the REFA command.

A second ACT command can be sent after t_{RC} to address c0, the same bank (or an adjacent bank) as the REFA command.

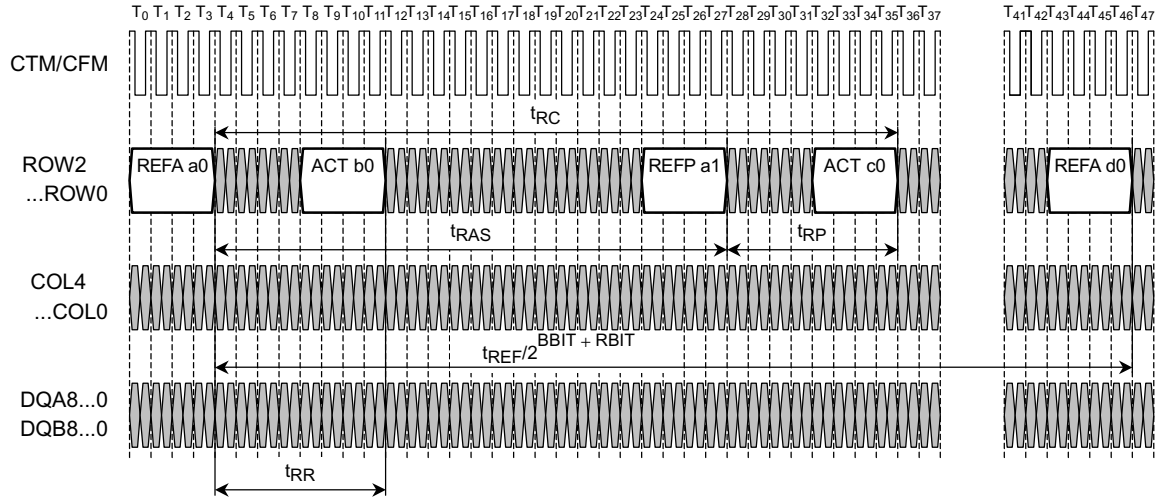
Note that a broadcast REFP command is issued t_{RAS} after the initial REFA command in order to precharge the refreshed bank in all RDRAMs. After a bank is given a REFA command, no other core operations (active or precharge) should be issued to it until it receives a REFP.

It is also possible to interleave refresh transactions (is not shown). In the figure, the ACT b0 command would be replaced by a REFA b0 command. The b0 address would be broadcast to all devices, and would be {Broadcast, Ba + 2, REFR}. Note that the bank address should skip by two to avoid adjacent bank interference. A possible bank incrementing pattern would be: {13, 11, 9, 7, 5, 3, 1, 8, 10, 12, 14, 0, 2, 4, 6, 15, 29, 27, 25, 23, 21, 19, 17, 24, 26, 28, 30, 16, 18, 20, 22, 31}. Every time bank 31 is reached, the REFA command would automatically increment the REFR register.

A second refresh mechanism is available for use in PDN and NAP power states. This mechanism is called Self-Refresh Mode. When the PDN power state is entered, or when NAP power state is entered with the NSR control register bit set, then Self-Refresh is automatically started for the RDRAM.

Self-Refresh uses an internal time base reference in the RDRAM. This causes an activate and precharge to be carried out once in every $t_{REF}/2^{BBIT + RBIT}$ interval. The REFB and REFR control registers are used to keep track of the bank and row being refreshed.

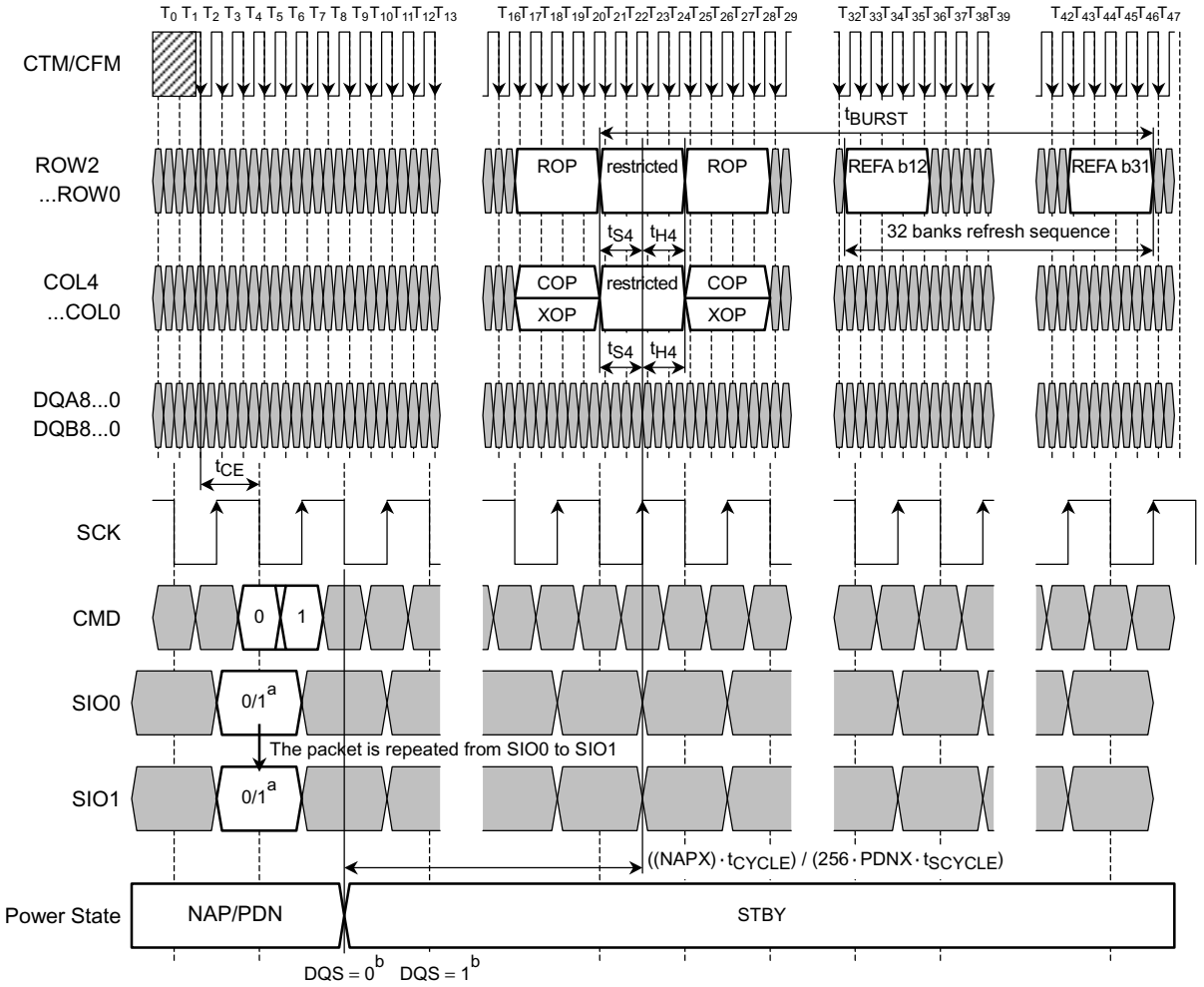
Before a controller places a RDRAM into Self-Refresh Mode, it should perform REFA/REFP refreshes until the bank address is equal to the maximum value. This ensures that no rows are skipped. Likewise, when a controller returns a RDRAM to REFA/REFP refresh, it should start with the minimum bank address value (zero).



Transaction a: REFA	a0 = {Broadcast, Ba, REFR}	a1 = {Broadcast, Ba}
Transaction b: xx	b0 = {Db, / = {Ba, Ba + 1, Ba – 1}, Rb}	
Transaction c: xx	c0 = {Dc, = = Ba, Rc}	
Transaction d: REFA	d0 = {Broadcast, Ba + 1, REFR}	

BBIT = # bank address bits
RBIT = # row address bits
REFB = REFB4…REFB0
REFR = REFR8…REFR0

Figure 37 - (1). REFA/REFP Refresh Transaction Example



a: Use 0 for NAP exit, 1 for PDN exit.

b: Device selection timing slot is selected by DQS field of NAPX register.

Figure 37 - (2). NAP/PDN Exit–t_{BURST} Requirement

Current and Temperature Control

Figure 38 shows an example of a transaction which performs current control calibration. It is necessary to perform this operation once to every RDRAM in every t_{CCTRL} interval in order to keep the I_{OL} output current in its proper range.

The example uses four COLX packets with a CAL command. These cause the RDRAM to drive four calibration packets Q (a0) a time t_{CAC} later. An offset of $t_{READTOCC}$ must be placed between the Q (a0) packet and read data Q (a1) from the same device. These calibration packets are driven on the DQA4…3 and DQB4…3 wires. The TSQ bit of the INIT register is driven on the DQA5 wire during same interval as the calibration packets. The remaining DQA and DQB wires are not used during these calibration packets. The last COLX packet also contains a SAM command (concatenated with the CAL command). The RDRAM samples the last calibration packet and adjusts its I_{OL} current value.

Unlike REF commands, CAL and SAM commands cannot be broadcast. This is because the calibration packets from different devices would interfere. Therefore, a current control transaction must be sent every t_{CCTRL}/N, where N is the number of RDRAMs on the Channel. The device field Da of the address a0 in the CAL/SAM command should be incremented after each transaction.

Figure 39 shows an example of a temperature calibration sequence to the RDRAM. This sequence is broadcast once every t_{TEMP} interval to all the RDRAMs on the Channel. The TCEN and TCAL are ROP commands, and cause the slew rate of the output drivers to adjust for temperature drift. During the quiet interval $t_{TCQUIET}$ the devices being calibrated can't be read, but they can be written.

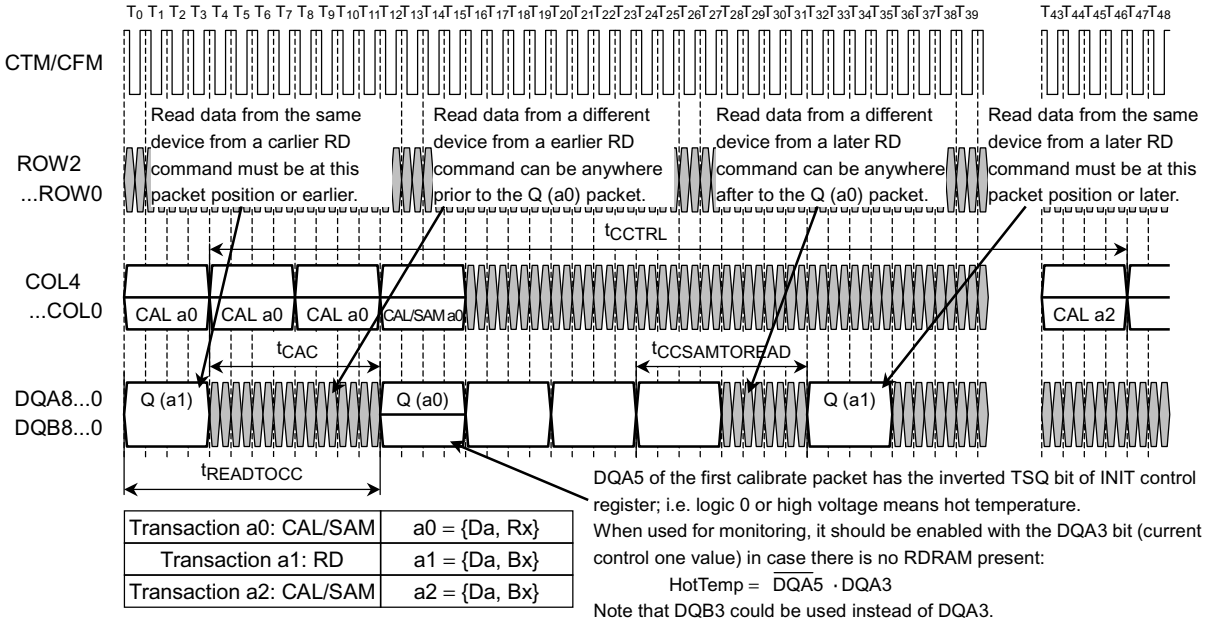


Figure 38. Current Control CAL/SAM transaction Example

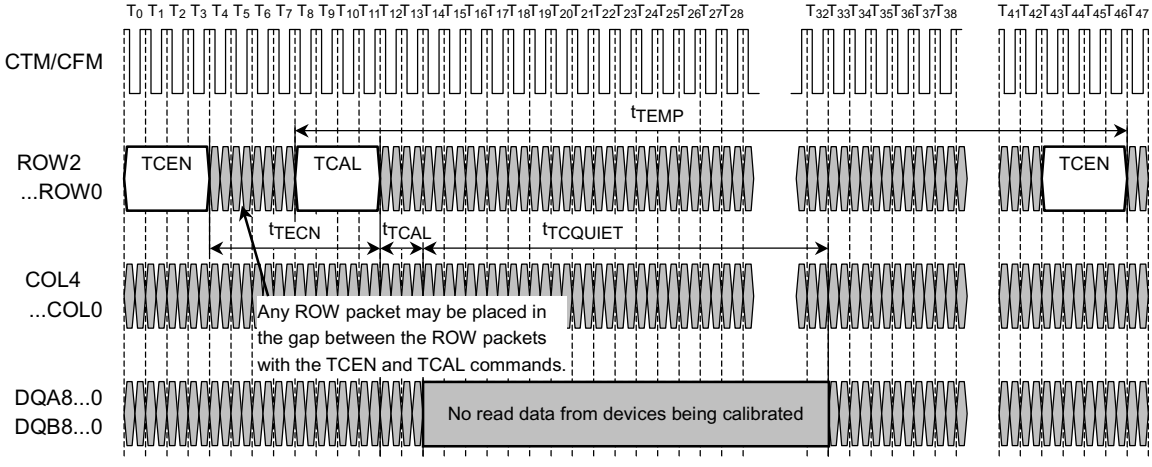


Figure 39. Temperature Calibration (TCEN-TCAL) Transitions to RDRAM

Electrical Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_J	Junction temperature under bias	TBD	TBD	°C
V_{DD}, V_{DDA}	Supply voltage	2.50 – 0.13	2.50 + 0.13	V
$V_{DD,N}$, $V_{DDA,N}$	Supply voltage droop (DC) during NAP interval (t_{NLIMIT})	—	2.0	%
$v_{DD,N}$, $v_{DDA,N}$	Supply voltage ripple (AC) during NAP interval (t_{NLIMIT})	–2.0	2.0	%
V_{CMOS}[a]	Supply voltage for CMOS pins (2.5 V controllers)	V_{DD}	V_{DD}	V
	Supply voltage for CMOS pins (1.8 V controllers)	1.80 – 0.1	1.80 + 0.2	V
V_{REF}	Reference voltage	1.40 – 0.2	1.40 + 0.2	V
V_{DIL}	RSL data input — low voltage	V_{REF} – 0.5	V_{REF} – 0.2	V
V_{DIH}	RSL data input — high voltage[b]	V_{REF} + 0.2	V_{REF} + 0.5	V
R_{DA}	RSL data asymmetry: $R_{DA} = (V_{DIH} - V_{REF}) / (V_{REF} - V_{DIL})$	0.67	1.0	—
V_{CM}	RSL clock input — common mode $V_{CM} = (V_{CIH} + V_{CIL}) / 2$	1.3	1.8	V
$V_{CIS,CTM}$	RSL clock input swing: $V_{CIS} = V_{CIH} - V_{CIL}$ (CTM, CTMN pins)	0.35	1.0	V
$V_{CIS,CFM}$	RSL clock input swing: $V_{CIS} = V_{CIH} - V_{CIL}$ (CFM, CFMN pins)	0.225	1.0	V
$V_{IL,CMOS}$	CMOS input low voltage	–0.3[c]	$V_{CMOS}/2$ – 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	$V_{CMOS}/2$ + 0.25	V_{CMOS} + 0.3[d]	V

a. V_{CMOS} must remain on as long as V_{DD} is applied and cannot be turned off.
b. V_{DIH} is typically equal to V_{TERM} (1.8 V ± 0.1 V) under DC conditions in a system.
c. Voltage undershoot is limited to –0.7 V for a duration of less than 5 ns.
d. Voltage overshoot is limited to V_{CMOS} + 0.7 V for a duration of less than 5 ns.

Timing Conditions

SYMBOL	PARAMETER		MIN	MAX	UNIT	Figure (s)
t_{CYCLE}	CTM and CFM Cycle times	-600	3.33	3.83	ns	Figure 40
		-711	2.80	3.83		
		-800	2.50	3.83		
t_{CR}, t_{CF}	CTM and CFM input rise and fall times		0.2	0.5	ns	Figure 40
t_{CH}, t_{CL}	CTM and CFM high and low times		40%	60%	t_{CYCLE}	Figure 40
t_{TR}	CTM-CFM differential (MSE/MS = 0/0)		0.0	1.0	t_{CYCLE}	Figure 31
	CTM-CFM differential (MSE/MS = 1/1)[a]		0.9	1.0	t_{CYCLE}	Figure 40
t_{DCW}	Domain crossing window		–0.1	0.1	t_{CYCLE}	Figure 46
t_{DR}, t_{DF}	DQA/DQB/ROW/COL input rise/fall times		0.2	0.65	ns	Figure 41
t_S, t_H	DQA/DQB/ROW/COL-to-CFM Set-up/Hold	@t_{CYCLE} = 3.33 ns	0.275[b, d]	—	ns	Figure 41
		@t_{CYCLE} = 2.81 ns	0.240[c, d]	—		
		@t_{CYCLE} = 2.50 ns	0.200[d]	—		
t_{DR1}, t_{DF1}	SIO0, SIO1 input rise and fall times		—	5.0	ns	Figure 43
t_{DR2}, t_{DF2}	CMD, SCK input rise and fall times		—	2.0	ns	Figure 43
t_{CYCLE1}	SCK Cycle time-Serial Control Register Transactions		1000	—	ns	Figure 43
	SCK Cycle time-Power Transactions		10	—	ns	Figure 43
t_{CH1}, t_{CL1}	SCK high and low times		4.25	—	ns	Figure 43

Timing Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT	Figure (s)
t_{S1}	CMD Set-up time to SCK rising or falling edge[e]	1.25	—	ns	Figure 43
t_{H1}	CMD Hold time to SCK rising or falling edge[e]	1	—	ns	Figure 43
t_{S2}	SIO0 Set-up time to SCK falling edge	40	—	ns	Figure 43
t_{H2}	SIO0 Hold time to SCK falling edge	40	—	ns	Figure 43
t_{S3}	PDEV Set-up time on DQA5…0 to SCK rising edge	0	—	ns	Figure 44
t_{H3}	PDEV Hold time on DQA5…0 to SCK rising edge	5.5	—	ns	Figure 44
t_{S4}	ROW2…0, COL4…0 Set-up time for Quiet Window	−1	—	t_{CYCLE}	Figure 35
t_{H4}	ROW2…0, COL4…0 Hold time for Quiet Window[f]	5	—	t_{CYCLE}	Figure 35
t_{NPQ}	Quiet on ROW/COL bits during NAP/PDN entry	4	—	t_{CYCLE}	Figure 34
$t_{READTOCC}$	Offset between read data and CC packets (same device)	12	—	t_{CYCLE}	Figure 38
$t_{CCSAMTOREAD}$	Offset between CC packets and read data (same device)	8	—	t_{CYCLE}	Figure 38
t_{CE}	CTM/CFM stable before NAP/PDN exit	2	—	t_{CYCLE}	Figure 35
t_{CD}	CTM/CFM stable after NAP/PDN entry	100	—	t_{CYCLE}	Figure 34
t_{FRM}	ROW packet to COL packet ATTN framing delay	7	—	t_{CYCLE}	Figure 33
t_{NLIMIT}	Maximum time in NAP Mode	—	10.0	µs	Figure 32
t_{REF}	Refresh Interval	—	32	ms	Figure 37-(1)
t_{BURST}	Interval after PDN or NAP (with self-refresh) exit in which all banks of the RDRAM must be refreshed at least once.	—	200	µs	Figure 37-(2)
t_{CCTRL}	Current Control Interval	34 t_{CYCLE}	100 ms	ms/t_{CYCLE}	Figure 38
t_{TEMP}	Temperature Control Interval	—	100	ms	Figure 39
t_{TCEN}	TCE command to TCAL command	150	—	t_{CYCLE}	Figure 39
t_{TCAL}	TCAL command to quiet window	2	2	t_{CYCLE}	Figure 39
$t_{TCQUIET}$	Quiet window (no read data)	140	—	t_{CYCLE}	Figure 39
t_{PAUSE}	RDRAM Delay (no RSL operations allowed)	—	200.0	µs	page 36

a. MSE/MS are fields of the SKIP register. For this combination (skip override) the t_{DCW} parameter range is effectively 0.0 to 0.0.
b. This parameter also applies to a -800 or -711 part when operated with t_{CYCLE} = 3.33 ns.
c. This parameter also applies to a -800 part when operated with t_{CYCLE} = 2.81 ns.
d. $t_{S,MIN}$ and $t_{H,MIN}$ for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 3 specified t_{CYCLE} values.
e. With $V_{IL,CMOS} = 0.5\ V_{CMOS} - 0.4$ V and $V_{IH,CMOS} = 0.5\ V_{CMOS} + 0.4$ V
f. Effective setup becomes $t_{H4}' = t_{H4} + [PDNXA \cdot 64 \cdot t_{SCYCLE} + t_{PDNXB,MAX}] - [PDNX \cdot 256 \cdot t_{SCYCLE}]$ if $[PDNX \cdot 256 \cdot t_{SCYCLE}] < [PDNXA \cdot 64 \cdot t_{SCYCLE} + t_{PDNXB,MAX}]$. See Figure 35.

Electrical Characteristics

SYMBOL	PARAMETER AND CONDITIONS	MIN	MAX	UNIT
θ_{JC}	Junction-to-Case thermal resistance	—	TBD	°C/Watt
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	−10	10	μA
I_{OH}	RSL output high current @ ($0 \le V_{OUT} \le V_{DD}$)	−10	10	μA
I_{ALL}	RSL I_{OL} current @ V_{OL} = 0.9 $V_{DD,MIN}$, $T_{j,MAX}$ [a]	30	90	mA
ΔI_{OL}	RSL I_{OL} current resolution step	—	2.0	mA
r_{OUT}	Dynamic output impedance	150	—	Ω
$I_{OL,NOM}$	RSL I_{OL} current @ V_{OL} = 1.0 V [b, c]	26.6	30.6	mA
$I_{OL\_A01,NOM}$	RSL I_{OL} current @ V_{OL} = 0.9 V [b, d]	30.1	34.1	mA
$I_{I,CMOS}$	CMOS input leakage current @ ($0 \le V_{I,CMOS} \le V_{CMOS}$)	−10.0	10.0	μA
$V_{OL,CMOS}$	CMOS output voltage @ $I_{OL,CMOS}$ = 1.0 mA	—	0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$ = −0.25 mA	V_{CMOS} − 0.3	—	V

a. This measurement is made in manual current control mode; i.e. with all output device legs sinking current.
b. This measurement is made in automatic current control mode after at least 64 current control calibration operations to a device and after CCA and CCB are initialized to a value of 64. This value applies to all DQA and DQB pins.
c. This measurement is made in automatic current control mode in a 25 Ω test system with V_{TERM} = 1.714 V and V_{REF} = 1.357 V and with the ASYMA and ASYMB register fields set to 0.
d. This measurement is made in automatic current control mode in a 25 Ω test system with V_{TERM} = 1.714 V and V_{REF} = 1.357 V and with the ASYMA and ASYMB register fields set to 1.

Timing Characteristics

SYMBOL	PARAMETER AND CONDITIONS		MIN	MAX	UNIT	Figure (s)
t_Q	CTM-to-DQA/DQB output time	@t_{CYCLE} = 2.50 ns	−0.260 [c]	+0.260 [c]	ns	Figure 42
		@t_{CYCLE} = 2.81 ns	−0.300 [b, c]	+0.300 [b, c]		
		@t_{CYCLE} = 3.33 ns	−0.350 [a, c]	+0.350 [a, c]		
t_{QR}, t_{QF}	DQA/DQB output rise and fall time		0.2	0.45	ns	Figure 42
t_{Q1}	SCK (neg)-to-SIO0 Delay @ $C_{LOAD,MAX}$ = 20 pF (SD read data valid).		—	10	ns	Figure 45
t_{HR}	SCK(pos)-to-SIO0 Delay @ $C_{LOAD,MAX}$ = 20 pF (SD read data hold).		2	—	ns	Figure 45
t_{QR1}, t_{QF1}	SIO_{OUT} rise/fall @ $C_{LOAD,MAX}$ = 20 pF		—	5	ns	Figure 45
t_{PROP1}	SIO0-to-SIO1 or SIO1-to-SIO0 Delay @ $C_{LOAD,MAX}$ = 20 pF		—	10	ns	Figure 45
t_{NAPXA}	NAP Exit Delay-Phase A		—	50	ns	Figure 35
t_{NAPXB}	NAP Exit Delay-Phase B		—	40	ns	Figure 35
t_{PDNXA}	PDN Exit Delay-Phase A		—	4	μs	Figure 35
t_{PDNXB}	PDN Exit Delay-Phase B		—	9000	t_{CYCLE}	Figure 35
t_{AS}	ATTN-to-STBY Power State Delay		—	1	t_{CYCLE}	Figure 33
t_{SA}	STBY-to-ATTN Power State Delay		—	0	t_{CYCLE}	Figure 33
t_{ASN}	ATTN/STBY-to-NAP Power State Delay		—	8	t_{CYCLE}	Figure 34
t_{ASP}	ATTN/STBY-to-PDN Power State Delay		—	8	t_{CYCLE}	Figure 34

a. This parameter also applies to a -800 or -711 part when operated with t_{CYCLE} = 3.33 ns.
b. This parameters also applies to a -800 for part when operated with t_{CYCLE} = 2.81 ns.
c. $t_{Q,MIN}$ and $t_{Q,MAX}$ for other t_{CYCLE} values can be interpolated between or extrapolated from the timings at the 3 specified t_{CYCLE} values.

RSL Clocking

Figure 40 is a timing diagram which shows the detailed requirements for the RSL clock signals on the Channel.

The CTM and CTMN are differential clock inputs used for transmitting information on the DQA and DQB, outputs. Most timing is measured relative to the points where they cross. The t_{CYCLE} parameter is measured from the falling CTM edge to the falling CTM edge. The t_{CL} and t_{CH} parameters are measured from falling to rising and rising to falling edges of CTM. The t_{CR} and t_{CF} rise-and fall-time parameters are measured at the 20% and 80% points.

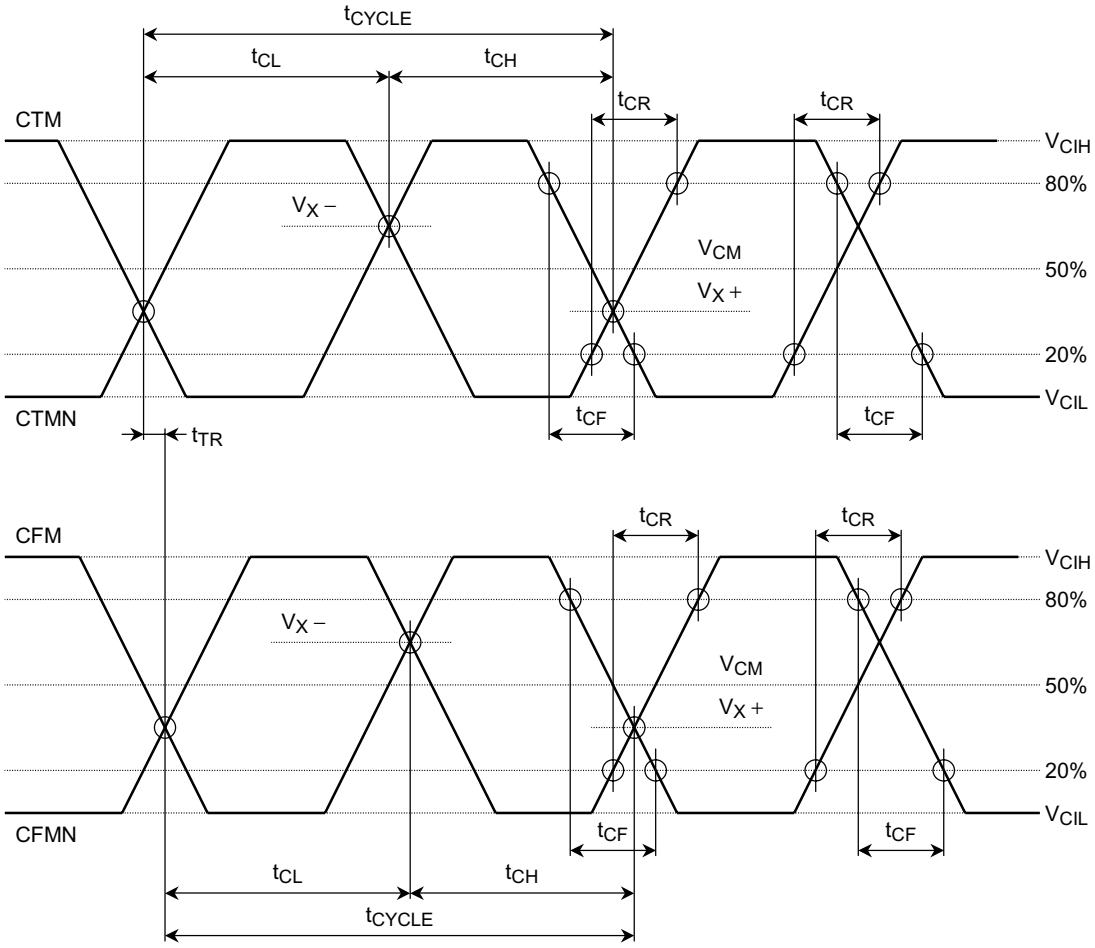


Figure 40. RSL Timing-Clock Signals

The CFM and CFMN are differential clock outputs used for receiving information on the DQA, DQB, ROW and COL outputs. Most timing is measured relative to the points where they cross. The t_{CYCLE} parameter is measured from the falling CFM edge to the falling CFM edge. The t_{CL} and t_{CH} parameters are measured from falling to rising and rising to falling edges of CFM. The t_{CR} and t_{CF} rise-and fall-time parameters are measured at the 20% and 80% points.

The t_{TR} parameter specifies the phase difference that may be tolerated with respect to the CTM and CFM differential clock inputs (the CTM pair is always earlier).

RSL-Receive Timing

Figure 41 is a timing diagram which shows the detailed requirements for the RSL input signals on the Channel.

The DQA, DQB, ROW, and COL signals are inputs which receive information transmitted by a Direct RAC on the Channel. Each signal is sampled twice per t_{CYCLE} interval. The set/hold window of the sample points is t_S/t_H. The sample points are centered at the 0% and 50% points of a cycle, measured relative to the crossing points of the falling CFM clock edge. The set and hold parameters are measured at the VREF voltage point of the input transition.

The t_{DR} and t_{DF} rise-and fall-time parameters are measured at the 20% and 80% points of the input transition.

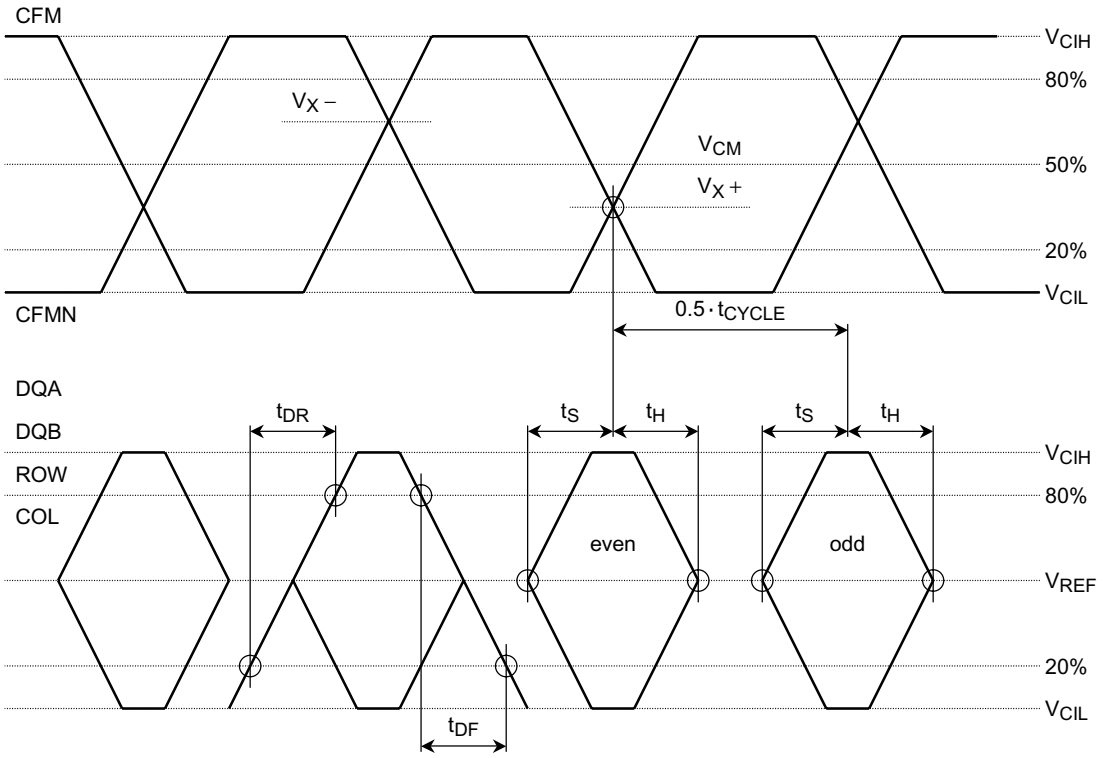


Figure 41. RSL Timing-Data Signals for Receive

RSL-Transmit Timing

Figure 42 is a timing diagram which shows the detailed requirements for the RSL output signals on the Channel.

The DQA and DQB signals are outputs to transmit information that is received by a Direct RAC on the Channel. Each signal is driven twice per t_{CYCLE} interval. The beginning and end of the even transmit window is at the 75% point of the previous cycle and at the 25% point of the current cycle. The beginning and end of the odd transmit window is at the 25% point and at the 75% point of the current cycle. These transmit points are measured relative to the crossing points of the falling CTM clock edge. The size of the actual transmit window is less than the ideal $t_{CYCLE}/2$, as indicated by the non-zero values of $t_{Q,MIN}$ and $t_{Q,MAX}$. The t_Q parameters are measured at the VREF voltage point of the output transition.

The t_{QR} and t_{QF} rise-and fall-time parameters are measured at the 20% and 80% points of the output transition.

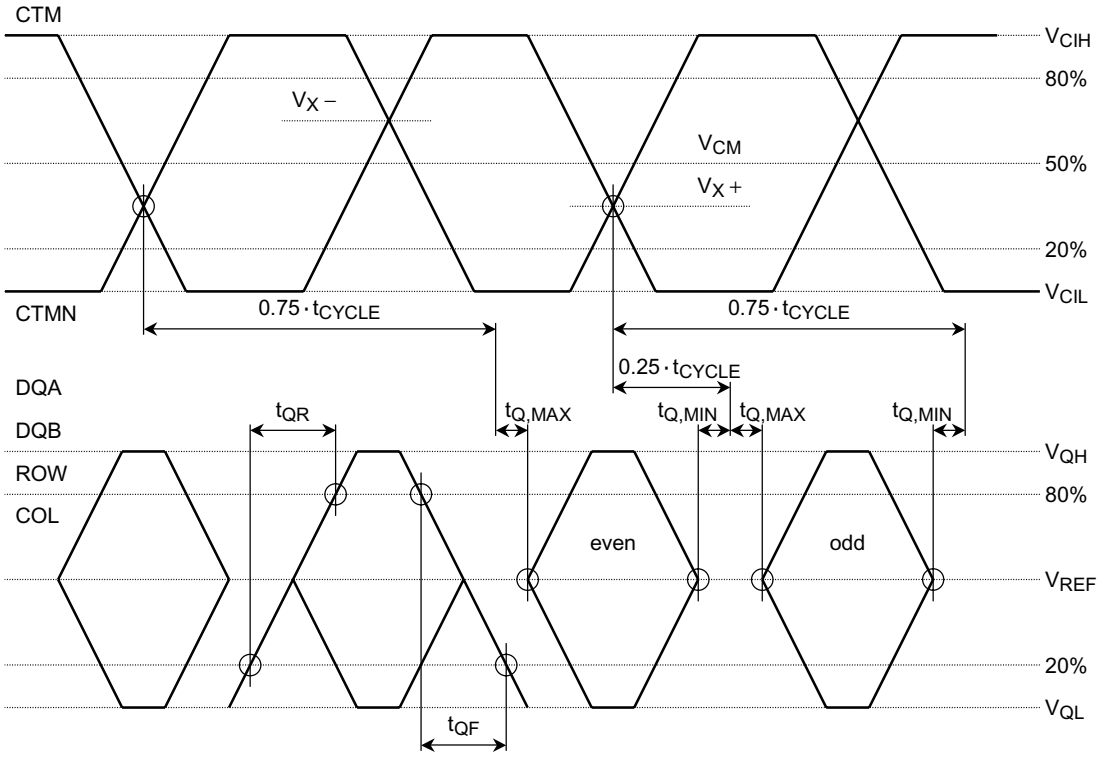


Figure 42. RSL Timing-Data Signals for Transmit

CMOS-Receive Timing

Figure 43 is a timing diagram which shows the detailed requirements for the CMOS input signals.

The CMD and SIO0 signals are inputs which receive information transmitted by a controller (or by another RDRAM's SIO1 output. SCK is the CMOS clock signal driven by the controller. All signals are high true.

The cycle time, high phase time, and low phase time of the SCK clock are t_{CYCLE1}, t_{CH1} and t_{CL1}, all measured at the 50% level. The rise and fall times of SCK, CMD, and SIO0 are t_{DR1} and t_{DF1}, measured at the 20% and 80% levels.

The CMD signal is sampled twice per t_{CYCLE1} interval, on the rising edge (odd data) and the falling edge (even data). The set/hold window of the sample points is t_{S1}/t_{H1}. The SCK and CMD timing points are measured at the 50% level.

The SIO0 signal is sampled once per t_{CYCLE1} interval on the falling edge. The set/hold window of the sample points is t_{S2}/t_{H2}. The SCK and SIO0 timing points are measured at the 50% level.

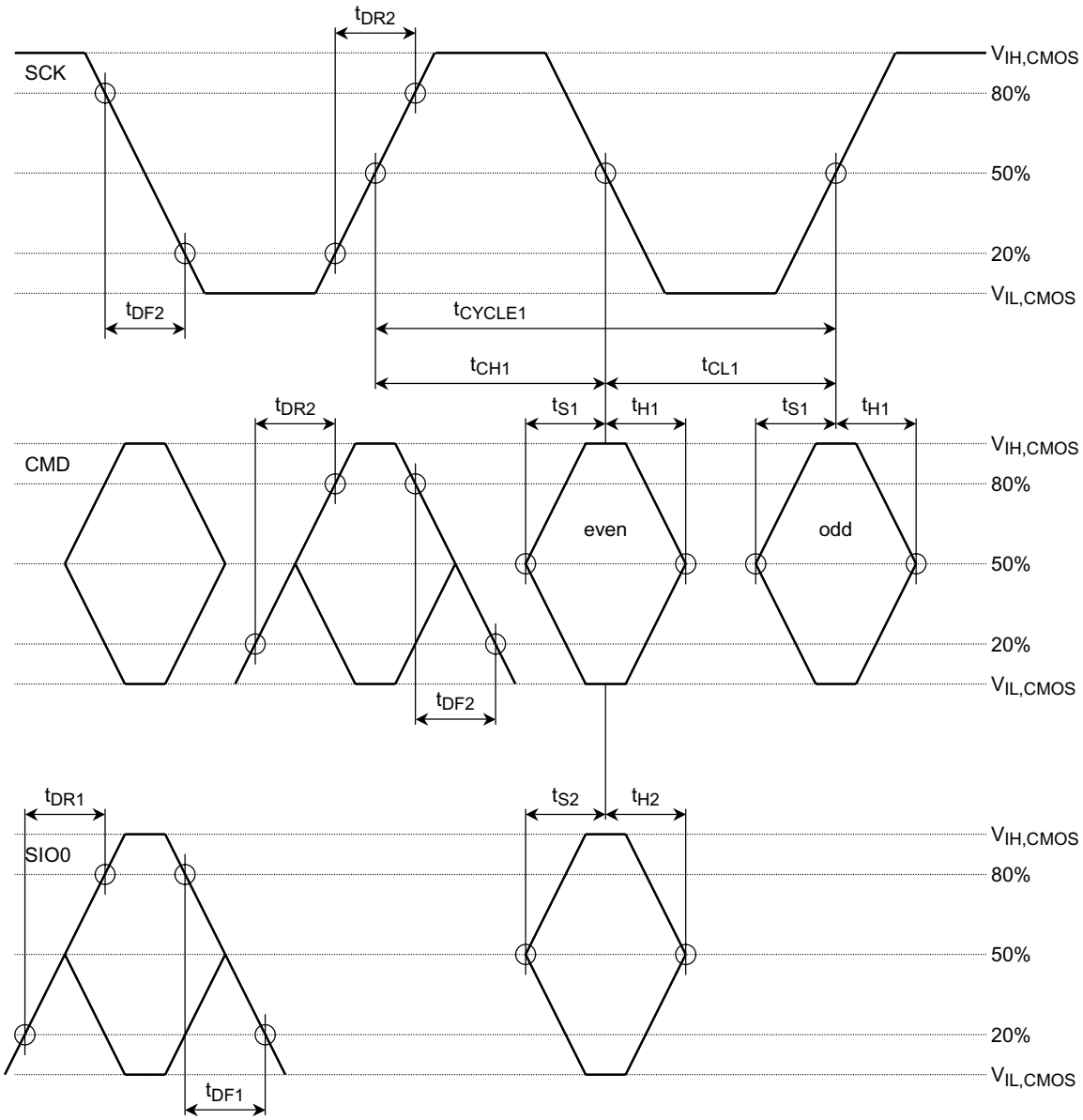


Figure 43. CMOS Timing-Data Signals for Receive

The SCK clock is also used for sampling data on RSL inputs in one situation. Figure 35 shows the PDN and NAP exit sequences. If the PSX field of the INIT register is one (see Figure 27), then the PDN and NAP exit sequences are broadcast; i.e. all RDRAMs that are in PDN or NAP will perform the exit sequence. If the PSX field of the INIT register is zero, then the PDN and NAP exit sequences are directed; i.e. only one RDRAM that is in PDN or NAP will perform the exit sequence.

The address of that RDRAM is specified on the DQA [5:0] bus in the set/hold window t_{S3}/t_{H3} around the rising edge of SCK. This is shown in Figure 44. The SCK timing point is measured at the 50% level, and the DQA [5:0] bus signals are measured at the V_{REF} level.

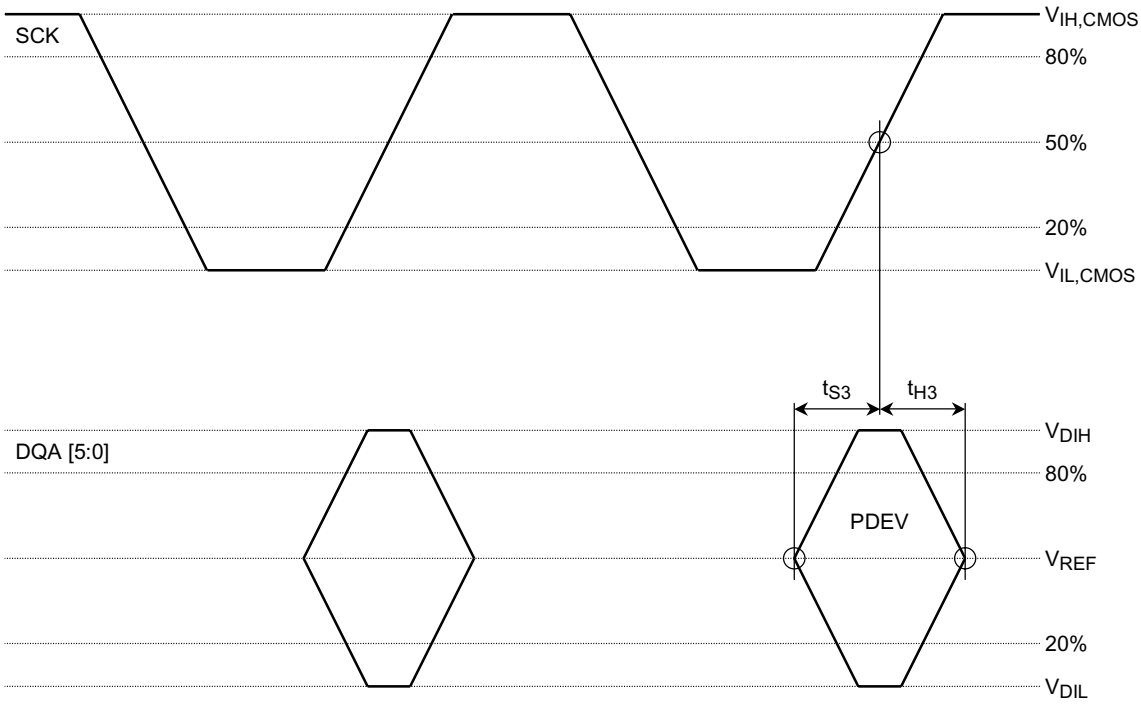


Figure 44. CMOS Timing-Device Address for NAP or PDN Exit

CMOS-Transmit Timing

Figure 45 is a timing diagram which shows the detailed requirements for the CMOS output signals. The SIO0 signal is driven once per t_{CYCLE1} interval on the falling edge. The clock-to-output window is $t_{HR,MIN}/t_{Q1,MAX}$. The SCK and SIO0 timing points are measured at the 50% level. The rise and fall times of SIO0 are t_{QR1} and t_{QF1}, measured at the 20% and 80% levels.

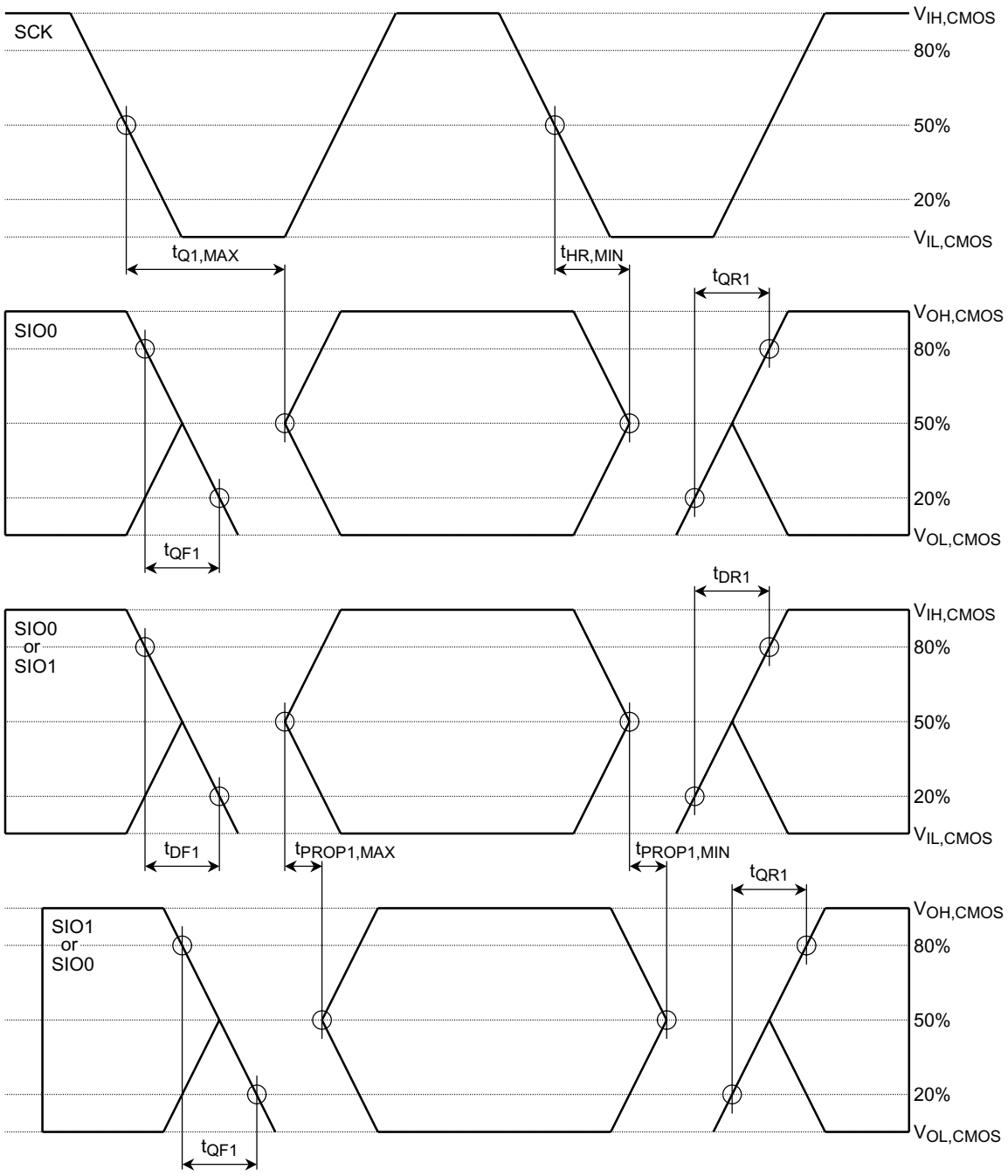


Figure 45. CMOS Timing-Data Signals for Transmit

Figure 45 also shows the combinational path connecting SIO0 to SIO1 and the path connecting SIO1 to SIO0 (read data only). The t_{PROP1} parameter specified this propagation delay. The rise and fall times of SIO0 and SIO1 inputs must be t_{DR1} and t_{DF1}, measured at the 20% and 80% levels. The rise and fall times of SIO0 and SIO1 outputs are t_{QR1} and t_{QF1}, measured at the 20% and 80% levels.

RSL-Domain Crossing Window

When read data is returned by the RDRAM, information must cross from the receive clock domain (CFM) to the transmit clock domain (CTM). The t_{TR} parameter permits the CFM to CTM phase to vary through an entire cycle; i.e. there is no restriction on the alignment of these two clocks. A second parameter t_{DCW} is needed in order to describe how the delay between a RD command packet and read data packet varies as a function of the t_{TR} value.

Figure 46 shows this timing for five distinct values of t_{TR}. Case A ($t_{TR} = 0$) is what has been used throughout this document. The delay between the RD command and read data is t_{CAC}. As t_{TR} varies from zero to t_{CYCLE} (cases A through E), the command to data delay is ($t_{CAC} - t_{TR}$). When the t_{TR} value is in the range 0 to $t_{DCW,MAX}$, the command to data delay can also be ($t_{CAC} - t_{TR} - t_{CYCLE}$).

This is shown as cases A' and B' (the gray packets). Similarly, when the t_{TR} value is in the range ($t_{CYCLE} + t_{DCW,MIN}$) to t_{CYCLE}, the command to data delay can also be ($t_{CAC} - t_{TR} + t_{CYCLE}$). This is shown as cases D' and E' (the gray packets). The RDRAM will work reliably with either the white or gray packet timing. The delay value is selected at initialization, and remains fixed thereafter.

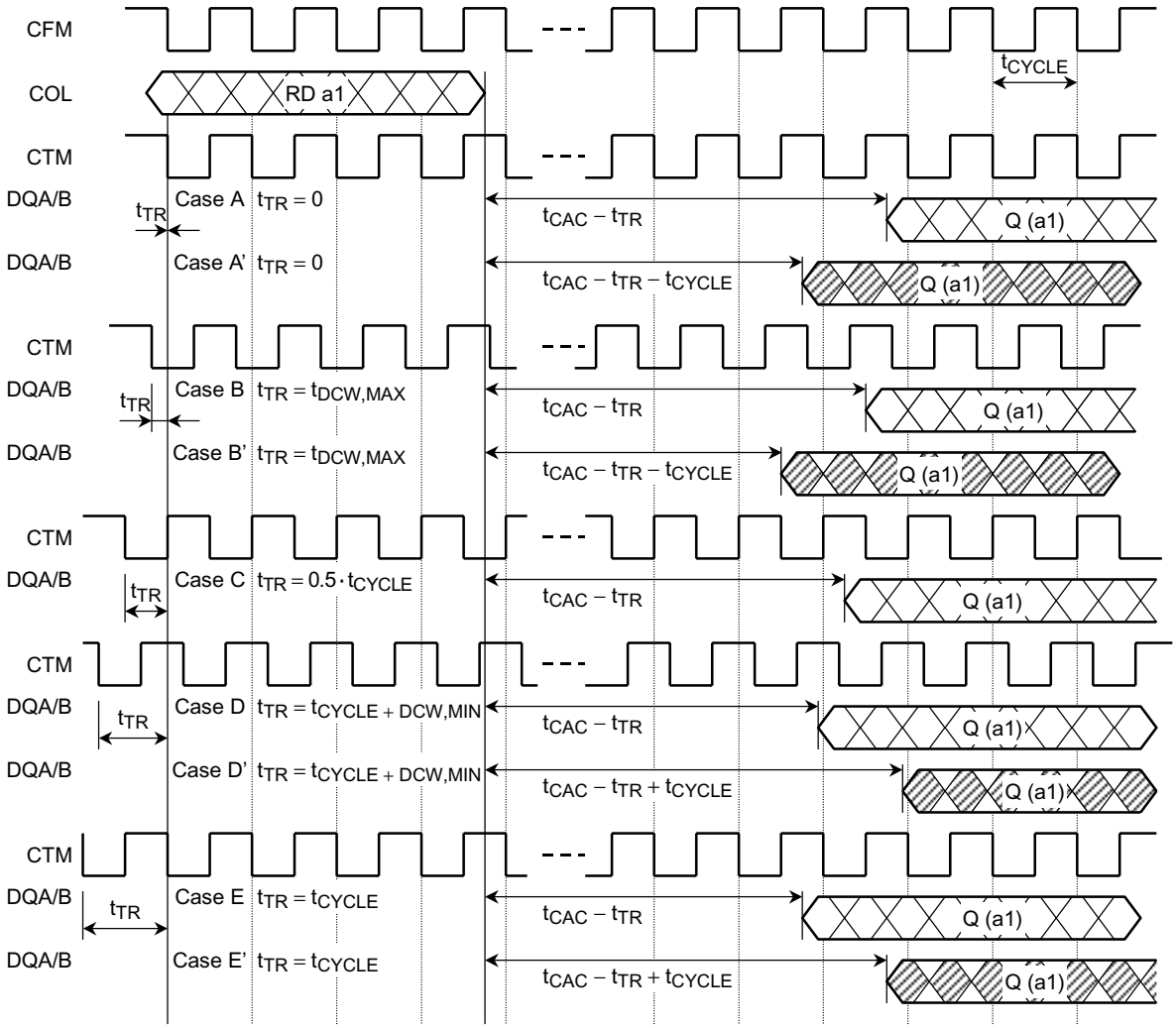


Figure 46. RSL Transmit-Crossing Read Domains

Timing Parameters

PARAMETER	DESCRIPTION	MIN -40 -800	MIN -45 -800	MIN -50 -800	MIN -45 -711	MIN -50 -711	MIN -45 600	MIN -53 -600	MAX	UNITS	Figure (s)
t_{RC}	Row Cycle time of RDRAM banks — the interval between ROWA packets with ACT commands to the same bank.	28	28	34	28	28	22	28	—	t_{CYCLE}	Figure 15 Figure 16
t_{RAS}	RAS-Asserted time of RDRAM bank — the interval between ROWA packet with ACT command and next ROWR packet with PRER[a] command to the same bank.	20	20	24	20	20	16	20	64 µs[b]	t_{CYCLE}	Figure 15 Figure 16
t_{RP}	Row Precharge time of RDRAM banks — the interval between ROWR packet with PRER[a] command and next ROWA packet with ACT command to the same bank.	8	8	10	8	8	6	8	—	t_{CYCLE}	Figure 15 Figure 16
t_{PP}	Precharge-to-Precharge time of RDRAM device — the interval between successive ROWR packets with PRER[a] commands to any banks of the same device.	8	8	8	8	8	8	8	—	t_{CYCLE}	Figure 12
t_{RR}	RAS-to-RAS time of RDRAM device — the interval between successive ROWA packets with ACT commands to any banks of the same device.	8	8	8	8	8	8	8	—	t_{CYCLE}	Figure 11
t_{RCD}	RAS-to-CAS Delay — the interval from ROWA packet with ACT command to COLC packet with RD or WR command. Note: the RAS-to-CAS delay seen by the RDRAM core (t_{RCD-C}) is equal to $t_{RCD-C} = 1 + t_{RCD}$ because of differences in the row and column paths through the RDRAM interface.	7	9	11	7	9	5	7	—	t_{CYCLE}	Figure 15 Figure 16
t_{CAC}	CAS Access delay — the interval from RD command to Q read data. The equation for t_{CAC} is given in the TPARM register in Figure 30.	8	8	8	8	8	8	8	12	t_{CYCLE}	Figure 4 Figure 30
t_{CWD}	CAS Write Delay — the interval from WR command to D write data.	6	6	6	6	6	6	6	6	t_{CYCLE}	Figure 4
t_{CC}	CAS-to-CAS time of RDRAM bank — the interval between successive COLC commands.	4	4	4	4	4	4	4	—	t_{CYCLE}	Figure 15 Figure 16
t_{PACKET}	Length of ROWA, ROWR, COLC, COLM or COLX packet.	4	4	4	4	4	4	4	4	t_{CYCLE}	Figure 3
t_{RTR}	Interval from COLC packet with WR command to COLC packet which causes retire, and to COLM packet with bytemask.	8	8	8	8	8	8	8	—	t_{CYCLE}	Figure 17
t_{OFFP}	The interval (offset) from COLC packet with RDA command, or from COLC packet with retire command (after WRA automatic precharge), or from COLC packet with PREC command, or from COLX packet with PREX command to the equivalent ROWR packet with PRER. The equation for t_{OFFP} is given in the TPARM register in Figure 30.	4	4	4	4	4	4	4	—	t_{CYCLE}	Figure 14 Figure 30
t_{RDP}	Interval from last COLC packet with RD command to ROWR packet with PRER.	4	4	4	4	4	4	4	—	t_{CYCLE}	Figure 15
t_{RTP}	Interval from last COLC packet with automatic retire command to ROWR packet with PRER.	4	4	4	4	4	4	4	—	t_{CYCLE}	Figure 16

a. Or equivalent PREC or PREX command. See Figure 14.

b. This is a constraint imposed by the core, and is therefore in units of µs rather than t_{CYCLE}.

Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to GND	−0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$, $V_{DDA,ABS}$	Voltage on V_{DD} and V_{DDA} with respect to GND	−0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	−50	100	°C

IDD-Supply Current Profile

Supply Current Profile

I_{DD} VALUE	RDRAM POWER STATE And STEADY-STATE TRANSACTION RATES[b]	MIN	MAX @ t_{CYCLE} = 3.33 ns	MAX @ t_{CYCLE} = 2.81 ns	MAX @ t_{CYCLE} = 2.50 ns	UNIT
$I_{DD,PDN}$	Device in PDN, self-refresh enable and INIT. LSR = 0	—	6000	6000	6000	μA
$I_{DD,PDN,L}$	Device in PDN, self-refresh enable and INIT. LSR = 1	—	NA	NA	NA	μA
$I_{DD,NAP}$	Device in NAP.	—	4.2	4.2	4.2	mA
$I_{DD,STBY}$	Device in STBY. This is the average for a device in STBY with (1) no packets on the Channel, and (2) with packets sent to other devices.	—	90	100	101	mA
$I_{DD,REFRESH}$	Device in STBY and refreshing rows at the $t_{REEF,MAX}$ period.	—	95	105	110	mA
$I_{DD,ATTN}$	Device in ATTN. This is the average for a device in ATTN with (1) no packets on the Channel, and (2) with packet sent to other devices.	—	125	140	148	mA
$I_{DD,ATTN-W}$	Device in ATTN. ACT command every $8 \cdot t_{CYCLE}$, PRE command every $8 \cdot t_{CYCLE}$ WR command every $4 \cdot t_{CYCLE}$ and data is 1100..1100	—	525	590	635	mA
$I_{DD,ATTN-R}$	Device in ATTN. ACT command every $8 \cdot t_{CYCLE}$, PRE command every $8 \cdot t_{CYCLE}$ RD command every $4 \cdot t_{CYCLE}$ and data is 1111..1111[c]	—	480	535	575	mA

a. The numbers in this table are targets, not specifications.
b. CMOS interface consumes no power in all power states
c. This does not include the I_{OL} sink current. The RDRAM dissipates $I_{OL} \cdot V_{OL}$ in each output driver when a logic one is driven.

Supply Current at Initialization

SYMBOL	PARAMETER	Allowed Range of t_{CYCLE}	V_{DD}	MIN	MAX	UNIT
$I_{DD,PWRUP,D}$	I_{DD} from power-on to SETR	3.33 ns to 3.83 ns 2.50 ns to 3.32 ns	$V_{DD,MIN}$	—	150[b] 200[a]	mA
$I_{DD,SETR,D}$	IDD from SETR to CLRR	3.33 ns to 3.83 ns 2.50 ns to 3.32 ns	$V_{DD,MIN}$	—	250[b] 332[a]	mA

a. The numbers in this table are specifications, and must be met by all devices.
b. This supply current will be 150 mA when t_{CYCLE} is in the range 15 ns to 100 ns.

Capacitance and Inductance

Figure 47 shows the equivalent load circuit of the RSL and CMOS pins. The circuit models the load that the device presents to the Channel.

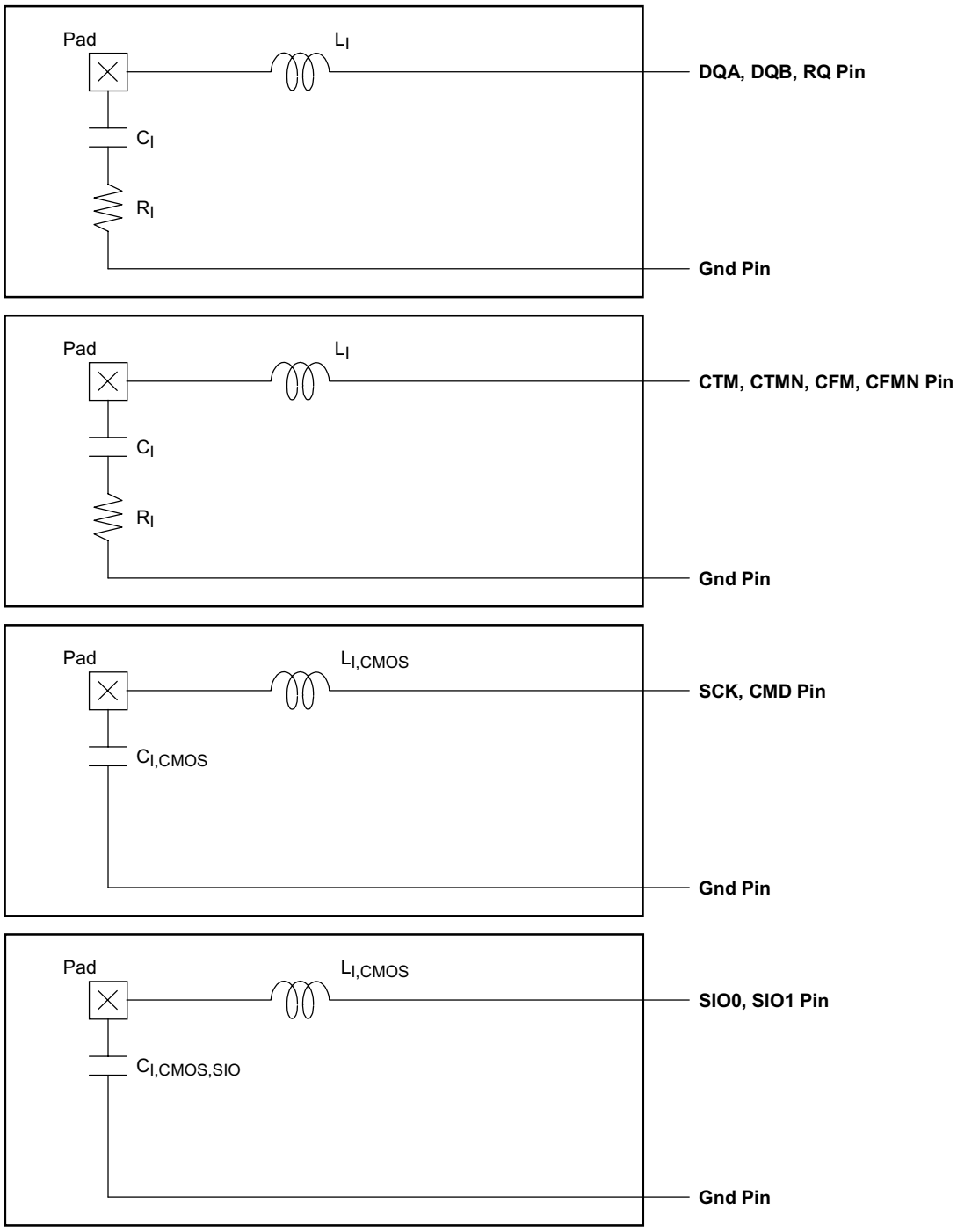


Figure 47. Equivalent Load Circuit for RSL Pins

This circuit does not include pin coupling effects that are often present in the packaged device. Because coupling effects make the effective single-pin inductance L_I, and capacitance C_I, a function of neighboring pins, these parameters are intrinsically data-dependent. For purposes of specifying the device electrical loading on the Channel, the effective L_I and C_I are defined as the worst-case values over all specified operating conditions.

L_I is defined as the effective pin inductance based on the device pin assignment. Because the pad assignment places each RSL signal adjacent to an AC ground (a Gnd or V_{DD} pin), the effective inductance must be defined based on this configuration. Therefore, L_I assumes a loop with the RSL pin adjacent to an AC ground.

C_I is defined as the effective pin capacitance based on the device pin assignment. It is the sum of the effective package pin capacitance and the IO pad capacitance.

SYMBOL	PARAMETER AND CONDITIONS-RSL PINS		MIN	MAX	UNIT
L_I	RSL effective input inductance		—	4.0	nH
L_{12}	Mutual inductance between any DQA or DQB RSL signals.		—	0.2	nH
	Mutual inductance between any ROW or COL RSL signals.		—	0.6	
ΔL_I	Difference in L_I value between any RSL pins of a single device.		—	1.8	nH
C_I	RSL effective input capacitance[a]	-800	2.0	2.4	pF
		-711	2.0	2.4	
		-600	2.0	2.6	
C_{12}	Mutual capacitance between any RSL signals.		—	0.1	pF
ΔC_I	Difference in C_I value between average of CTM/CFM and any RSL pins of a single device.		—	0.06	pF
R_I	RSL effective input resistance		4	15	Ω

a. This value is a combination of the device IO circuitry and package capacitances.

SYMBOL	PARAMETER AND CONDITIONS-CMOS PINS	MIN	MAX	UNIT
$L_{I,CMOS}$	CMOS effective input inductance	—	8.0	nH
$C_{I,CMOS}$	CMOS effective input capacitance (SCK, CMD)[a]	1.7	2.1	pF
$C_{I,CMOS,SIO}$	CMOS effective input capacitance (SIO1, SIO0)[a]	—	7.0	pF

a. This value is a combination of the device IO circuitry and package capacitances.

Interleaved Device Mode

Interleaved Device Mode permits a group of eight RDRAMs on the Channel to collectively respond to a command. The purpose of this collective response is to limit the number of bits in each dualoct data packet which are read from or written to a single RDRAM device. This capability permits a memory controller to implement hardware for fault detection and correction that can tolerate the complete internal failure of one RDRAM device on a Channel.

The IDM bit of the INIT control register enables this fault tolerant operating mode. When it is set, the RDRAM will interpret the DR4..0 and DC4..0 fields of the ROW and COLC packets differently. Figure 48 shows the differences using an example system with eight RDRAMs.

The DEVID4..0 registers of these RDRAMs are initialized to "00000" through "00111". However, when the IDM bit is set, only the upper two bits (DEVID4..3) will be compared to the DR4..3 and DC4..3 fields. This means that ROW and COLC packets will be executed by groups of eight RDRAMs, with a Channel containing from one to four of these groups. The low-order DR2..0 bits are not used when IDM is set, and the low-order DC2..0 bits have a modified function described below.

With IDM set, a directed ACT or PRE command in a ROW packet causes eight RDRAMs to perform the indicated operation. Likewise, when a RD or WR command is specified in a COLC command, the selected group of eight RDRAMs responds. When using IDM, devices must be added to the Channel in groups of eight. An application will typically make the IDM bit setting the same for all RDRAMs on a Channel.

The mechanism for indicating a broadcast ROW packet (DR4F and DR4T are both set to one) is not affected by the setting of the IDM bit; i.e. IDM mode does not change the broadcast ROW packet mechanism.

Likewise, the COLX fields (DX4..0, XOP4..0, and BX4..0) are not changed by IDM mode – all COLX packets are directed to a single device.

When the IDM bit is set, COLM packets should not be used (the M bit should be set to zero, selecting only COLX packets). This is because the mapping of bytes to RDRAM storage cells is changed by IDM mode.

Returning to Figure 48, the remaining fields of the ROW and COLC packets are interpreted in the same way regardless of the setting of the IDM bit – IDM mode does not affect these fields. Specifically, the BR4..0 and BC4..0 fields of the ROW and COLC packets are used to select one of the banks just as when IDM is not set. The R8..0 field of the ROW packet selects a row of the selected (BR4..0) bank to load into the bank's sense amp. And the C6..0 field selects one dualoct of the selected (BC4..0) bank's sense amp.

The IDM bit affects what is done with this selected dualoct. When IDM is not set, the dualoct is driven onto the Channel by the single selected RDRAM device. When IDM is set, each RDRAM of the eight device group selected by DC4..3 drives either 16 bits (×16 device) or 16 or 24 bits (×18 device) of the 144-bit dualoct. The bits driven are a function of the DEVID2..0 RDRAM register field, the DC2..0 COLC packet field, and the device width (×16 or ×18).
Figure 48 shows the mapping that is appropriate for DC2..0 = 000.

Figure 49 and Figure 50 show the mapping for all eight values of DC2..0. There are eight mappings, which are rotated among the eight devices using the following equation:

$$Pin = 7 - 4 \cdot (DEVID2 \wedge DC2) - 2 \cdot (DEVID1 \wedge DC1) - 1 \cdot (DEVID0 \wedge DC0) \quad \text{(Eq 1)}$$

where "^" is the exclusive-or function. "Pin" is the pin number that is driven by the RDRAM with the DEVID2..0 value. For example, Pin = 0 means the RDRAM drives DQA0 and DQB0, and so forth.

The DQA8 pin is always driven with DQA7, and DQB8 is always driven with DQB6 for ×18 devices. For ×16 devices, the DQA8 and DQB8 pins are not used.

For each of the eight mappings, the eight-RDRAM group supplies a complete dualoct. As the application steps through eight values of DC2..0, all the bits of the eight underlying dualocts will be accessed. Thus, an eight-RDRAM group appears to be a single RDRAM with eight times the normal page size, with the DC2..0 field providing the extra column addressing information (beyond what C6..0 provides).

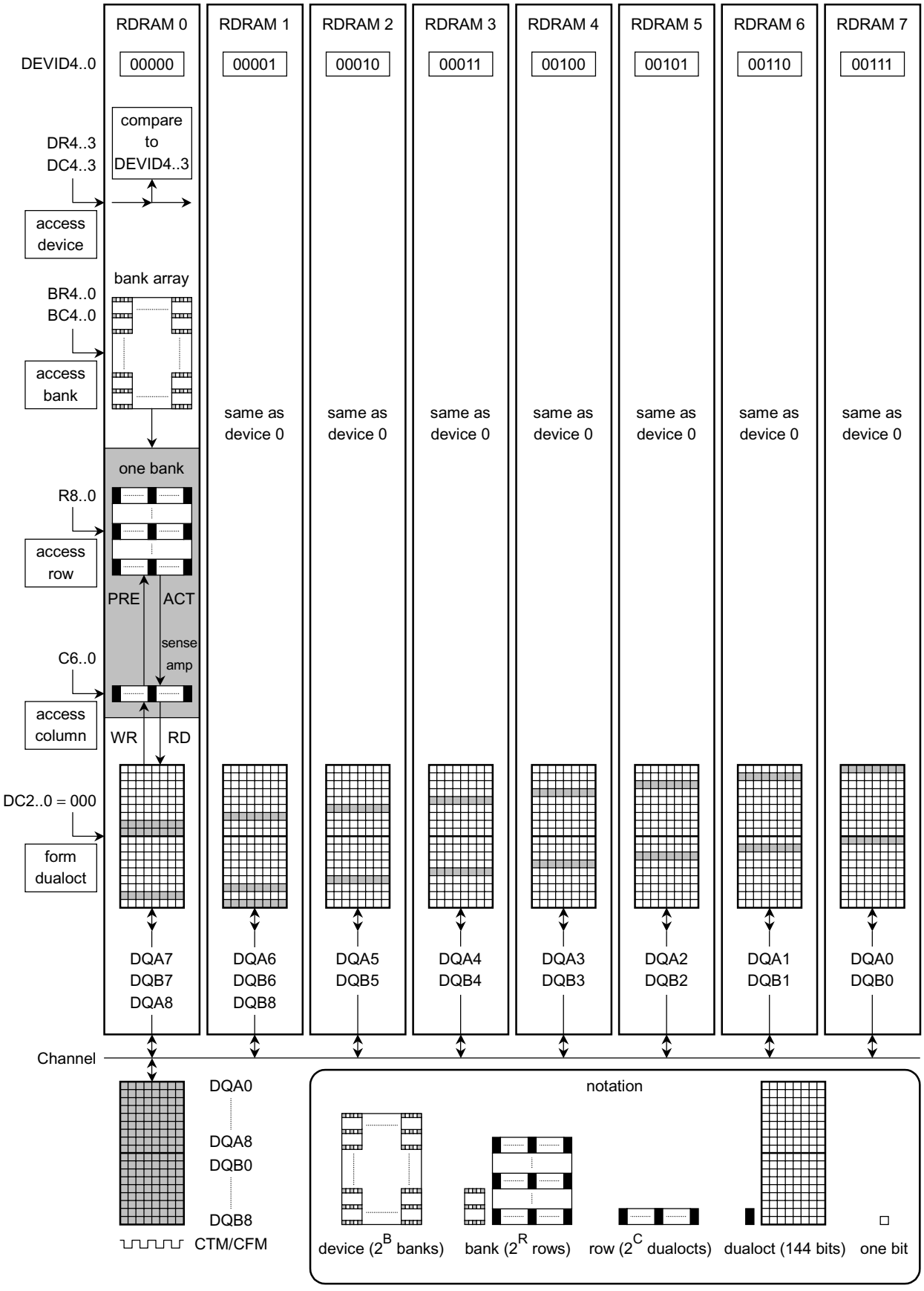


Figure 48. ACT, PRE, RD, and WR Commands for Eight RDRAM System with IDM = 1

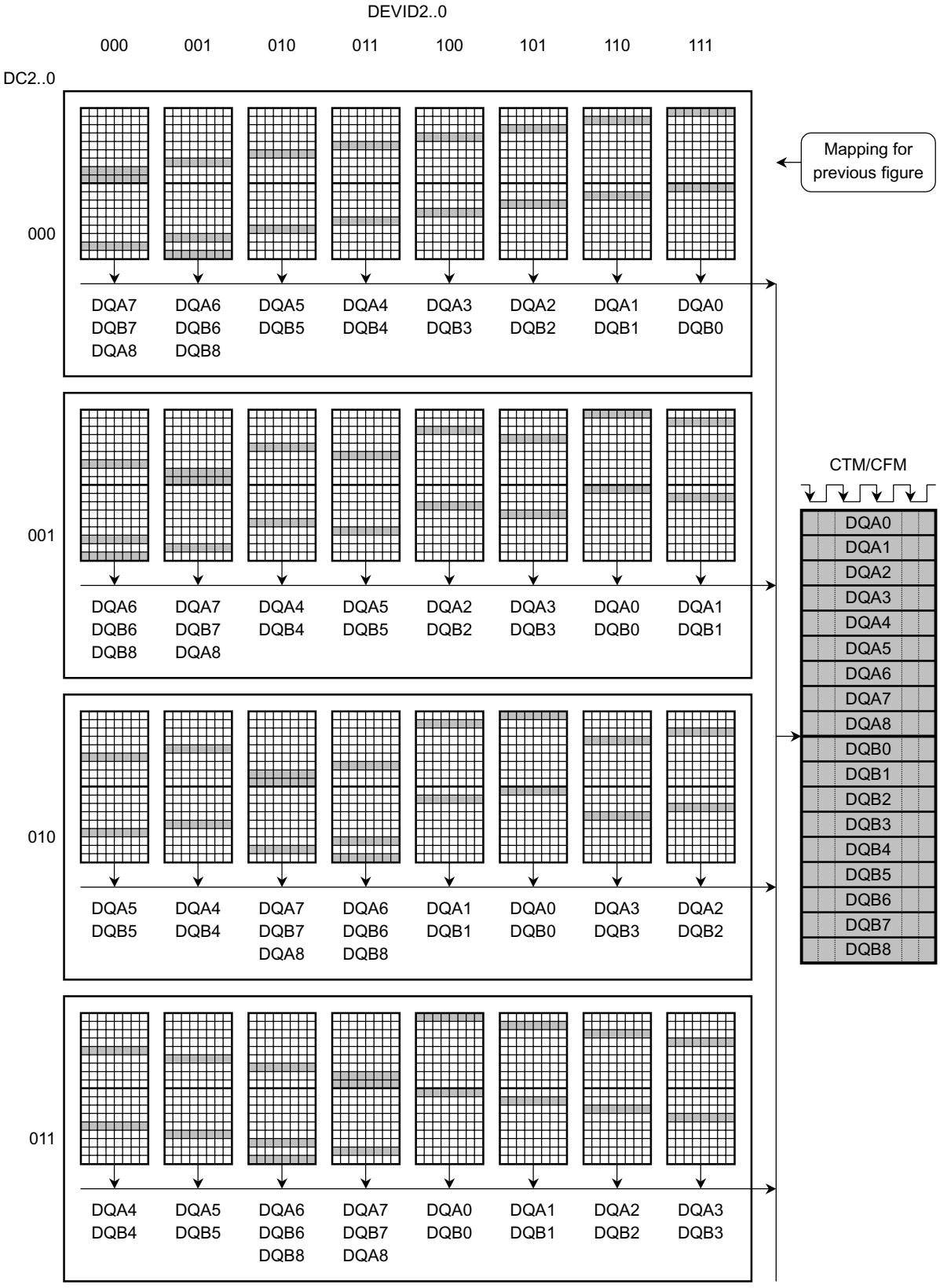


Figure 49. Mapping from DEVID2..0 and DC2..0 Fields to DQ Packet with IDM = 1

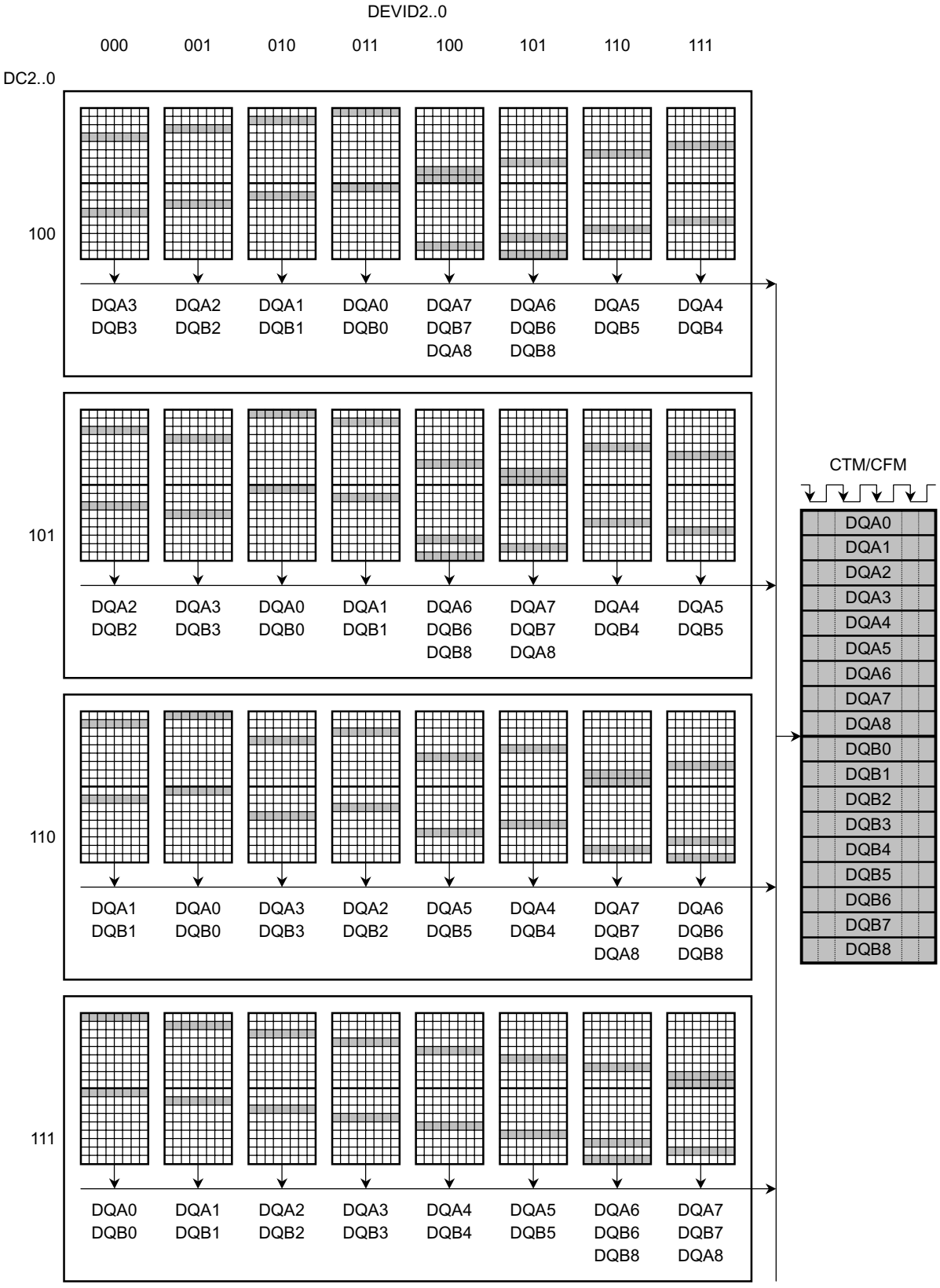


Figure 50. Mapping from DEVID2..0 and DC2..0 Fields to DQ Packet with IDM = 1 (continued)

Glossary of Terms

ACT	Activate command from AV field
activate	To access a row and place it in a sense amp
adjacent	Two RDRAM banks which share sense amps (also called doubled banks)
ASYM	CCA register field for RSL V_{OL}/V_{OH}
ATTN	Power state-ready for ROW/COL packets
ATTNR	Power state-transmitting Q packets
ATTNW	Power state-receiving D packets
AV	Op-code field in ROW packets
bank	A block of $2^{RBIT} \cdot 2^{CBIT}$ storage cells in the core of the RDRAM
BC	Bank address field in COLC packet
broadcast	An operation executed by all RDRAMs
BR	Bank address field in ROW packets
bubble	Idle cycle (s) on RDRAM pins needed because of a resource constraint
BYT	CNFGB register field-8/9 bits per byte
BX	Bank address field in COLX packet
C	Column address field in COLC packet
CAL	Calibrate (I_{OL}) command in XOP field
CBIT	CNFGB register field-# of column address bits
CCA	Control register-Current Control A
CCB	Control register-Current Control B
CFM, CFMN	Clock pins for receiving packets
Channel	ROW/COL/DQ pins and external wires
CLRR	Clear Reset command from SOP field
CMD	CMOS pin for initialization/power control
CNFGA	Control register with configuration fields
CNFGB	Control register with configuration fields
COL	Pin for column access control
COL	COLC, COLM or COLX packet on COL pins
COLC	Column operation packet on COL pins
COLM	Write mask packet on COL pins
column	Rows in a bank or activated row in sense amps have 2^{CBIT} dualocts column storage
command	A decoded bit-combination from a field
COLX	Extended operation packet on COL pins
controller	A logic device which drives the ROW/COL/DQ wires for a Channel of RDRAMs
COP	Column op-code field in COLC packet
CORG	CNFGB register field-# of bank and row address bits
core	The banks and sense amps of a RDRAM
CTM, CTMN	Clock pins for transmitting packets
current control	Periodic operations to update the proper I_{OL} value of RSL output drivers

D	Write data packet on DQ pins
DBL	CNFGA register field-double bank
DC	Device address field in COLC packet
device	A RDRAM on a Channel
DEVID	Control register with device address that is matched against DR, DC and DX fields
DM	Device match for ROW packet decode
doubled-bank	RDRAM with shared sense amp
DQ	DQA and DQB pins
DQA	Pins for data byte A
DQB	Pins for data byte B
DQS	NAPX register field-PDN/NAP exit
DR, DR4T, DR4F	Device address field and packet framing fields in ROWA and ROWR packets
dualoct	16 bytes-the smallest addressable data item
DX	Device address field in COLX packet
field	A collection of bits in a packet
INIT	Control register with initialization fields
initialization	Configuring a Channel of RDRAMs so that they are ready to respond to transactions
LSR	INIT register field-low-power self-refresh
M	Mask op-code field (COLM/COLX packet)
MA	Field in COLM packet for masking byte A
MB	Field in COLM packet for masking byte B
MSK	Mask command in M field
MVER	Control register-manufacturer ID
NAP	Power state-needs SCK/CMD wake-up
NAPR	Nap command in ROP field
NAPRC	Conditional nap command in ROP field
NAPXA	NAPX register field-NAP exit delay A
NAPXB	NAPX register field-NAP exit delay B
NOCOP	No-Operation command in COP field
NOROP	No-Operation command in ROP field
NOXOP	No-Operation command in XOP field
NSR	INIT register field-NAP self-refresh
packet	A collection of bits carried on the Channel
PDN	Power state-needs SCK/CMD wakeup
PDNR	Power-Down command in ROP field
PDNXA	Control register-PDN exit delay A
PDNXB	Control register-PDN exit delay B
pin efficiency	The fration of non-idle cycles on a pin
PRE	PREC, PRER and PREX precharge commands
PREC	Precharge command in COP field

precharge	Prepares sense amp and bank for Activate
PRER	Precharge command in ROP field
PREX	Precharge command in XOP field
PSX	INIT register field-PDN/NAP exit
PSR	INIT register field-PDN self-refresh
PVER	CNFGA register field-protocol version
Q	Read data packet on DQ pins
R	Row address field of ROWA packet
RD/RDA	Read (/precharge) command in COP field
read	Operation for accessing sense amp data
receive	Moving information from the Channel into the RDRAM (a serial stream is demuxed)
REFA	Refresh-Activate command in ROP field
REFB	Control register-next bank (self-refresh)
REFBIT	CNFGA register field-ignore bank bits (for REFA and self-refresh)
REFP	Refresh-Precharge command in ROP field
REFR	Control register-next row for REFA
refresh	Periodic operations to restore storage cells
retire	The automatic operation that stores write buffer into sense amp after WR command
RLX	RLXC, RLXR and RLXX relax commands
RLXC	Relax command in COP field
RLXR	Relax command in ROP field
RLXX	Relax command in XOP field
ROP	Row-op-code field in ROWR packet
row	2^{CBIT} dualocts of cells (bank/sense amp)
ROW	Pins for row access control
ROW	ROWA or ROWR packets on ROW pins
ROWA	Activate packet on ROW pins
ROWR	Row operation packet on ROW pins
RQ	Alternative name for ROW/COL pins
RSL	Rambus Signaling Levels
SAM	Sample (I_{OL}) command in XOP field
SA	Serial address packet for control register transactions w/ SA address field
SBC	Serial broadcast field in SRQ
SCK	CMOS clock pin
SD	Serial data packet for control register transactions w/ SD data field
SDEV	Serial device address in SRQ packet
SDEVID	INIT register field-Serial device ID
self-refresh	Refresh mode for PDN and NAP
sense amp	Fast storage that holds copy of bank's row

SETF	Set fast clock command from SOP field
SETR	Set reset command from SOP field
SINT	Serial interval packet for control register read/write transactions
SIO0, SIO1	CMOS serial pins for control registers
SOP	Serial op-code field in SRQ
SRD	Serial read opcode command from SOP
SRP	INIT register field-Serial Repeat bit
SRQ	Serial request packet for control register read/write transactions
STBY	Power state-ready for ROW packets
SVER	Control register-stepping version
SWR	Serial write op-code command from SOP
TCAS	TPARM register field-t_{CAS} core delay
TCDLY0	TPARM register field-t_{CDLY0} delay
TCDLY1	TCDLY register field-t_{CDLY1} delay
TCLS	TPARM register field-t_{CLS} core delay
TCYCLE	TCYCLE register-t_{CYCLE} delay
TEST77	TEST77 register-for test purposes
TEST78	TEST78 register-for test purposes
transaction	ROW, COL or DQ packets for memory access
transmit	Moving information from the RDRAM onto the Channel (parallel word is muxed)
WR/WRA	Write (/precharge) command in COP field
write	Operation of modifying sense amp data
XOP	Extended opcode field in COLX packet

PACKAGE DIMENSIONS

Unit: mm

P-TFBGA92-1018-0.80AZ