TH7110

315/433MHz FSK/FM/ASK

Double-Conversion Superheterodyne Receiver

Features

- Double superhet architecture for high degree of image rejection
- FSK for digital data and FM reception for analog signal transmission
- FM/FSK demodulation either with phase-coincidence or PLL demodulator
- Low current consumption in active mode and very low standby current
- Switchable LNA gain for improved dynamic range
- AFC feature allows wide carrier frequency acceptance range
- RSSI allows signal strength indication and ASK detection
- Surface mount package LQFP44

Ordering Information

Part No.	*Temperature Range*	*Package*
TH7110	-40 °C to 85 °C	LQFP44

Application Examples

- General digital and analog 315 MHz or 433 MHz ISM band usage
- Low-power telemetry
- Alarm and security systems
- Keyless car and central locking
- Pagers

Technical Data Overview

- Input frequency range: 300 MHz to 500 MHz
- Power supply range: 2.3 V to 5.5 V at ASK and 2.5 V to 5.5 V at FSK
- Temperature range: -40 °C to +85 °C
- Operating current: 6.5 mA at low gain and 7.8 mA at high gain mode
- Standby current: 50 nA
- Sensitivity: -111 dBm [1)] with 40 kHz second IF filter BW (incl. SAW front-end filter loss)
- Sensitivity: -104 dBm [2)] with 150 kHz second IF filter BW (incl. SAW front-end filter loss)
- Range of first IF: 10 MHz to 80 MHz
- Range of second IF: 455 kHz to 21.4 MHz
- Maximum input level: –10 dBm at ASK and 0 dBm at FSK
- Input impedance: 50 Ω
- Image rejection: > 65 dB (e.g. with SAW front-end filter and at 10.7 MHz 2^{nd} IF)
- Spurious emission: < -70 dBm
- Carrier frequency acceptance: ±200 kHz (with AFC active)
- RSSI range: 70 dB
- Frequency deviation range: ±5 kHz to ±120 kHz
- Maximum data rate: 80 kbit/s NRZ
- Maximum analog modulation frequency: 15 kHz

[1)] at ± 8 kHz FSK deviation, BER = $3 \cdot 10^{-3}$ and phase-coincidence demodulation
[2)] at ± 50 kHz FSK deviation, BER = $3 \cdot 10^{-3}$ and phase-coincidence demodulation

General Description

The TH7110 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) for generation of the first and second local oscillator signals LO1 and LO2
- Parts of the PLL SYNTH are the high-frequency VCO1, the feedback dividers DIV_8 and DIV_2, a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (IF1)
- second mixer (MIX2) for down-conversion of the IF1 to the second IF (IF2)
- IF amplifier (IFA) to amplify and limit the IF2 signal and for RSSI generation
- Phase coincidence demodulator (DEMOD) with third mixer (MIX3) to demodulate the IF signal
- Operational amplifier (OA) for data slicing, filtering, ASK detection and automatic-frequency control (AFC)
- Bias circuitry for bandgap biasing and circuit shutdown

With the TH7110 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FM/FSK reception the IF tank used in the phase coincidence demodulator can be constituted either by a ceramic resonator or an LC tank (optionally with varactor to create an AFC circuit). In PLL demodulator configuration, the multiplier MIX3 forms a phase comparator. In ASK configuration, the RSSI signal is feed to an ASK detector, which is constituted by the operational amplifier. The second VCO (VCO2) can be used either as the VCO of a PLL demodulator or as the LO2 source of a second external PLL in a multi-channel system. The following table briefly summarizes the various configurations.

	Single-conversion configuration	Double-conversion configuration
FM/FSK	narrow-band RX with ceramic demodulation tank	narrow-band RX with ceramic demodulation tank
FM/FSK	wide-band RX with LC demod. tank and AFC	wide-band RX with LC demod. tank and AFC
FM/FSK	extended sensitivity RX with PLL demodulator	extended sensitivity RX with PLL demodulator
FM/FSK		multi-channel RX with ceramic demodulation tank and external channel synthesizer
ASK	RX with RSSI-based demodulation	RX with RSSI-based demodulation
ASK		RX with RSSI-based demodulation and external channel synthesizer

The preferred superheterodyne configuration is **double conversion** where MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. This allows a **high degree of image rejection**, achieved in conjunction with an RF front-end filter. Efficient RF front-end filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding a LC filter at the LNA output.

It is also possible to use the TH7110 in **single-conversion** configuration. This can be achieved by switching the LO2 input of MIX2 from the on-chip PLL synthesizer to the pin IN_MIX2 by means of an internal switch (done via pin SW_MIX2). Now MIX2 operates as an amplifier for the IF1 signal if an external pull-down resistor at pin IN_MIX2 is added.

The same setting of MIX2 can be used for **multi-channel applications**. In this situation IN_MIX2 must be driven by an external LO2 signal. This signal can be generated by the VCO2, which is mainly a bipolar transistor that can be configured as a varactor-tuned VCO. Furthermore, a second external PLL for channel selection via LO2 tuning is required. This may be arranged by using the Melexis TH7010 PLL synthesizer chip that can be controlled through a 3-wire bus serial interface. The reference signal for the external PLL synthesizer can be directly taken from the crystal-based reference oscillator RO.

Block Diagram

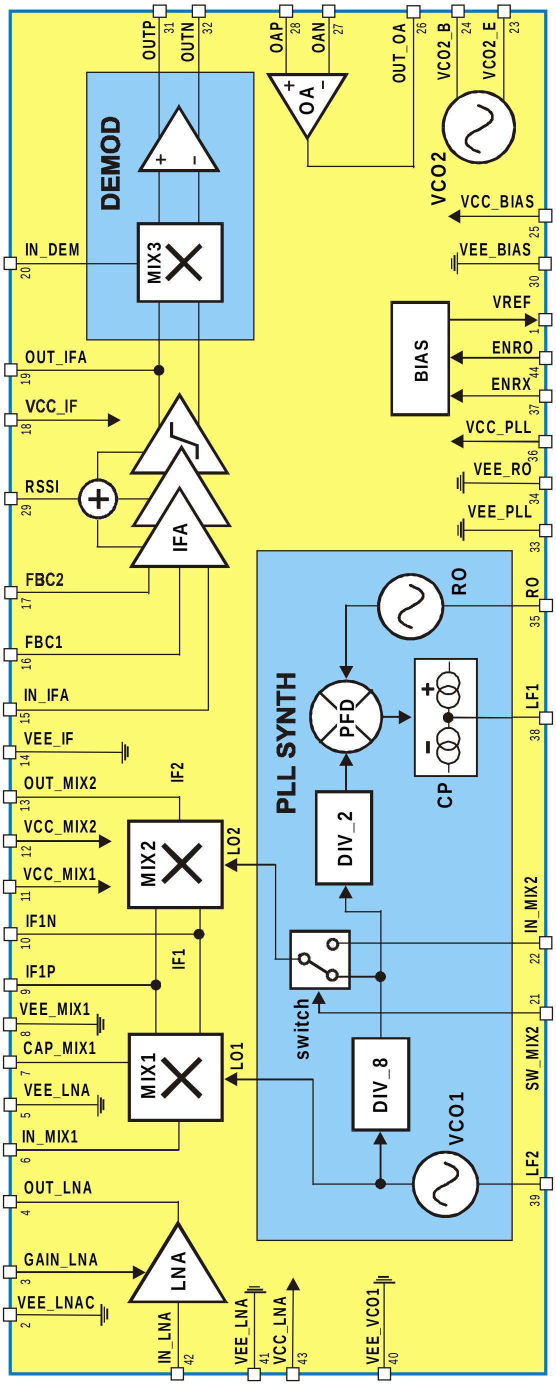


Fig. 1: TH7110 block diagram

Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that might be chosen, and then the only possible choice is low-side or high-side injection of the LO1 signal (which is now the one and only LO signal in the receiver).

The receiver's double-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them are the image of the RF signal (that must be suppressed by the RF front-end filter), spurious signals injected to the first IF (IF1) and their images which could be mixed down to the same second IF (IF2) as the desired RF signal (they must be suppressed by the LC filter at IF1 and/or by low-crosstalk design).

By configuring the TH7110 for double conversion and using its internal PLL synthesizer with fixed feedback divider ratios of N1 = 8 (DIV_8) and N2 = 2 (DIV_2), four types of down-conversion are possible: low-side injection of LO1 and LO2 (**low-low**), LO1 low-side and LO2 high-side (**low-high**), LO1 high-side and LO2 low-side (**high-low**) or LO1 and LO2 high-side (**high-high**). The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF), the first IF (IF1) and the VCO1 or first LO frequency (LO1), respectively, for a given RF and second IF (IF2).

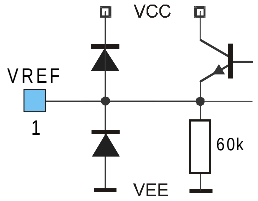
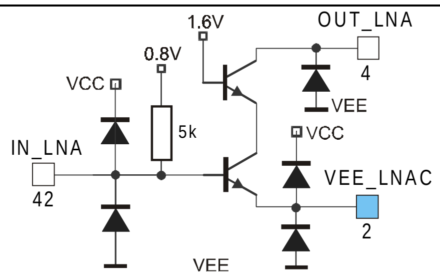
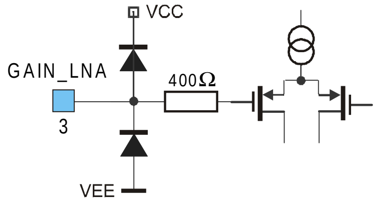
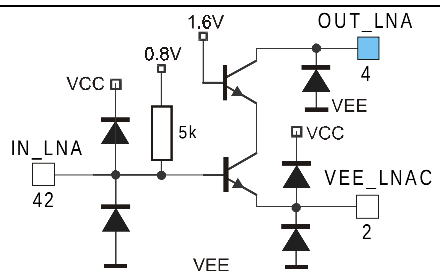
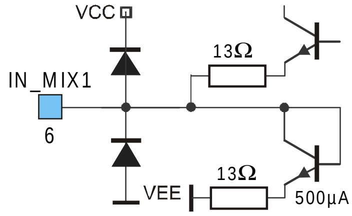
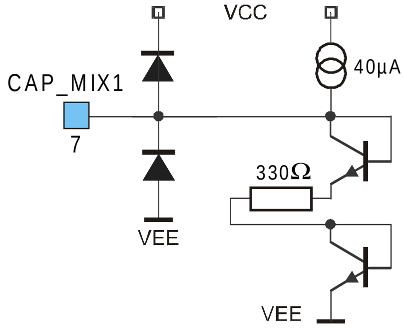
Injection type	high-high	low-low	high-low	low-high
REF	(RF – IF2)/14	(RF – IF2)/18	(RF + IF2)/14	(RF + IF2)/18
LO1	16•REF	16•REF	16•REF	16•REF
IF1	LO1 – RF	RF – LO1	LO1 – RF	RF – LO1
LO2	2•REF	2•REF	2•REF	2•REF
IF2	LO2 – IF1	IF1 – LO2	IF1 – LO2	LO2 – IF1

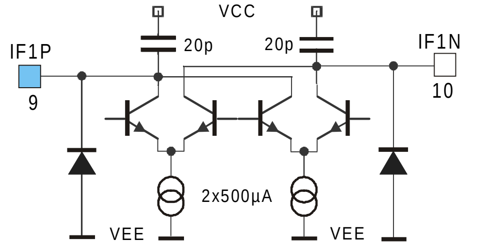
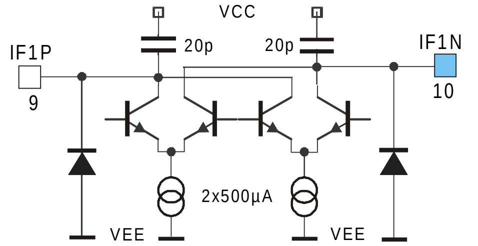
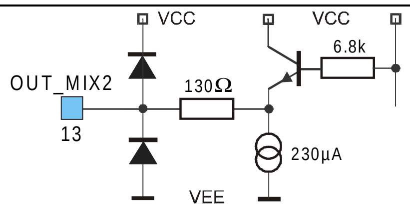
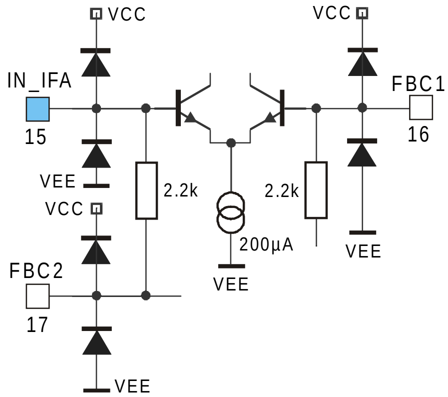
The following table depicts generated, desired, possible images and some undesired signals considering the examples of 315 MHz and 433.6 MHz RF reception at IF2 = 10.7 MHz.

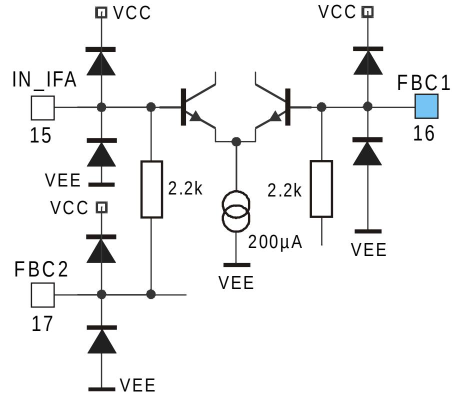
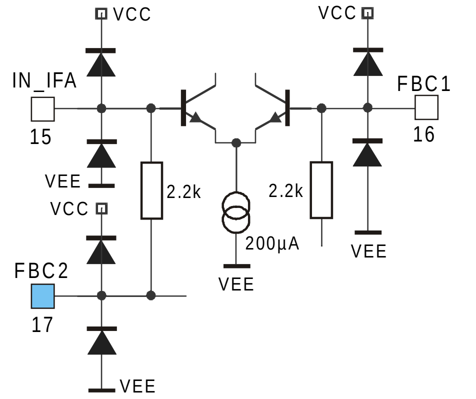
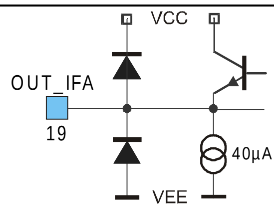
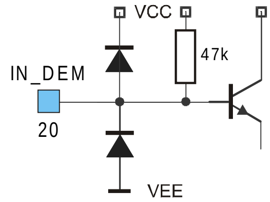
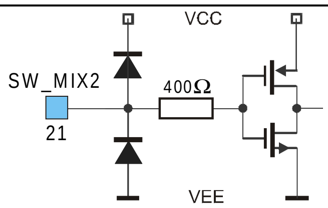
Signal type	RF = 315 MHz	RF = 315 MHz	RF = 315 MHz	RF = 315 MHz	RF = 433.6 MHz	RF = 433.6 MHz	RF = 433.6 MHz	RF = 433.6 MHz
Injection type	high-high	low-low	**high-low**	low-high	high-high	**low-low**	high-low	low-high
REF / MHz	21.73571	16.90556	**23.26429**	18.09444	30.20714	**23.49444**	31.73571	24.68333
LO1 / MHz	347.77143	270.48889	**372.22857**	289.51111	483.31429	**375.91111**	507.77143	394.93333
IF1 / MHz	32.77143	44.51111	**57.22857**	25.48889	49.71429	**57.68889**	74.17143	38.66667
LO2 / MHz	43.47143	33.81111	**46.52857**	36.18889	60.41429	**46.98889**	63.47143	49.36667
RF image/MHz	380.54286	225.97778	**429.45714**	264.02222	533.02857	**318.22222**	581.94286	356.26667
IF1 image/MHz	54.17143	23.11111	**35.82857**	46.88889	71.11429	**36.28889**	52.77143	60.06667

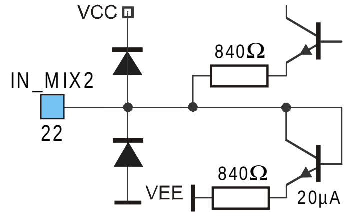
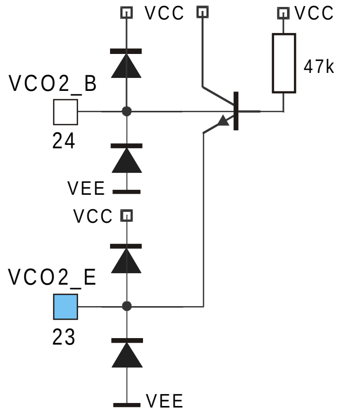
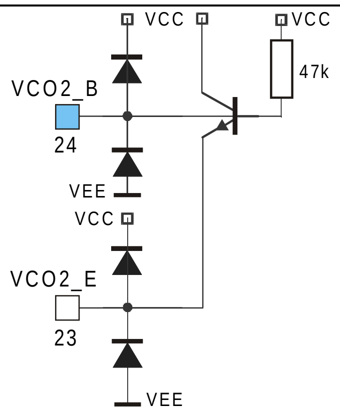
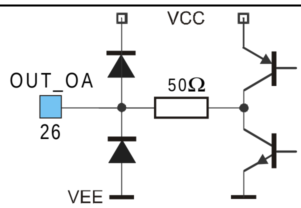
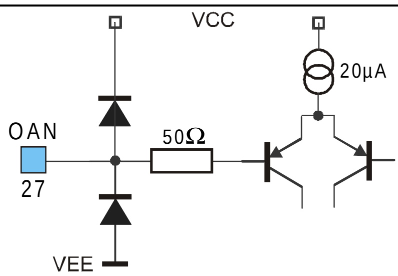
The selection of the reference crystal frequency is based on some assumptions. As for example: the first IF and the image frequencies should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO1 signal should be in the range of 300 MHz to 450 MHz (because this is the optimum frequency range of the VCO1). Furthermore the first IF should be as high as possible to achieve highest RF image rejection. The columns in bold depict the selected frequency plans to receive at 315 MHz and 433.6 MHz, respectively.

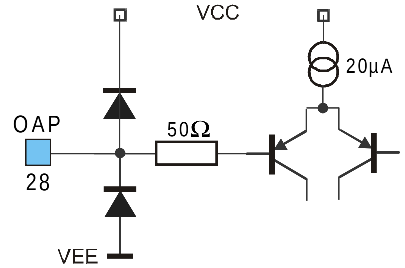
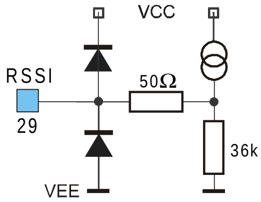
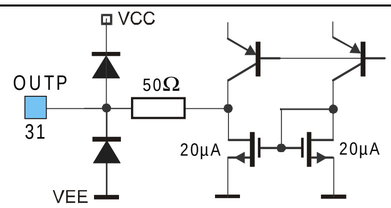
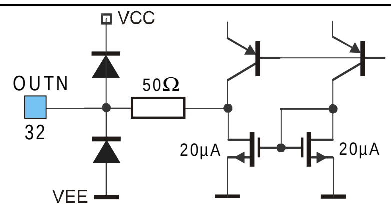
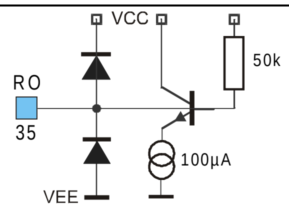
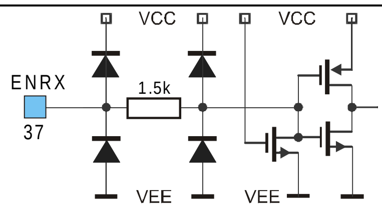
Pin Definition and Description

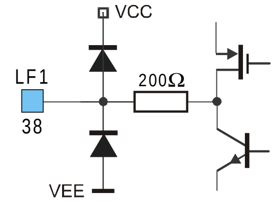
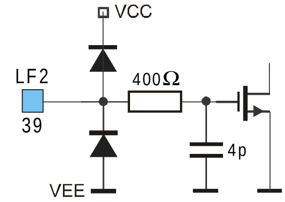
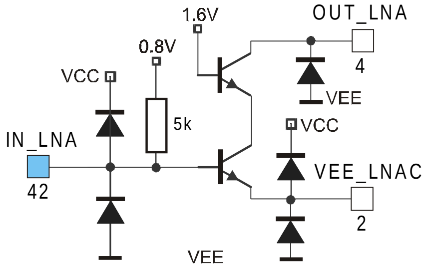
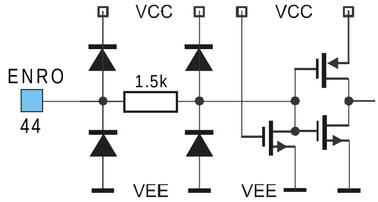
Pin No.	Name	I/O Type	Functional Schematic	Description
1	VREF	analog output		reference voltage output, approx. 1.23V
2	VEE_LNAC	ground		ground of LNA core (cascode)
3	GAIN_LNA	analog input		LNA gain control (CMOS input with hysteresis)
4	OUT_LNA	analog output		LNA open-collector output, to be connected to external LC tank that resonates at RF
5	VEE_LNA	ground		LNA biasing ground
6	IN_MIX1	analog input		MIX1 input, approx. 33Ω single-ended
7	CAP_MIX1	analog I/O		connection for MIX1 blocking capacitor

Pin No.	Name	I/O Type	Functional Schematic	Description
8	VEE_MIX1	ground		MIX1 ground
9	IF1P	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
10	IF1N	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
11	VCC_MIX1	supply		MIX1 positive supply
12	VCC_MIX2	supply		MIX2 positive supply
13	OUT_MIX2	analog output		MIX2 output, approx. 330Ω output impedance
14	VEE_IF	ground		ground of MIX2, IFA and DEMOD
15	IN_IFA	analog input		IFA input, approx. 2.2kΩ input impedance

Pin No.	Name	I/O Type	Functional Schematic	Description
16	FBC1	analog I/O		to be connected to external IFA feedback capacitor
17	FBC2	analog I/O		to be connected to external IFA feedback capacitor
18	VCC_IF	supply		positive supply for IFA, DEMOD and VCO2
19	OUT_IFA	analog I/O		IFA output and MIX3 input (of DEMOD)
20	IN_DEM	analog input		DEMOD input, to MIX3 core
21	SW_MIX2	digital input		input selection for LO2 input port of MIX2

Pin No.	Name	I/O Type	Functional Schematic	Description
22	IN_MIX2	analog input		external LO2 input port of MIX2, approx. 1kΩ single-ended
23	VCO2_E	analog output		VCO2 output, emitter of a bipolar transistor
24	VCO2_B	analog input		VCO2 input, base of a bipolar transistor
25	VCC_BIAS	supply		positive supply of general bias system and OA
26	OUT_OA	analog output		OA output, 40uA current drive capability
27	OAN	analog input		negative OA input, input voltage limited to approx. 0.7 V_{pp} between pins OAP and OAN

Pin No.	Name	I/O Type	Functional Schematic	Description
28	OAP	analog input		positive OA input, input voltage limited to approx. 0.7 V_{pp} between pins OAP and OAN
29	RSSI	analog output		RSSI output, for RSSI and ASK detection, approx. 36kΩ output impedance
30	VEE_BIAS	ground		ground for general bias system and OA
31	OUTP	analog output		FSK/FM positive output, high-impedance
32	OUTN	analog output		FSK/FM negative output, high-impedance
33	VEE_PLL	ground		ground of dividers and PFD
34	VEE_RO	ground		RO ground
35	RO	analog input		RO input, Colpitts type oscillator with internal feedback capacitors
36	VCC_PLL	supply		positive supply of RO, DIV, PFD and charge pump
37	ENRX	digital input		mode control input (CMOS input)

Pin No.	Name	I/O Type	Functional Schematic	Description
38	LF1	analog output		charge pump output
39	LF2	analog input		VCO1 control input
40	VEE_VCO1	ground		ground of VCO1 and charge pump
41	VEE_LNA	ground		ground of LNA biasing
42	IN_LNA	analog input		LNA input, approx. 50Ω single-ended
43	VCC_LNA	supply		positive supply of LNA biasing
44	ENRO	digital input		mode control input (CMOS input)

Technical Data

Mode Configurations

ENRX	ENRO	Mode	Description
0	0	SBY	standby mode
0	1	RO only	only reference oscillator active
1	0	ON	entire chip active
1	1	ON	entire chip active

Note: ENRX and ENRO are pulled down internally

Second Mixer Input

IN_MIX2	SW_MIX2	Mode
External LO2	0	double conversion with external LO2
Ext. pull-down res. (15 kΩ)	0	single conversion
N/C	1	double conversion with internal LO2

LNA Gain Control

V_{GAIN_LNA}	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain by voltage at GAIN_LNA
> 1.4 V	LOW GAIN	LNA set to low gain by voltage at GAIN_LNA

Note: hysteresis between gain modes to ensure stability

Absolute Maximum Ratings

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{cc}		0	7.0	V
Analog/digital control voltage	V_{CTRL}		- 0.3	V_{CC}+0.3	V
Input RF level	P_{imax}	no damage		10	dBm
Storage temperature	T_{STG}		-40	+125	°C
Electrostatic discharge	ESD	human body model, MIL STD 833D method 3015.7	1.0		kV

Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at ASK	$V_{cc,\ ASK}$		2.3	5.5	V
Supply voltage at FSK/FM	$V_{cc,\ FSK}$		2.5	5.5	V
Operating temperature	T_a		-40	+85	ºC
Input frequency	f_i		300	500	MHz
Frequency deviation	Δf	at FM or FSK	±5	±120	kHz
FSK data rate	R_{FSK}	NRZ		40	kbit/s
FM bandwidth	f_m			15	kHz
ASK data rate	R_{ASK}	NRZ		80	kbit/s

DC Characteristics

all parameters under normal operating conditions, unless otherwise stated

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	I_{SBY}	ENRX=0, ENRO=0			50	nA
Reference-oscillator-only current	$I_{cc, RO}$	ENRX=0, ENRO=1	0.4	0.5	0.6	mA
Total supply current at low gain	$I_{cc, tot}$	ENRX=1, V_{GAIN_LNA} > 1.4 V	6.2	6.5	6.8	mA
Total supply current at high gain	$I_{cc, tot}$	ENRX=1, V_{GAIN_LNA} < 0.8 V	7.4	7.8	8.2	mA
Reference voltage	V_{reff}		1.15		1.30	V
Opamp input offset voltage	V_{offs}		-5		5	mV
Opamp input offset current	I_{offs}		-30		30	nA
Opamp input bias current	I_{bias}		-80		80	nA

AC System Characteristics

all parameters under normal operating conditions, unless otherwise stated;
all parameters based on test circuits for FSK (Fig. 2), FM (Fig. 3) and ASK (Fig. 4), respectively;
RF at 433.6 MHz, second IF at 10.7 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Start-up time – fast mode FSK/FM	T_{fast}	ENRX from 0 to 1, ENRO = 1, valid data at output		0.4		ms
Start-up time – slow mode FSK/FM	T_{slow}	ENRX from 0 to 1, ENRO = 0, valid data at output		1.0		ms
Start-up time – ASK	T_{ASK}	depends on ASK detector time constant and start-up mode, valid data at output			R3•C1 4 + T_{fast} (or T_{slow})	s
Input sensitivity – FSK (narrow band)	$P_{min, n}$	B_{IF2} = 40kHz $\Delta f = \pm 15$kHz (FSK/FM) note 1		-111		dBm
Input sensitivity – FSK (wide band)	$P_{min, w}$	B_{IF2} = 150kHz $\Delta f = \pm 50$kHz (FSK/FM) note 1		-104		dBm
Input sensitivity – ASK (narrow band)	$P_{minA, n}$	B_{IF2} = 40kHz note 1		-109		dBm
Input sensitivity – ASK (wide band)	$P_{minA, w}$	B_{IF2} = 150kHz note 1		-106		dBm
Maximum input signal – FSK/FM	$P_{max, FM}$	note 1 LNA at LOW GAIN		0		dBm
Maximum input signal – ASK	$P_{max, ASK}$	note 1 LNA at LOW GAIN		-10		dBm
Spurious emission	P_{spur}				-70	dBm
Image rejection	ΔP_{imag}			65		dB
Blocking immunity	ΔP_{block}	$\Delta f_{block} > \pm$ 2MHz note 2		57		dB

Notes: 1. BER $\leq 3 \cdot 10^{-3}$
2. desired signal with FSK/FM or ASK modulation, CW blocking signal

Test Circuits

FSK Reception

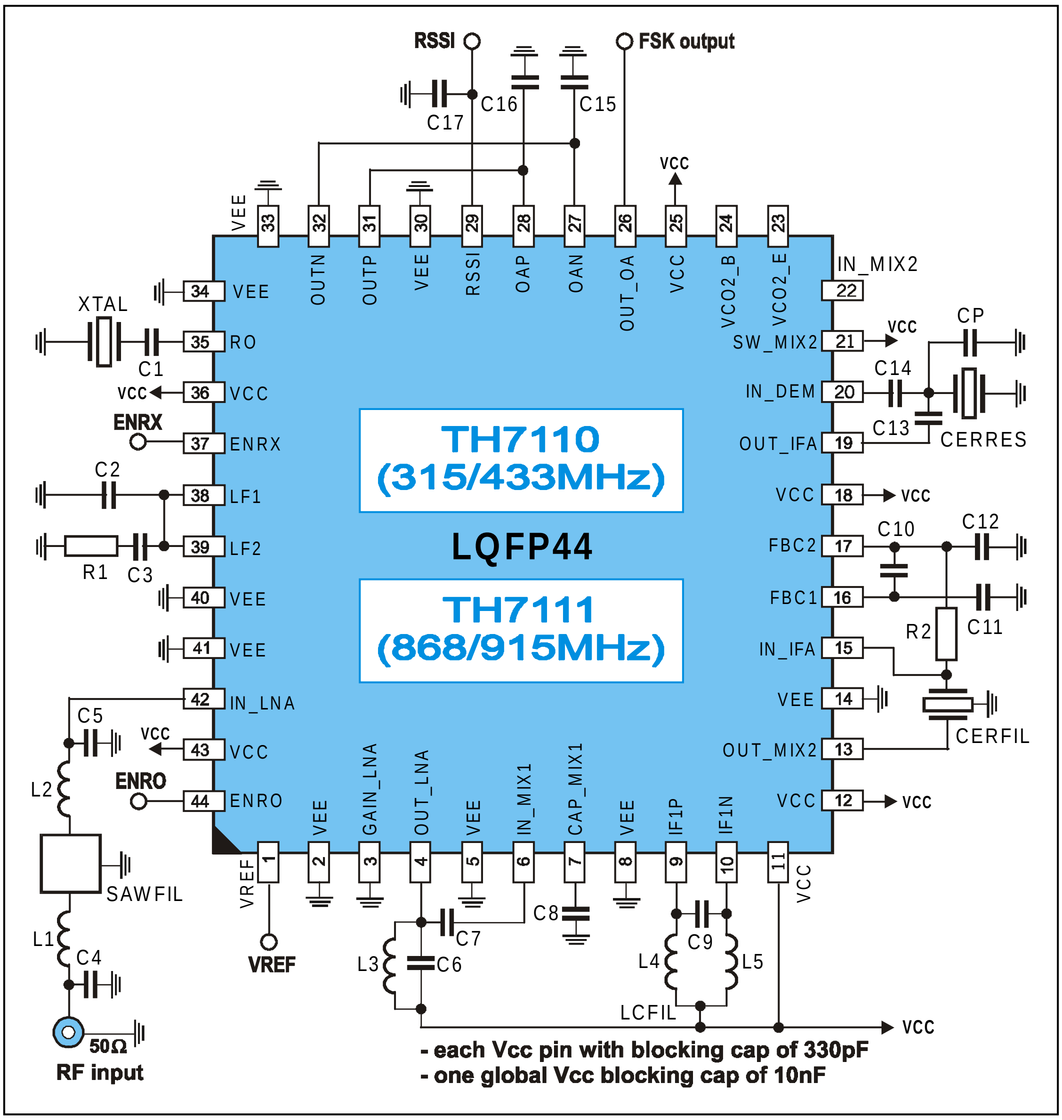


Fig. 2: Test circuit for FSK reception

FSK test circuit component list to Fig. 2

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C2	0805	NIP	±10%	loop filter capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	NIP	±5%	capacitor to match to SAW filter input
C5	0603	NIP	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C8	0603	330 pF	±10%	MIX1 blocking capacitor
C9	0603	27pF	±5%	IF1 tank capacitor
C10	0805	33 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1 nF	±10%	IFA feedback capacitor
C13	0603	10 pF	±5%	DEMOD phase-shift capacitor
C14	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	33 nF	±10%	IFA feedback capacitor
C15	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C17	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R2	0805	330 Ω	±5%	CERFIL output matching resistor
L1	0603	33 nH	±5%	inductor to match to SAW filter input
L2	0603	33 nH	±5%	inductor to match to SAW filter output
L3	0603	15 nH	±5%	LNA output tank inductor
L4	0805	100 nH	±5%	IF1 tank induction
L5	0805	100 nH	±5%	IF1 tank induction
XTAL	HC49-SMD	23.26429 MHz @ RF = 315 MHz 23.49444 MHz @ RF = 433.6 MHz	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF
SAWFIL	QCC8C	B3551 @ RF = 315 MHz B3555 @ RF = 433.6 MHz	±175 kHz B_{3dB} = 900kHz ±100 kHz B_{3dB} = 860kHz (f_0 = 433.92MHz)	low-loss SAW filters from EPCOS
CERFIL	leaded type SMD type	SFE10.7MV @ B_{IF2} = 40 kHz SFECV10.7MJA @ B_{IF2} = 150 kHz	TBD ±40 kHz	ceramic filters from Murata
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

FM Reception

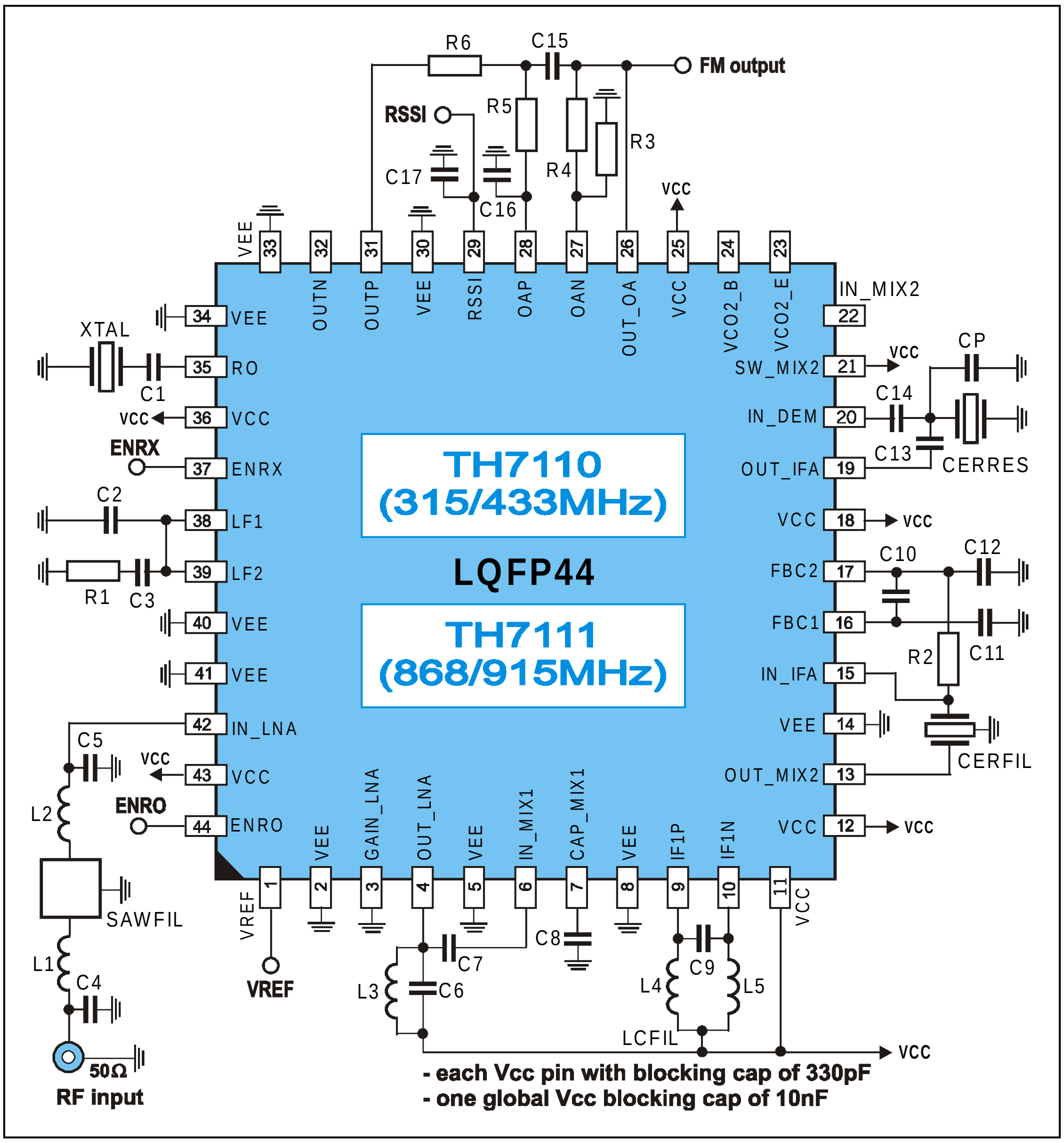


Fig. 3: Test circuit for FM reception

FM test circuit component list to Fig. 3

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C2	0805	NIP	±10%	loop filter capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	NIP	±5%	capacitor to match to SAW filter input
C5	0603	NIP	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C8	0603	330 pF	±10%	MIX1 blocking capacitor
C9	0603	27 pF	±5%	IF1 tank capacitor
C10	0805	33 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1 nF	±10%	IFA feedback capacitor
C13	0603	10 pF	±5%	DEMOD phase-shift capacitor
C14	0603	680 pF	±10%	DEMOD coupling capacitor
C15	0805	100 pF	±5%	Sallen-Key low-pass filter capacitor, to set cut-off frequency
C16	0805	100 pF	±5%	Sallen-Key low-pass filter capacitor, to set cut-off frequency
C17	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R2	0805	330 Ω	±5%	CERFIL output matching resistor
R3	0805	12 kΩ	±5%	Sallen-Key filter resistor, to set desired filter characteristic
R4	0805	6.8 kΩ	±5%	Sallen-Key filter resistor, to set desired filter characteristic
R5	0805	33 kΩ	±5%	Sallen-Key filter resistor, to set cut-off frequency
R6	0805	33 kΩ	±5%	Sallen-Key filter resistor, to set cut-off frequency
L1	0603	33 nH	±5%	inductor to match to SAW filter input
L2	0603	33 nH	±5%	inductor to match to SAW filter output
L3	0603	15 nH	±5%	LNA output tank inductor
L4	0603	100 nH	±5%	IF1 tank inductor
L5	0603	100 nH	±5%	IF1 tank inductor
XTAL	HC49-SMD	23.26429 MHz @ RF = 315 MHz 23.49444 MHz @ RF = 433.6 MHz	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF
SAWFIL	QCC8C	B3551 @ RF = 315 MHz B3555 @ RF = 433.6 MHz	±175 kHz B_{3dB} = 900kHz ±100 kHz B_{3dB} = 860kHz (f_0 = 433.92MHz)	low-loss SAW filters from EPCOS
CERFIL	leaded type SMD type	SFE10.7MV @ B_{IF2} = 40 kHz SFECV10.7MJA @ B_{IF2} = 150 kHz	TBD ±40 kHz	ceramic filters from Murata
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

ASK Reception

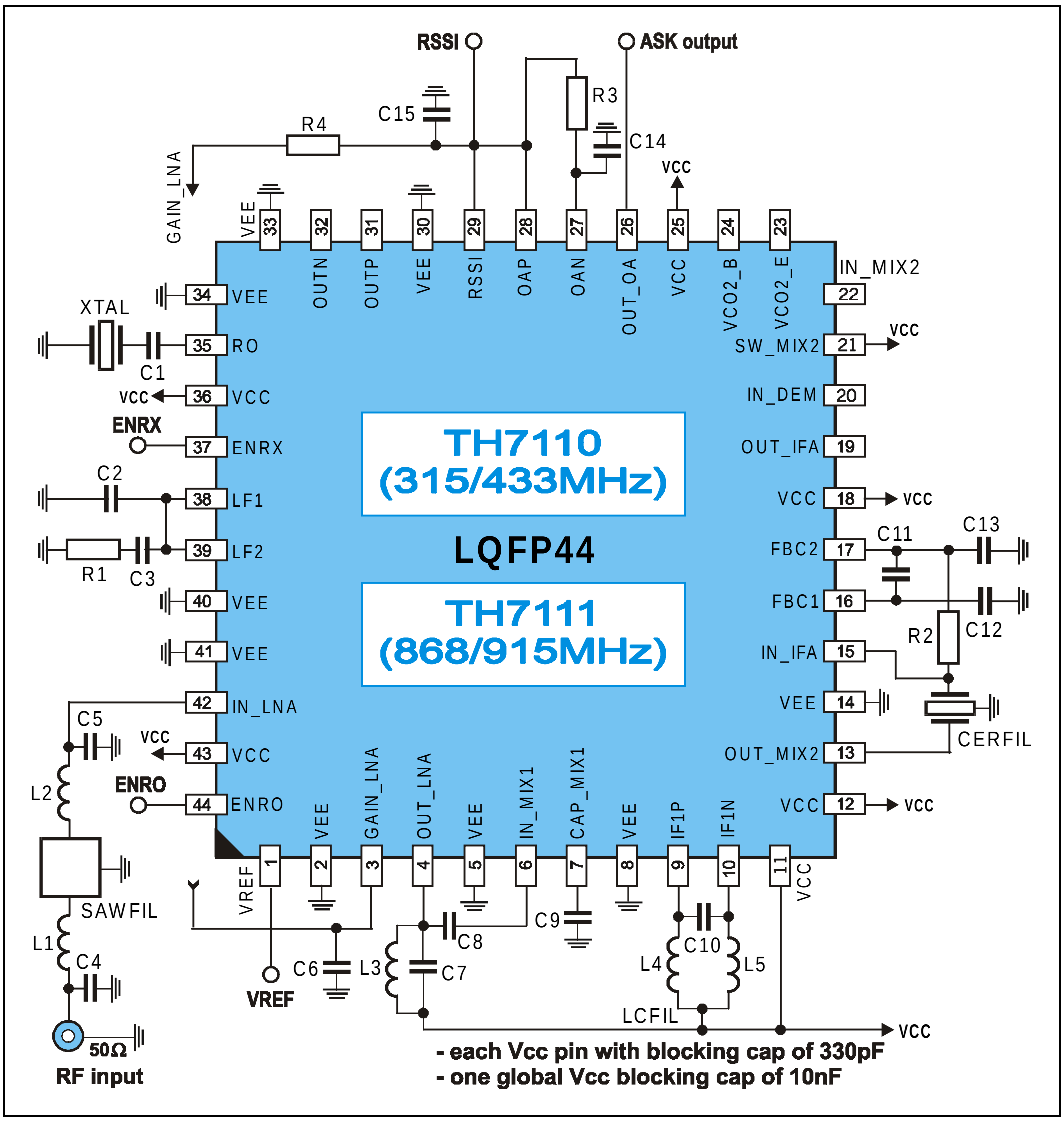


Fig. 4: Test circuit for ASK reception

ASK test circuit component list to Fig. 4

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C2	0805	NIP	±10%	loop filter capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	NIP	±5%	capacitor to match to SAW filter input
C5	0603	NIP	±5%	capacitor to match to SAW filter output
C6	0603	330 pF	±10%	AGC time constant capacitor
C7	0603	4.7 pF	±5%	LNA output tank capacitor
C8	0603	2.2 pF	±5%	MIX1 input matching capacitor
C9	0603	330 pF	±10%	MIX1 blocking capacitor
C10	0805	27 pF	±5%	IF1 tank capacitor
C11	0805	33 nF	±10%	IFA feedback capacitor
C12	0603	1 nF	±10%	IFA feedback capacitor
C13	0603	1 nF	±10%	IFA feedback capacitor
C14	0805	1 nF	±10%	ASK data slicer capacitor, depending on data rate
C15	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R2	0805	330 Ω	±5%	CERFIL output matching resistor
R3	0603	1 MΩ	±5%	ASK data slicer resistor, depending on data rate
R4	0603	15 kΩ	±5%	AGC time constant resistor
L1	0603	33 nH	±5%	inductor to match to SAW filter input
L2	0603	33 nH	±5%	inductor to match to SAW filter output
L3	0603	15 nH	±5%	LNA output tank inductor
L4	0603	100 nH	±5%	IF1 tank inductior
L5	0603	100 nH	±5%	IF1 tank inductior
XTAL	HC49-SMD	23.26429 MHz @ RF = 315 MHz 23.49444 MHz @ RF = 433.6 MHz	±25ppm calibra-tion ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF
SAWFIL	QCC8C	B3551 @ RF = 315 MHz B3555 @ RF = 433.6 MHz	±175 kHz B_{3dB} = 900kHz ±100 kHz B_{3dB} = 860kHz (f_0 = 433.92MHz)	low-loss SAW filters from EPCOS
CERFIL	leaded type SMD type	SFE10.7MV @ B_{IF2} = 40 kHz SFECV10.7MJA @ B_{IF2} = 150 kHz	TBD ±40 kHz	ceramic filters from Murata

NIP – not in place, may be used optionally

Package Dimensions

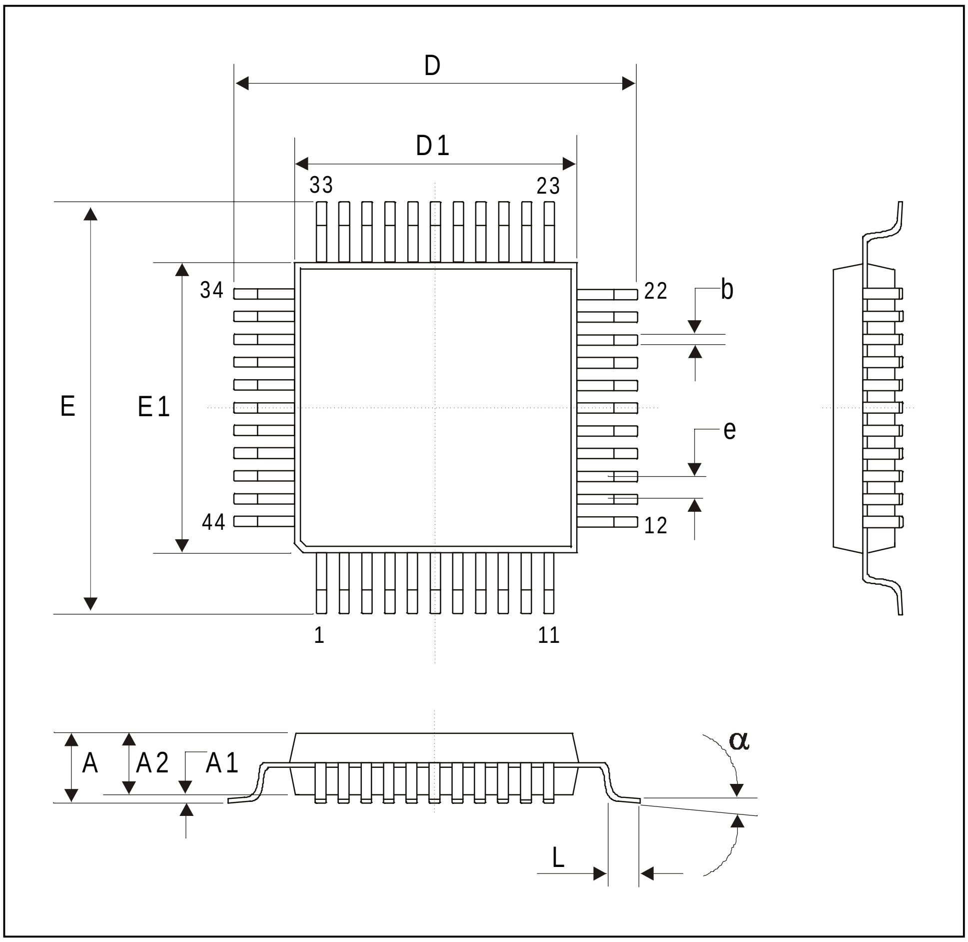


Fig. 5: LQFP44 (Low Quad Flat Package)

All Dimension in mm, coplanaríty < 0.1mm									
	E1, D1	**A**	**A1**	**A2**	**e**	**b**	**L**	**E, D**	**α**
min	10.00		0.05	1.35	0.8	0.30	0.45	12.00	0°
max		1.60	0.15	1.45		0.45	0.75		7°
All Dimension in inch, coplanaríty < 0.004”									
min	0.394		0.002	0.053	0.031	0.012	0.018	0.472	0°
max		0.630	0.006	0.057		0.018	0.030		7°

Melexis Headquarter

Melexis N.V.
Transportstraat 1
B-3680 Tessenderlo,
Belgium
Phone: +32 13 67 0780
Fax: +32 13 67 2134

Melexis Inc.
41 Locke Road
Concord, NH 03301
USA
Phone: +1 603 223 2362
Fax: +1 603 223 9614

Melexis GmbH
Haarbergstrasse 67
D-99097 Erfurt
Germany
Phone: +49 361 427 6165
Fax: +49 361 427 7614

For the latest version of this document,
Go to our website at:

www.melexis.com

Or for additional information

Contact Melexis Direct:

■ ***USA***

Melexis Inc.
41 Locke Road
Concord, NH 03301
USA
Phone: +1 603 223 2362
Fax: +1 603 223 9614
Email: sales_usa@melexis.com

■ ***Germany***

Melexis GmbH
Schiess Strasse 55
D-40549 Düsseldorf,
Germany
Phone: +49 211 536 02 0
Fax: +49 211 536 02 50
Email: sales_de@melexis.com

■ ***United Kingdom***

Silicon Concepts
PCB Lynchborough Road
Hampshire GU30 7SB
United Kingdom
Phone: +44 1428 751 617
Fax: +44 1428 751 603
Email: sales_uk@melexis.com

■ ***France***

Melexis France
Tour Arago, 5 rue Bellini
92806 Puteaux La Defense
France
Phone: +33 147 78 11 34
Fax: +33 147 78 06 35
Email: sales_france@melexis.com

■ ***Italy***

Diamacred IRL
Via Papa Giovanni XXIII no.25
20046 Biassono
Italy
Phone: +39 039 249 4856
Fax: +39 039 491 773
Email: sales_italy@melexis.com

■ ***Japan***

Thermopile Japan Co., LTD
3-48-10 Ogikubo, Suginami-ku,
Tokyo
Phone: +81 3 3392 6961
Fax: +81 3 3392 6901
Email: sales@thermopile.co.jp

■ ***Taiwan***

Beechwood Int'l Taiwan Co.
Room 8, 17F, No.189,
Taipei, Taiwan
Phone: +886 2 2739 3322
Fax: +886 2 2739 3090
Email: sales_taiwan@melexis.com

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