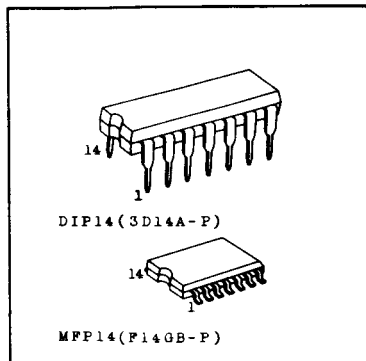
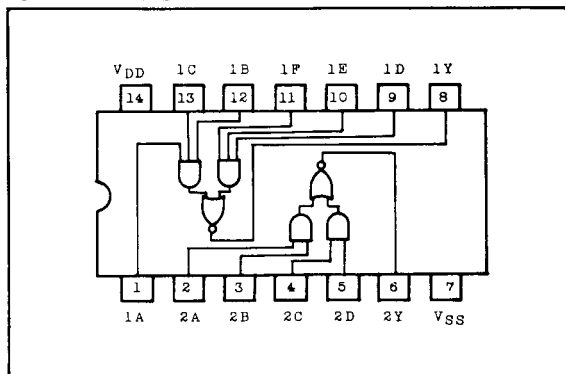


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C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H051 DUAL AND-OR-INVERT GATE



MAXIMUM RATINGS

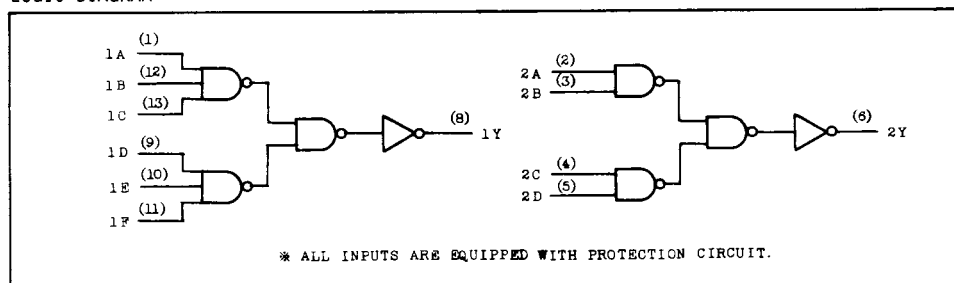
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +10	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Input Current	I _{IN}	±10	mA
Power Dissipation	PD	300 (DIP) / 180 (MFP)	mW
Storage Temperature	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C • 10 sec	

TRUTH TABLE

$$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$$

$$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$$

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0.0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	-	2.0	-	8.0	V
Input Voltage	V _{IN}	-	0	-	V _{DD}	V
Operating Temperature	T _{opr}	-	-40	-	85	°C

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ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V)

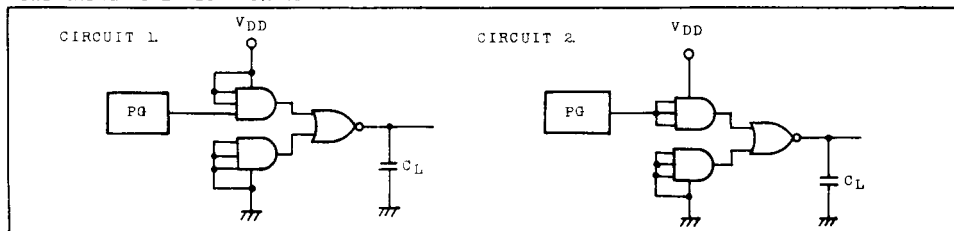
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I _{OH}	V _{OH} =4.6V V _{IN} =V _{SS} , V _{DD}	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I _{OL}	V _{OL} =0.4V V _{IN} =V _{SS} , V _{DD}	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage	"H" Level	V _{IH} I _{OUT} < 1μA	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level	V _{IL} V _{OUT} =0.5V V _{OUT} =4.5V	5	-	1.0	-	-	1.0	-	1.0	
Input Current	"H" Level	I _{IH} V _{IH} =8.0V	8	-	0.3	-	10 ⁻⁵	0.3	-	1.0	μA
	"L" Level	I _{IL} V _{IL} =0.0V	8	-	-0.3	-	-10 ⁻⁵	-0.3	-	-1.0	
Quiescent Supply Current	I _{DD}	*V _{IN} =V _{SS} , V _{DD}	5	-	2.0	-	10 ⁻³	2.0	-	10.0	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (T_a=25°C, V_{SS}=0.0V, C_L=15pF)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t _{or}	Circuit 1	5	-	14	30	ns
Output Fall Time		t _{of}	Circuit 1	5	-	10	30	
Propagation Delay Time	(Low-High)	t _{PLH}	Circuit 1	5	-	24	36	ns
	(High-Low)	t _{pHL}		5	-	20	30	
Propagation Delay Time	(Low-High)	t _{pLH}	Circuit 2	5	-	18	28	ns
	(High-Low)	t _{pHL}		5	-	22	33	
Input Capacitance		C _{IN}			-	5	-	pF

SWITCHING TIME TEST CIRCUIT



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SWITCHING TIME TEST WAVEFORM

