Contents

64-bit THERMAL HEAD DRIVER S-4621A

The S-4621A is a CMOS thermal print head driver containing a 64-bit shift register and a latch. It can be used for general purpose because "H" or "L" can be selected for the latch and the driver enable. It is ideal for the bar-code printer and the thermal print head of high-speed printing because of its large driver output current of 50 mA.

■ Features

- Low current consumption : 0.4 mA typ.
  (f_{CLK}=5 MHz, SI: fixed)
- High speed operation : 7 MHz (chip)
  5 MHz (cascade connection)
- Driver output voltage : 36 V max.
- Driver output current : 50 mA max.
- 64-bit shift register and latch are built in
- Driver enable
- Driver-off function when supply voltage falls
- Selectable "H/L" for latch and driver enable

■ Block Diagram

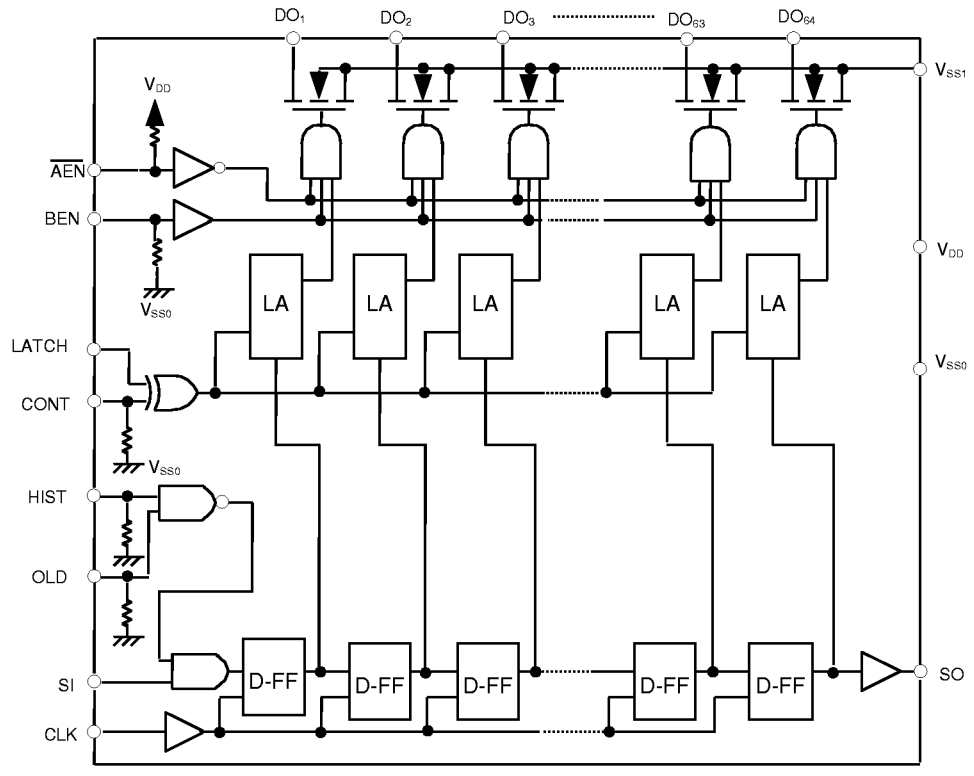

Figure 1

This IC is still under development, thus the specifications are subject to change without notice.

■ Operation

The 64-bit shift register reads the data input to SI at the rising edge of the CLOCK input.

The latch circuit operates depending on the levels of CONT and LATCH ; it reads the data of the shift register when their levels are the same, and it holds the data of the shift register when they differ.

The latch data is output to the respective drivers when $\overline{AEN}$ is low and BEN is high. The driver output transistor turns ON when the latch data is high and turns OFF when low. Turning $\overline{AEN}$ high or BEN low makes all driver output transistors go off.

All driver output transistors go off when power supply voltage becomes lower than V_{DET} regardless of all input signals.

■ Terminal Functions (Refer to the dimensions for the pad arrangement)

Table 1

No.	Name	Functions
1 to 64	DO_1 to DO_{64} (DO_n)	Driver output terminals (Nch open-drain)
65, 66, 73, 74, 82, 83	V_{SS1}	GND for driver (0 V)
71, 78	V_{DD}	Positive power supply for logic (+5 V)
67, 75	V_{SS0}	GND for logic (0 V)
77	CLK	Clock input terminal for 64-bit shift register
81	SI	Serial data input terminal for 64-bit shift register
68	SO	Serial data output terminal for 64-bit shift register
69	LATCH	Data latch signal input terminal When CONT="L" or open LATCH="L": Reads the data of the shift register LATCH="H": Holds the preceding data When CONT="H" LATCH="L": Holds the preceding data LATCH="H": Reads the data of the shift register
72	CONT	Data latch signal control terminal : Selects "H" or "L" for LATCH (pull-down resistor is built in)
76	$\overline{AEN}$	Driver enable terminal : Outputs the latch data to the driver when low (pull-up resistor is built in)
70	BEN	Driver enable terminal : Outputs the latch data to the driver when high (pull-down resistor is built in)
79	OLD	Former column serial data input terminal (A pull-up resistor is built in)
80	HIST	Former column serial data input control terminal (A pull-down resistor is built in) HIST="H" : OLD terminal is active. HIST="L" or open : Input from OLD terminal is not allowed.

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Ratings	Unit
Supply voltage	$V_{SS0,1}$ - V_{DD}	-0.4 to +7.0	V
Driver output voltage	V_{DOH}	36	V
Driver output current	I_{DOL}	50	mA
Input voltage	V_{IN}	V_{SS0}-0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	V_{SS0}-0.5 to V_{DD}+0.5	V
Max. junction temperature	T_{jMAX}	125	°C
Operating temperature range	T_{opr}	-10 to +80	°C
Storage temperature range	T_{stg}	-40 to +125	°C

■ DC Electrical Characteristics

Table 3

(Unless otherwise specified: V_{DD}=5.0 V±10%, Ta=-10 °C to 80 °C)

Parameter	Sybl	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}			4.5	5.0	5.5	V
High level input voltage	V_{IH}	*1		0.7×V_{DD}	—	V_{DD}	V
Low level input voltage	V_{IL}			V_{SS}	—	0.3×V_{DD}	V
High level input current	I_{IH}	VDD=5.0 V VIH=5.0 V Ta=25 °C	BEN, CONT,OLD,HIS	—	—	55	µA
				—	—	0.5	µA
Low level input current	I_{IL}	VDD=5.0 V VIL=0 V	$\overline{AEN}$	-55	—	—	µA
				-0.5	—	—	µA
High level output voltage	V_{OH}	SO terminal, no load		4.45	—	—	V
Low level output voltage	V_{OL}	SO terminal, no load		—	—	0.05	V
High level output current	I_{OH}	SO terminal, V_{OH}=V_{DD}-0.4 V		—	—	-0.5	mA
Low level output current	I_{OL}	SO terminal, V_{OL}=0.4 V		0.5	—	—	mA
High level driver output voltage	V_{DOH}	Heat generator resistance: 500 Ω min.		—	24	26	V
Low level driver output voltage	V_{DOL}	I_{DOL}=30 mA		—	0.7	1.5	V
Driver leakage current	I_{LEAK}	V_{DOH}=26 V Per 1-bit of driver output		—	—	1.0	µA
		V_{DOH}=26 V Per 64-bit of driver output		—	—	10	µA
Current consumption	I_{DD}	Ta= 25 °C	f_{CLK}=2 MHz,SI : fixed		0.2	0.6	mA
			f_{CLK}=5 MHz,SI : fixed		0.4	1.2	mA
			f_{CLK}=5 MHz, SI=1/2f_{CLK}		1.6	5.0	mA
Lower V_{DD} detection voltage	V_{DET}			0.8	—	4.0	V

*1 CLK : f_{CLK}=fmax duty 50%
T_{SUD}=THD=100 nsec
SI, OLD, HIS : 1/2 fmax
LATCH : T_{WLA}=100 nsec
Others : DC level

■ AC Electrical Characteristics

Table 4

(Unless otherwise specified: V_{DD}=5.0 V±10%, Ta=-10 °C to 80 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse width	t_{WCLK}		70	—	—	ns
Data setup time	t_{SUD}	$V_{IH}=V_{DD}$, $V_{IL}=V_{SS0}$	40	—	—	ns
Data hold time	t_{HD}	$V_{IH}=V_{DD}$, $V_{IL}=V_{SS0}$	40	—	—	ns
Latch pulse width	t_{WLA}		100	—	—	ns
Latch setup time	t_{SULA}		100	—	—	ns
CLK-SO propagation delay time	t_{dSO}	C_L=3 pF	—	—	120	ns
EN-DOn propagation delay time	t_{dDO}	R_L=1.0 kΩ, V_{DOH}=24 V	—	—	10.5	µs
DOn rise time	t_{rDO}	R_L=1.0 kΩ, V_{DOH}=24 V	—	2.0	6.0	µs
DOn fall time	t_{fDO}	R_L=1.0 kΩ, V_{DOH}=24 V	—	3.5	10.0	µs
Clock frequency	f_{CLK}	When cascade connection	—	—	5.0	MHz

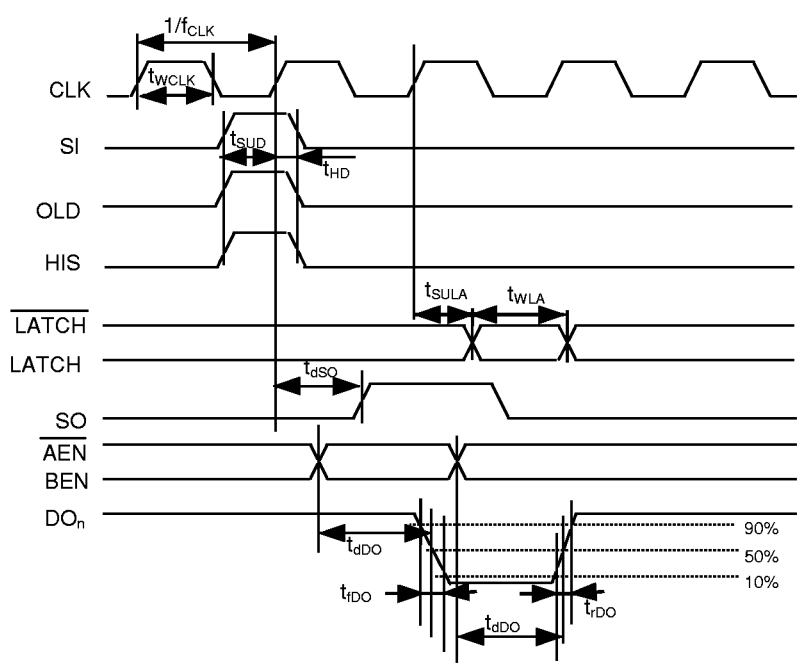

Figure 2

■ Dimensions

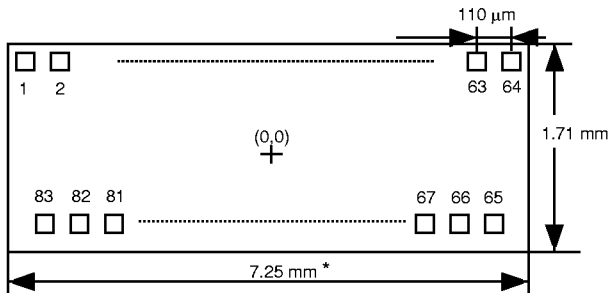

Figure 3

Pad size : 80 μm × 80 μm
(passivation opening)
Pad pitch : 110 μm (driver output pad)
Chip thickness : 350±30 μm

*Before dicing

■ Pad Coordinates (The origin of the coordinate axes is the center of the chip)

Table 5

Unit: μm

Pad No.	Name	X	Y	Pad No.	Name	X	Y	Pad No.	Name	X	Y
1	DO_1	-3465	257.5	29	DO_{29}	-385	257.5	57	DO_{57}	2695	257.5
2	DO_2	-3355	257.5	30	DO_{30}	-275	257.5	58	DO_{58}	2805	257.5
3	DO_3	-3245	257.5	31	DO_{31}	-165	257.5	59	DO_{59}	2915	257.5
4	DO_4	-3135	257.5	32	DO_{32}	-55	257.5	60	DO_{60}	3025	257.5
5	DO_5	-3025	257.5	33	DO_{33}	55	257.5	61	DO_{61}	3135	257.5
6	DO_6	-2915	257.5	34	DO_{34}	165	257.5	62	DO_{62}	3245	257.5
7	DO_7	-2805	257.5	35	DO_{35}	275	257.5	63	DO_{63}	3355	257.5
8	DO_8	-2695	257.5	36	DO_{36}	385	257.5	64	DO_{64}	3465	257.5
9	DO_9	-2585	257.5	37	DO_{37}	495	257.5	65	V_{SS1}	3455	-257.5
10	DO_{10}	-2475	257.5	38	DO_{38}	605	257.5	66	V_{SS1}	3335	-257.5
11	DO_{11}	-2365	257.5	39	DO_{39}	715	257.5	67	V_{SS}	2855	-257.5
12	DO_{12}	-2255	257.5	40	DO_{40}	825	257.5	68	SO	2455	-257.5
13	DO_{13}	-2145	257.5	41	DO_{41}	935	257.5	69	LATCH	2005	-125.0
14	DO_{14}	-2035	257.5	42	DO_{42}	1045	257.5	70	BEN	1605	-257.5
15	DO_{15}	-1925	257.5	43	DO_{43}	1155	257.5	71	V_{DD}	1135	-257.5
16	DO_{16}	-1815	257.5	44	DO_{44}	1265	257.5	72	CONT	685	-257.5
17	DO_{17}	-1705	257.5	45	DO_{45}	1375	257.5	73	V_{SS1}	60	-242.5
18	DO_{18}	-1595	257.5	46	DO_{46}	1485	257.5	74	V_{SS1}	-60	-242.5
19	DO_{19}	-1485	257.5	47	DO_{47}	1595	257.5	75	V_{SS0}	-460	-257.5
20	DO_{20}	-1375	257.5	48	DO_{48}	1705	257.5	76	$\overline{AEN}$	-940	-257.5
21	DO_{21}	-1265	257.5	49	DO_{49}	1815	257.5	77	CLK	-1360	-257.5
22	DO_{22}	-1155	257.5	50	DO_{50}	1925	257.5	78	HIST	-1600	-257.5
23	DO_{23}	-1045	257.5	51	DO_{51}	2035	257.5	79	OLD	-2020	-257.5
24	DO_{24}	-935	257.5	52	DO_{52}	2145	257.5	80	V_{DD}	-2445	-257.5
25	DO_{25}	-825	257.5	53	DO_{53}	2255	257.5	81	SI	-2845	-257.5
26	DO_{26}	-715	257.5	54	DO_{54}	2365	257.5	82	V_{SS1}	-3335	-257.5
27	DO_{27}	-605	257.5	55	DO_{55}	2475	257.5	83	V_{SS1}	-3455	-257.5
28	DO_{28}	-495	257.5	56	DO_{56}	2585	257.5				