LOW VOLTAGE OPERATION DUAL H BRIDGE DRIVER

■ GENERAL DESCRIPTION

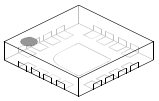
The NJU7381A is a dual H-bridge driver IC that features low voltage operation and low quiescent current.

The control method is 2 logic Inputs (2-IN) that includes standby mode.

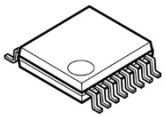
The independent comparator circuit can be used for position sensing signal processing and the others.

Small package makes the NJU7381A suitable for small stepper motor and DC motor, such as portable applications.

■ PACKAGE OUTLINE



NJU7381AMJE
(EQFN16-JE)

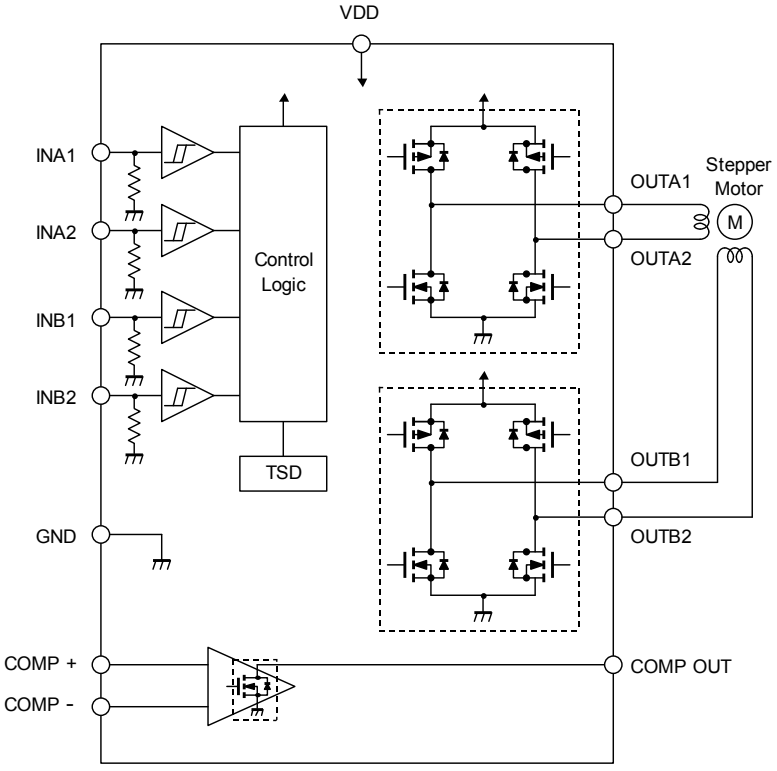


NJU7381AV
(SSOP16)

■ FEATURES

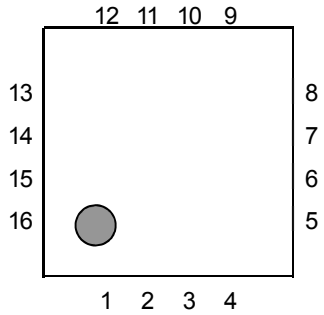
- Supply Voltage : V_{DD}=1.8V to 5.5V
- Output Current : I_O=200mA (Continuous)
  I_O=400mA (Peak)
- Output ON Resistance : $R_{O(H+L)}$=1.25Ω typ. at V_{DD}=3.3V
  $R_{O(H+L)}$=1.95Ω typ. at V_{DD}=1.8V
- Low Quiescent Current : 60μA typ. at V_{DD}=3.3V
- 2 Logic Inputs Control (2-IN)
- Stand-by Function (At no-input signal)
- Built-in Comparator Circuit
- Protection Circuit : Thermal Shutdown Circuit (TSD)
- Package Outline : EQFN16-JE, SSOP16

■ BLOCK DIAGRAM



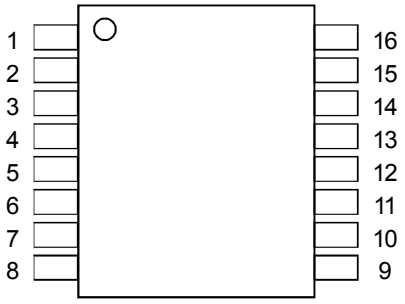
■ PIN CONFIGURATION

EQFN16-JE

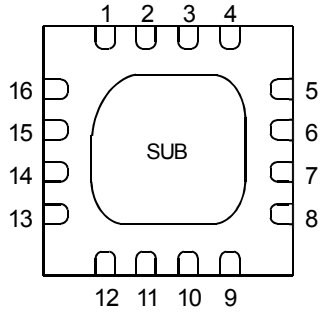


Top View

SSOP16



Top View



Bottom View

■ PIN DESCRIPTION

PIN No.		PIN NAME	FUNCTION	NOTES
EQFN16	SSOP16			
1	2	INB1	Bch Logic Input Pin 1	-
2	3	INB2	Bch Logic Input Pin 2	-
3,11	4,12	VDD	Power Supply Pin	Both pins must be connected together externally.
4	5	INA2	Ach Logic Input Pin 2	-
5	6	INA1	Ach Logic Input Pin 1	-
6	7	OUTA2	Ach Output Pin 2	-
7,15	8,16	GND	Ground Pin	Both pins must be connected together externally.
8	9	OUTA1	Ach Output Pin 1	-
9	11	COMP OUT	Comparator Output Pin	When not using, it should be set to open.
10	10	NC	No Connection	Not Internally Connected
12	13	COMP+	Comparator Non-inverted Input Pin	When not using, it should be connected to VDD.
13	14	COMP-	Comparator Inverted Input Pin	When not using, it should be connected to GND.
14	15	OUTB1	Bch Output Pin 1	-
16	1	OUTB2	Bch Output Pin 2	-
SUB	-	SUB	Back Side Thermal PAD (SUB)	The PAD is connected with the internal VDD. It must be set to open or connected to VDD.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25ºC)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTES
Supply Voltage	V_{DD}	7	V	-
Logic Input Voltage	V_{ID}	-0.3 to V_{DD}+0.3	V	-
Motor Output Current (Peak)	I_{OPEAK}	400	mA	Per channel
		800	mA	Ach & Bch parallel connection
Comparator Output Current	I_{CO}	10	mA	-
Comparator Output Voltage	V_{CO}	7	V	-
Operating Ambient Temperature	Topr	-40 to + 85	ºC	-
Junction Temperature	Tj	-40 to +150	ºC	-
Storage Temperature	Tstg	-50 to +150	ºC	-
Power Dissipation (EQFN16-JE)	P_D	720	mW	2 Layers on PCB (*1)
		1800		4 Layers on PCB (*2)
Power Dissipation (SSOP16)	P_D	300	mW	Device itself
		610		2 Layers on PCB (*3)
		780		4 Layers on PCB (*4)

*1: Mounted on glass epoxy board based on EIA/JEDEC. (101.5×114.5×1.6mm, FR-4, 2Layers, connected exposed PAD)

*2: Mounted on glass epoxy board on EIA/JEDEC. (101.5×114.5×1.6mm, FR-4, 4Layers, Inner Cu area : 99.5×99.5mm, In addition thermal via holes, connected exposed PAD)

*3: Mounted on glass epoxy board based on EIA/JEDEC. (76.2×114.3×1.6mm, FR-4, 2Layers)

*4: Mounted on glass epoxy board based on EIA/JEDEC. (76.2×114.3×1.6mm, FR-4, 4Layers, Inner Cu area : 74.2×74.2mm)

■ RECOMMENDED OPERATING CONDITIONS

(V_{DD}=3.3V, Ta=25ºC)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage 1	V_{DD1}	Not using comparator block (*5)	1.8	-	5.5	V
Supply Voltage 2	V_{DD1}	Using comparator block (*5)	2.0	-	5.5	V
Motor Output Current (Continuous)	I_O	Per channel	-	-	200	mA
		Ach & Bch parallel connection	-	-	400	mA

*5: Output voltage may not be provided enough depending on output current level, please review output ON resistance spec.

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=3.3V, Ta=25ºC)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
■ GENERAL						
Quiescent Current 1	I_{DD1}		-	60	120	µA
Quiescent Current 2	I_{DD2}	V_{DD}=1.8V	-	50	100	µA
Quiescent Current at Stand-by	I_{STB}		-	1	3	µA
Thermal Shutdown Temperature	T_{TSD}		-	190	-	ºC
Thermal Shutdown Hysteresis	T_{HYS}		-	40	-	ºC
■ LOGIC BLOCK						
H Level Input Voltage 1	V_{IH1}		2.4	-	V_{DD}	V
H Level Input Voltage 2	V_{IH2}	V_{DD}=1.8V	1.4	-	V_{DD}	V
L Level Input Voltage 1	V_{IL1}		0	-	0.8	V
L Level Input Voltage 2	V_{IL2}	V_{DD}=1.8V	0	-	0.4	V
Input Hysteresis Width	V_{IHYS}		-	0.2	-	V
H Level Input Current	I_{IH}	Per 1 Input	22	33	55	µA
L Level Input Current	I_{IL}	Per 1 Input	-	-	200	nA
Input Pull Down Resistance	R_{IN}		60	100	150	kΩ
Input Pulse Width	tp		2	-	-	µs
■ DRIVER BLOCK						
High Side Output ON Resistance 1	R_{ONH1}	I_O=200mA	-	0.75	1.0	Ω
High Side Output ON Resistance 2	R_{ONH2}	V_{DD}=2.1V, I_O=200mA	-	1.0	1.35	Ω
High Side Output ON Resistance 3	R_{ONH3}	V_{DD}=1.8V, I_O=200mA	-	1.2	1.6	Ω
Low Side Output ON Resistance 1	R_{ONL1}	I_O=200mA	-	0.5	0.7	Ω
Low Side Output ON Resistance 2	R_{ONL2}	V_{DD}=2.1V, I_O=200mA	-	0.65	0.9	Ω
Low Side Output ON Resistance 3	R_{ONL3}	V_{DD}=1.8V, I_O=200mA	-	0.75	1.05	Ω
Parallel Connection High Side Output ON Resistance 1	R_{PONH1}	Ach & Bch Parallel Connection, I_O=400mA	-	0.38	0.5	Ω
Parallel Connection High Side Output ON Resistance 2	R_{PONH2}	Ach & Bch Parallel Connection, V_{DD}=2.1V, I_O=400mA	-	0.5	0.68	Ω
Parallel Connection High Side Output ON Resistance 3	R_{PONH3}	Ach & Bch Parallel Connection, V_{DD}=1.8V, I_O=400mA	-	0.6	0.8	Ω
Parallel Connection Low Side Output ON Resistance 1	R_{PONL1}	Ach & Bch Parallel Connection, I_O=400mA	-	0.25	0.35	Ω
Parallel Connection Low Side Output ON Resistance 2	R_{PONL2}	Ach & Bch Parallel Connection, V_{DD}=2.1V, I_O=400mA	-	0.33	0.45	Ω
Parallel Connection Low Side Output ON Resistance 3	R_{PONL3}	Ach & Bch Parallel Connection, V_{DD}=1.8V, I_O=400mA	-	0.38	0.53	Ω
R_{ONH} Temperature Coefficient	$\Delta R_{ONH}/\Delta Tj$	Tj=40~125ºC, I_O=200mA	-	4.0	-	mΩ/ºC
R_{ONL} Temperature Coefficient	$\Delta R_{ONL}/\Delta Tj$	Tj=40~125ºC, I_O=200mA	-	3.0	-	mΩ/ºC
High Side Reverse Voltage	V_{ORH}	I_O=-200mA	-	0.85	1.0	V
Low Side Reverse Voltage	V_{ORL}	I_O=-200mA	-	0.75	0.9	V
High Side Leak Current	I_{OLEAKH}	V_{DD}=7.0V	-	-	1	µA
Low Side Leak Current	I_{OLEAKL}	V_{DD}=7.0V	-	-	1	µA
Output Turn ON Time	t_{ON}		200	400	600	ns
Output Turn OFF Time	t_{OFF}		5	40	80	ns
Dead Time	td		195	360	520	ns
■ COMPARATOR BLOCK						
Input Offset Voltage	V_{IO}		-12	-	+12	mV
Input Bias Current	I_{IB}		-	1	-	pA
Common Mode Input Voltage Range	V_{ICM}		0	-	V_{DD}-0.5	V
Output Voltage	Vsat	RL=10kΩ	-	0.1	-	V
Output Leak Current	I_{COLEAK}	V_{CO}=5.5V	-	-	1	µA

■ THERMAL RESISTANCE

• EQFN16-JE

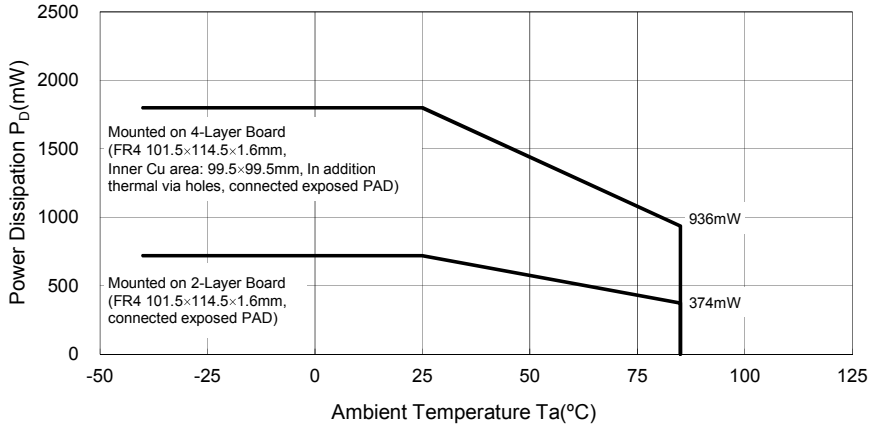
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Junction - Ambient Thermal Resistance 1	θ_{ja_1}	Mounted on glass epoxy board based on EIA/JEDEC. (101.5×114.5×1.6mm, FR-4, 2Layers, connected exposed PAD)	-	-	173	ºC/W
Junction – Case Surface Thermal Resistance 1	Ψ_{jt_1}		-	21	-	ºC/W
Junction - Ambient Thermal Resistance 2	θ_{ja_2}	Mounted on glass epoxy board based on EIA/JEDEC. (101.5×114.5×1.6mm, FR-4, 4Layers, Inner Cu area : 99.5×99.5mm, In addition thermal via holes, connected exposed PAD)	-	-	69	ºC/W
Junction – Case Surface Thermal Resistance 2	Ψ_{jt_2}		-	11	-	ºC/W

• SSOP16

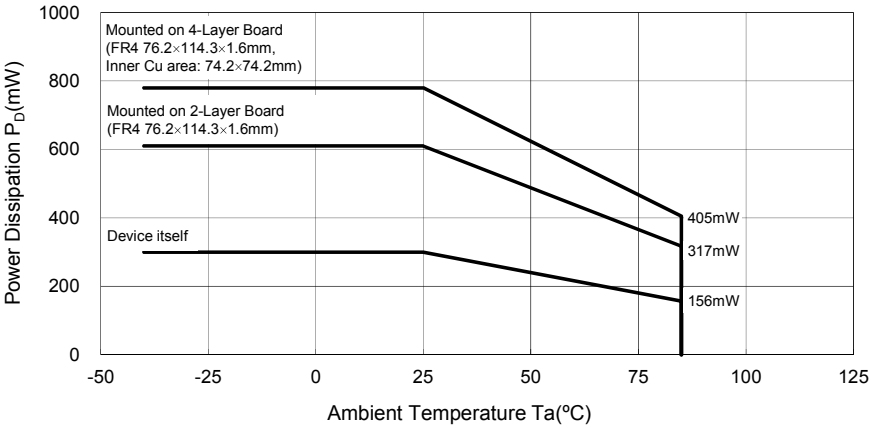
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Junction - Ambient Thermal Resistance 1	θ_{ja_1}	Mounted on glass epoxy board based on EIA/JEDEC. (76.2×114.3×1.6mm, FR-4, 2Layers)	-	-	204	ºC/W
Junction – Case Surface Thermal Resistance 1	Ψ_{jt_1}		-	35	-	ºC/W
Junction - Ambient Thermal Resistance 2	θ_{ja_2}	Mounted on glass epoxy board based on EIA/JEDEC. (76.2×114.3×1.6mm, FR-4, 4Layers, Inner Cu area : 74.2×74.2mm)	-	-	160	ºC/W
Junction – Case Surface Thermal Resistance 2	Ψ_{jt_2}		-	26	-	ºC/W

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

NJU7381AMJE P_D vs. Ta
(Topr=-40 to +85ºC, Tj=150ºC)



NJU7381AV P_D vs. Ta
(Topr=-40 to 85ºC, Tj=150ºC)



■ INPUT - OUTPUT TRUTH TABLE

INPUT				OUTPUT				Comparator Circuit	NOTES	
INA1	INA2	INB1	INB2	OUTA1	OUTA2	OUTB1	OUTB2			
ALL L				OFF	OFF	OFF	OFF	STOP (Output OFF)	Standby	
L	L	-		OFF	OFF	-		Normal Operation	Ach	OFF(Fast Decay)
H	L			H	L					CW
L	H			L	H					CCW
H	H			H	H					Brake(Slow Decay)
-		L	L	-		OFF	OFF		Bch	OFF(Fast Decay)
		H	L			H	L			CW
		L	H			L	H			CCW
		H	H			H	H			Brake(Slow Decay)
Don't Care				OFF	OFF	OFF	OFF		TSD	

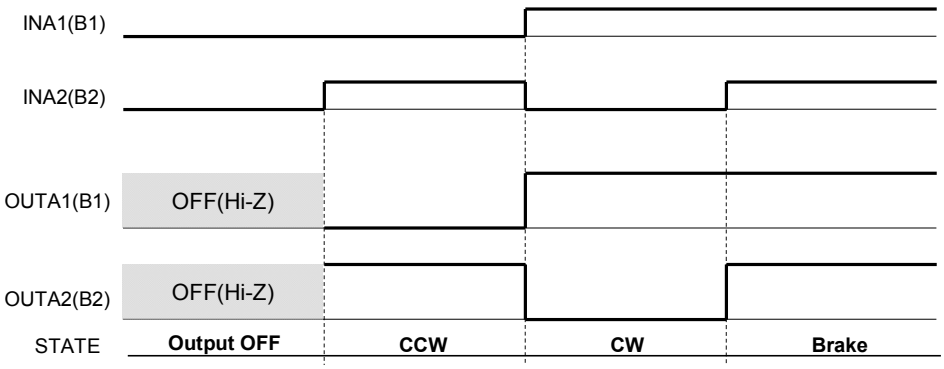
*OFF=Hi-Z

■ COMPARATOR TRUTH TABLE (Normal Operation)

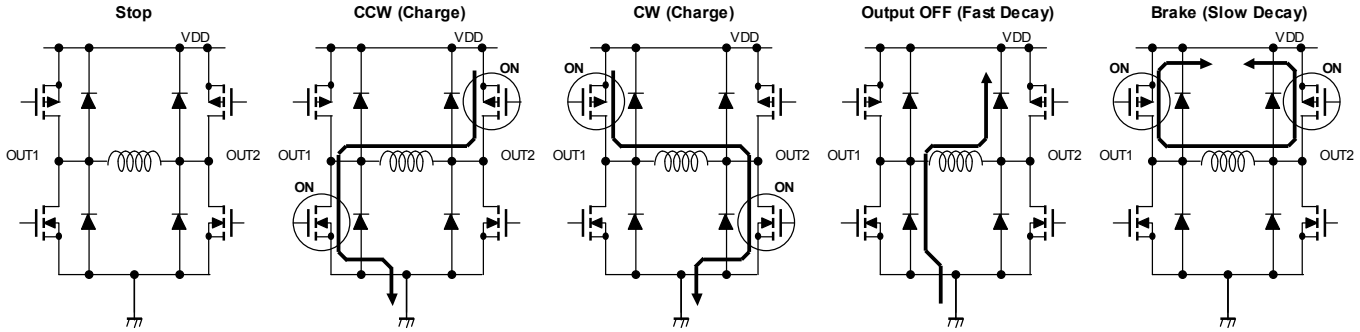
INPUT		OUTPUT	NOTES
COMP+	COMP-	COMPOUT	
H	L	OFF	FET: OFF Operation
L	H	L	FET: ON Operation

*OFF=Hi-Z

■ BASIC OPERATION TIMING CHART

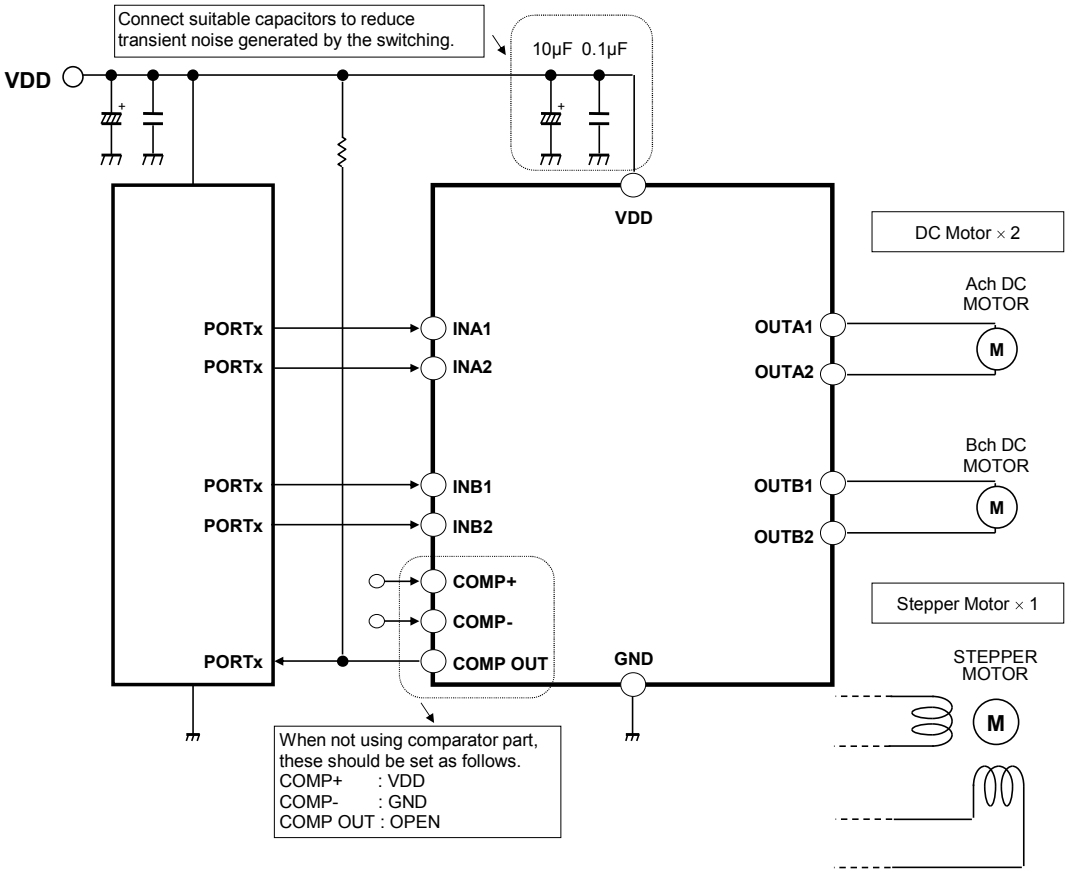


■ BASIC OUTPUT OPERATION PATTERN

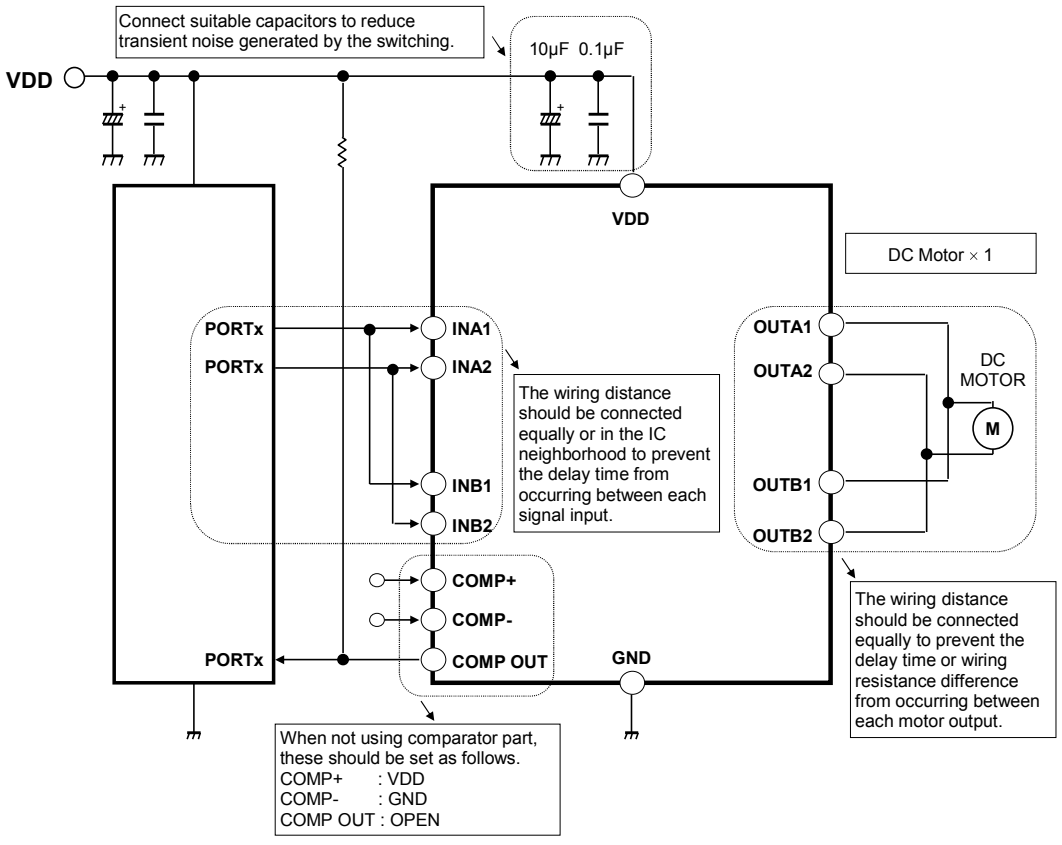


■ TYPICAL APPLICATIONS

• STANDARD

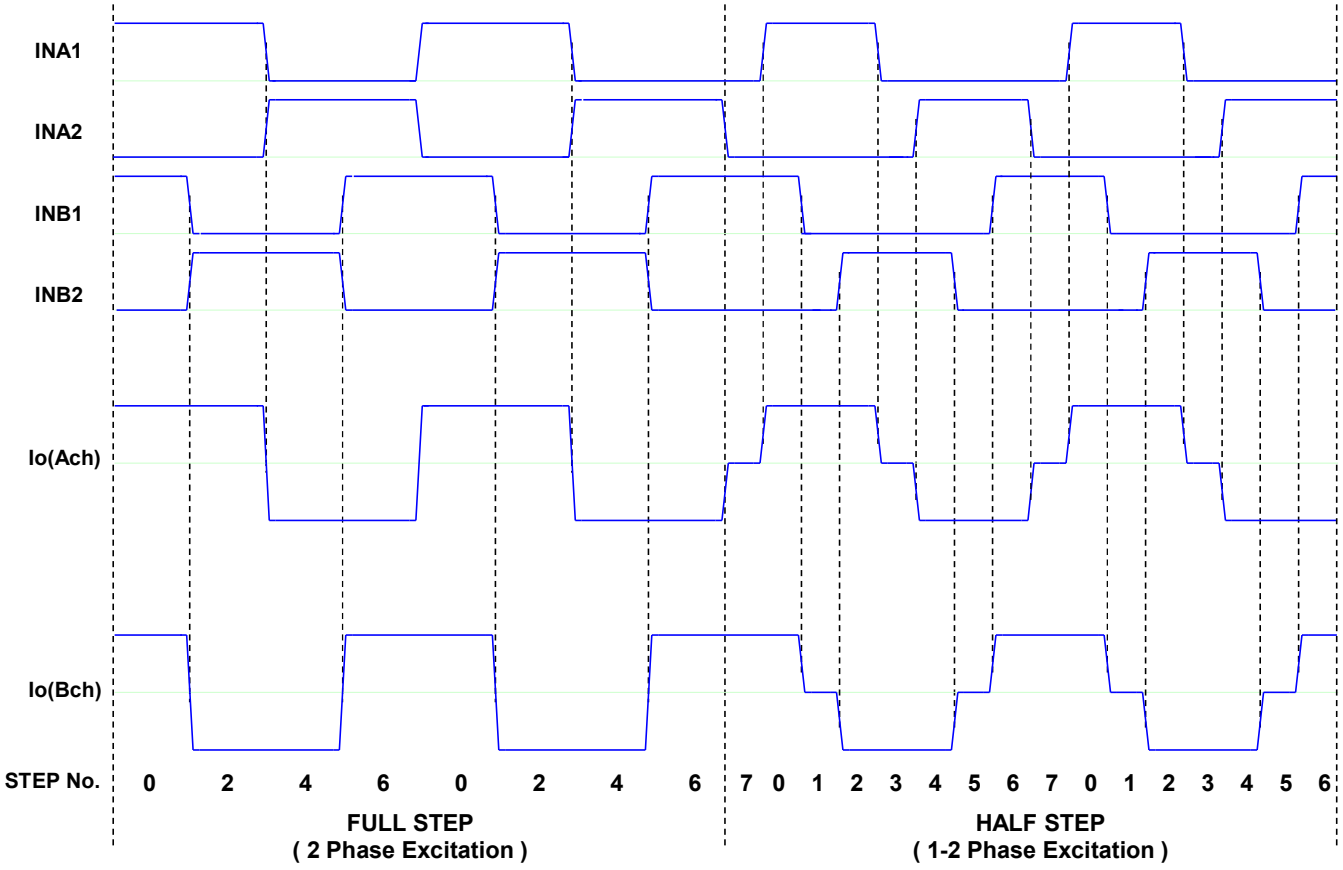


• PARALLEL CONNECTION (Boost Output Current)

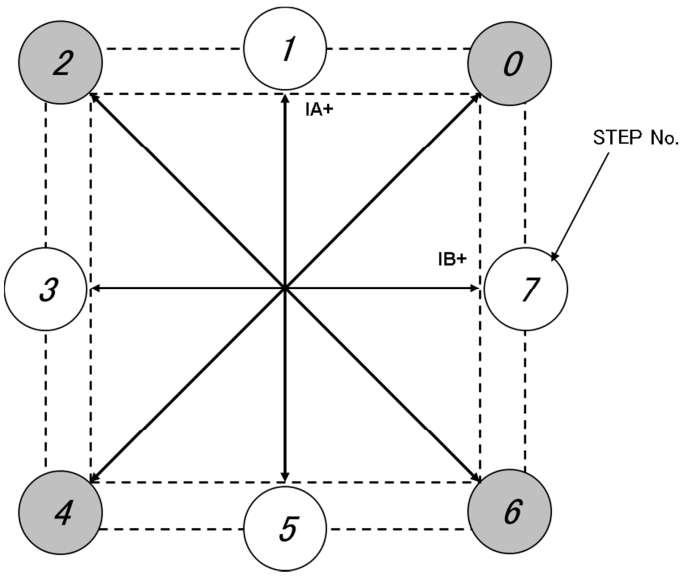


■ STEPPER MOTOR DRIVE APPLICATION

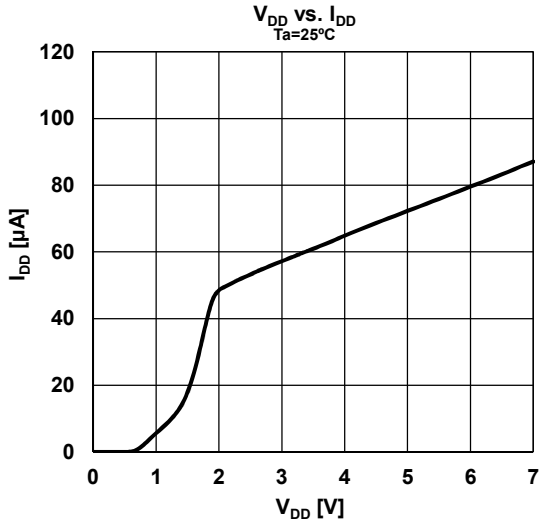
• TIMIG CHART

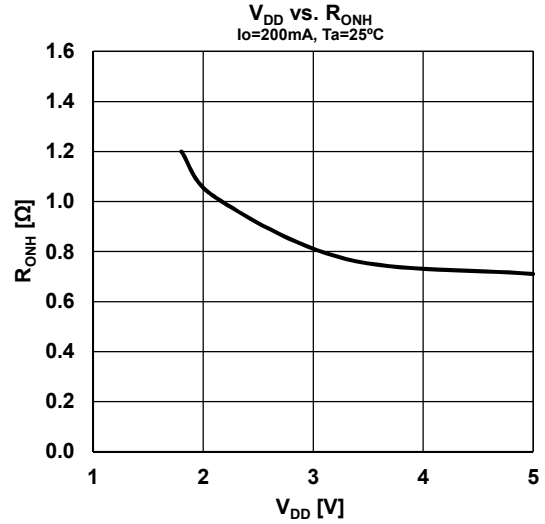


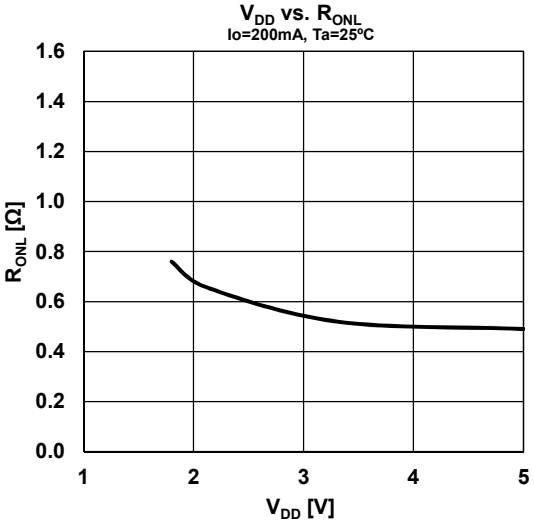
• ROTER POSITION (STEP No.)

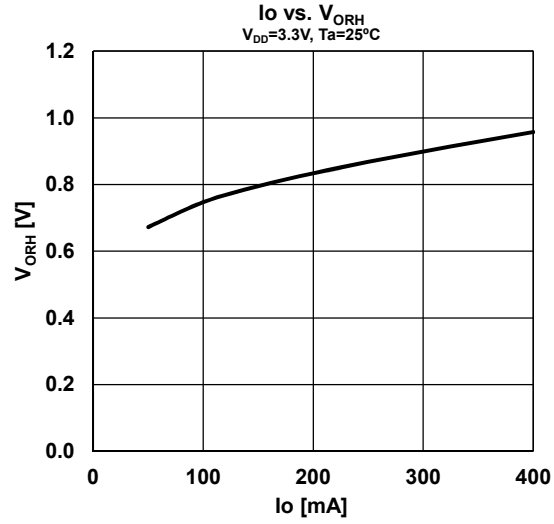


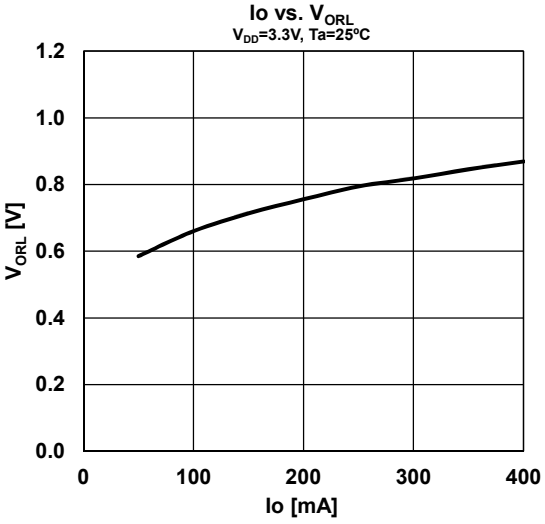
■ TYPICAL CHARACTERISTICS











■ TYPICAL CHARACTERISTICS