MTC-20285

PRELIMINARY

ISDN/IDSL + USB Terminal Controller

Advance Information

This document describes a product presently under development. Specifications are included as a guide only. Alcatel Microelectronics reserves the right to make changes without notification.

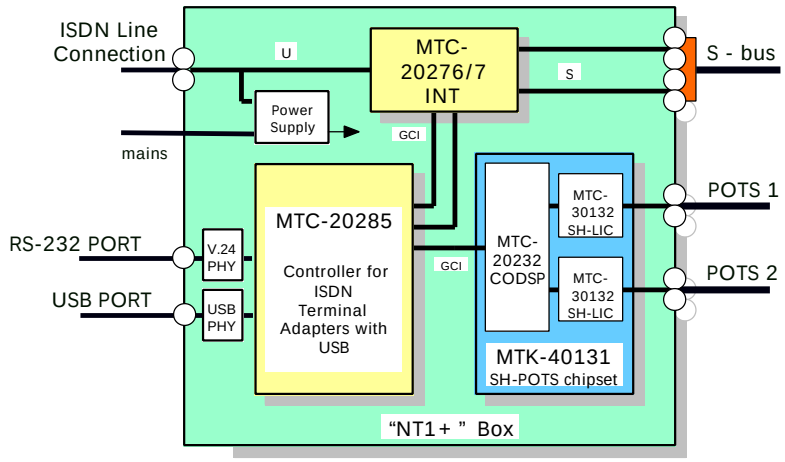
Key features:

- Integrated 32 MHz ARM7TDMI RISC processor core
- Integrated USB controller
- 16 or 8 bit memory bus
- 4Kbyte, 32-bit 0 wait-state RAM on board
- 5, full-duplex HDLC formatters with deep FIFOs (transparent mode via FIFOs)
- 3-way GCI interface and router
- 239.4 kb UART with full-duplex 16 byte FIFOs
- 24-bits user parallel I/O ports
- ISDN and application software available
- 144 pin PQFP package style

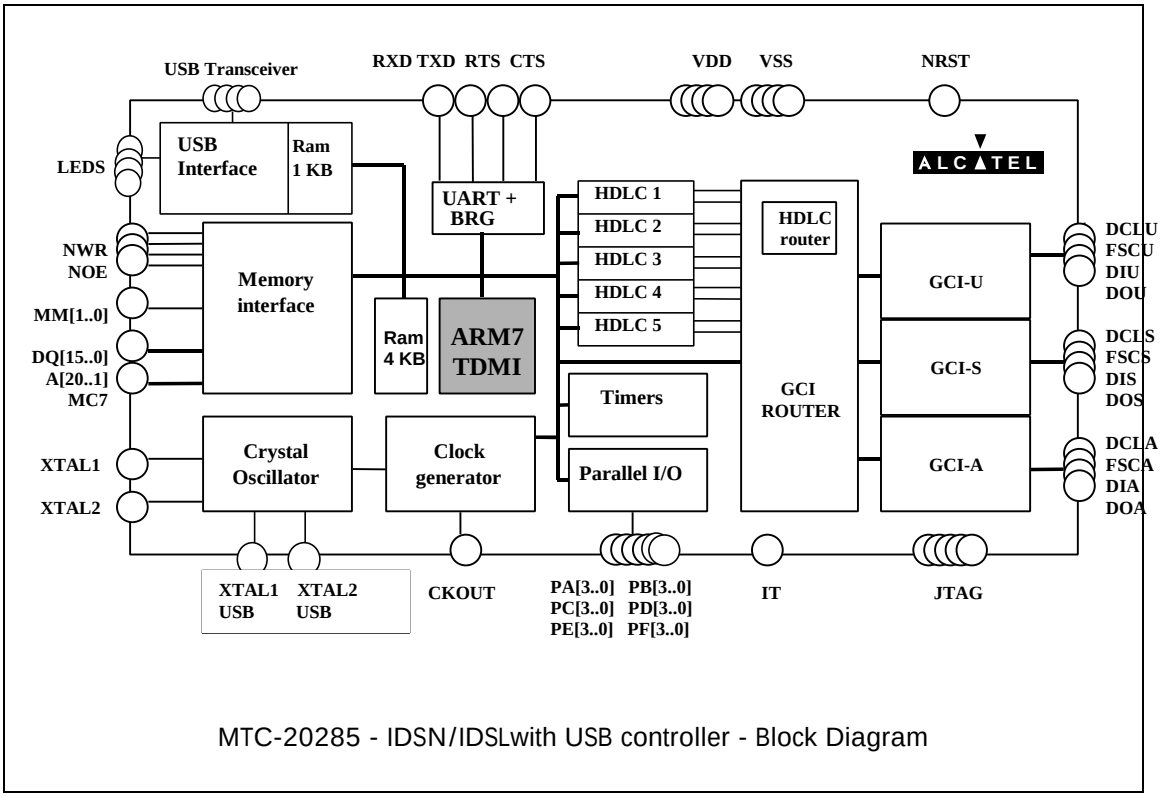
Key Applications:

- ISDN NT+ with high-speed USB data features
- USB-based ISDN TAs
- ISDN / IDSL routers / multiplexers
- ISDN PABX

The MTC-20285 is a fully integrated controller for ISDN/IDSL terminal equipment applications with advanced data communications features, offering integrated USB interfaces. It has been specifically designed for control and interface functions between a ISDN access devices, such as the MTC-20276/77 Integrated NT, and other terminal functions such as analog interfaces, e.g. by means of the MTK-40130 Short-Haul POTS chipset. It incorporates an ARM7TDMI RISC core, which can perform all of the terminal control and data flow management functions required in software. It can thus form the core of an Intelligent NT, or "NTplus" unit, as well as being the core of router/multiplexer equipment for data applications. In addition, the GCI port for analog peripherals supports the x8 multiplex mode, allowing up to 16 analog ports to be accessed. It can also form the core of a small ISDN based PABX. The register map is a functional superset of the MTC-20280 ISDN terminal controller, so is upwards software compatible. The on-board USB controller offers data connectivity to PCs for high-speed data applications, or for specialist products for CTI, dealer-desk or call-center applications.



ISDN/IDSL Terminal Controller - typical application



MTC-20285 - IDSN/IDSLwith USB controller - Block Diagram

General description

Clock generation and control

A master clock oscillator, based on an external crystal of 15.36Mhz, is provided. This provides an output at the crystal frequency for use by the ISDN chip (INTT or INTQ). It therefore offers better than 100ppm accuracy. The CPU clock frequency is SW selectable, allowing the power-consumption to be reduced at times when full processing speed is not required. An on-board DPLL doubles to clock frequency to allow the CPU and all peripherals to operate at higher clock speeds (The default condition emulates the timing of the MTC-20280 for software compatibility).

Memory bus

The external memory bus supports either 8-bit (for low cost) or 16 bit (high-speed) memory systems. It allows read/write access to off-chip memory and I/O resources, and includes a simple to use on-chip memory decoding scheme to minimize external logic. In mot cases, the external memory interfaces requires no glue-logic whatsoever. A maximum of 12 MBytes external memory can be accessed, in automatically decoded pages of 2 MBytes. It is designed to interface to standard FLASH EEPROM and (pseudo)static RAMs. The bus interface logic includes a programmable WAIT STATE generator, to allow access to slow external. 4 Kbytes of fast (0 wait-state with 32 bit access), on-chip static RAM is included.

A programmable Chip-Select (CS) decoder defines the external memory-map - the default map ensures that the CPU can start up from reset by enabling ROM at address. It provides for 6 external memory ranges to be individually decoded. With regard to EMC requirements, the slope of the memory bus transitions is controlled, in a manner consistent with achieving the required bus transfer speed. Each CS memory range has programmable wait-states.

3-way GCI interface

(Terminology. DOWNSTREAM 'refers to the transfer of data coming from the U interface towards the S or Analog interfaces. Upstream is the direction from the S or analog interfaces towards the U.)

The device provides for 3 fully independent CGI interfaces: normally allocated as follows:
1. U interface of MTC-20276/20277 INT, GCI-U
2. S interface of MTC-20276/20277 INT, GCI-S
3. Interface to analog devices such as MTK-40130 short-haul POTS chipset, GCI-A

In reality, all three GCI ports are identical - the allocation to U, S and A (analog) is arbitrary, for clarity only.

The U interface section of the INT will always provide the GCI clocks (master) when active. (This can be achieved by issuing the AWAKE command on the GCI C/I bits to the U interface, which activates the timing generator of the U interface without actually initiating transmission). All other GCI buses will generally be slaved to this one. In applications where the use of the U interface is not mandatory (e.g. in a micro-PABX system which allows internal calling without U activation), an internal GCI clock source can be selected. An integrated PLL system may be enabled to allow the internally generated GCI clocks to track and lock to the U GCI clock, should this become active in the course of operation.

All bytes of the GCI frames of all three GCI interfaces are accessible to the processor, read and write. A sophisticated router allows any of the GCI fields (B channel, D channel, C/I bits, Monitor channel) to be routed to the corresponding field of any destination channel (bytes can also be 'disabled', in which case they remain at the idle - logic '1'- state). Particularly powerful is the ability to set fixed routes of the B channels from a source to any destination without the need for further intervention by the CPU, thus relieving the CPU of much real-time processing. Up to 8 GCI time-slots is supported on each GCI port independently, where external GCI clocks are available. The internal GCI clock supports 1 timeslot or 8 timeslots. The clock source (which determines the number of timeslots supported by the channel) is independently selectable for each GCI port. Using an external clock thus allows the GCI ports to interface to all commonly used ISDN devices.

With regard to EMC requirements, the slope of the GCI data output pins is controlled, in a manner consistent with achieving the required bus transfer speed.

HDLC controllers

The 5 integrated HDLC controllers can be routed two / from any B or D channel of any port. In addition, they each have full-duplex 64 byte FIFOs, which allow a large timing latency and thus easy software timing constraints. The HDLC controller protocol may be disabled under software control, thus allowing the FIFOs to be used to buffer real-time data, e.g. for the processing of voice-band signals on B-channels (DTMF decoding, modem emulation, pre-recorded voice announcements etc...). In this mode, the data order (MSB first or LSB first) may be user-selected for compatibility with various applications (for example - using the FIFOs to buffer PCM data from an analog GCI terminal requires bit-reversal).

Generally, HDLC1 will be used to manage the ISDN D-channel. D-channel conflicts between the S bus and the HDLC1 controller of the device are handled by forcing a D-channel busy condition on the S-bus by means of the appropriate command to the S interface of the INT, via the appropriate M-channel commands. This is done only after the microprocessor has verified that the BUSY bit in the SIC's control registers is clear (i.e. D-channel not in use).

HDLC controllers 2 and 3 are generally used to handle packetized data transport over the B channels (including balanced applications such as LAPB). However, in specific applications such as internal call transfer support or PABX, the D-channel to/from the S-bus requires independent management (while still monitoring the D channel to/from the U interface). HDLC 2 to 5 may be used for this purpose. Additional HDLC controllers can be used to buffer speech information, as required.

DTMF decoding

Low-cost, external analog DTMF decoder circuits can be used to perform this function. These can be connected to the CPU via an on-chip 8-bit parallel I/O port (programmable bit directions). Alternatively, software algorithms on the ARM7TDMI processor may be used. The 0-wait-state on-chip RAM facilitates this.

Serial I/O

A UART with selectable baud-rate and full-duplex 64-byte buffering is provided. The baud-rate is programmable to standard rates up to 230.4 kbps. The external UART interface pins are 5V compatible. A second, simplified UART without buffering is also provided, intended for product configuration or diagnostics.

Parallel I/O ports

A number of parallel I/O port are provided, totaling 24 bits when in 16-bit memory bus mode (an additional 8 I/O pins are available when the 8-bit bus mode is used). These ports are primarily to allow an interface to external DTMF decoder chips and other application-dependent hardware. The ports are addressable by the CPU as a latched output, an unlatched input, and a data-direction register which is used to select the direction (input at reset) of each bit. External port pins may also request an interrupt to the CPU (maskable) when selected as an input.

Interrupt Control

The device contains several interrupt sources. Each can be masked by setting a bit in a control register. Priority is resolved in software; all Interrupt request 'bits from the various sources are readable in a register. This register can be written to; writing a 1 clears the corresponding request bit, but writing a 0 has no effect. Individual interrupt control registers also exist within each of the functional blocks (HDLC controller, UART etc... .). The registers described here provide a centralized and thus fast means of handling priorities. The various interrupt sources are permanently routed to the nIRQ (normal interrupts) and to the FIRQ (fast response) of the AMR7 CPU.

An external interrupt request pin allows external peripheral devices to communicate asynchronously with the CPU. In addition, most of the available parallel I/O pins can function as interrupt sources when programmed as inputs.

Timers / Watchdog

2, 16 bit timer/counters and a (7 second maximum) Watchdog timer are included. The timers support auto-pre-load timer interrupt generation, thus allowing interrupts to be generated at regular, programmable intervals. Timer 2 also support timer-capture functions (the source of which is selectable), to allow the timing of external events to be simplified. The watchdog output can be connect to provide either system reset (normal use) or routed to an interrupt pin for system debug.

CPU

The ARM7TDMI CPU is integrated, and will generally use the 16-bit data bus mode 'Thumb '. The external bus interface supports 16- or 32-bit transfers multiplexed to 16- or 8 bits, while access to the on-chip SRAM can take place as 8, 16 or 32 bit transfers (it thus supports the full performance of the ARM7 CPU). The CPU will generally run at the clock frequency set by the crystal oscillator (15.36 Mhz) multiplied by 2 (31 MHz). However, a programmable divider is provided to allow software control of the processor speed, and therefore the power consumption.

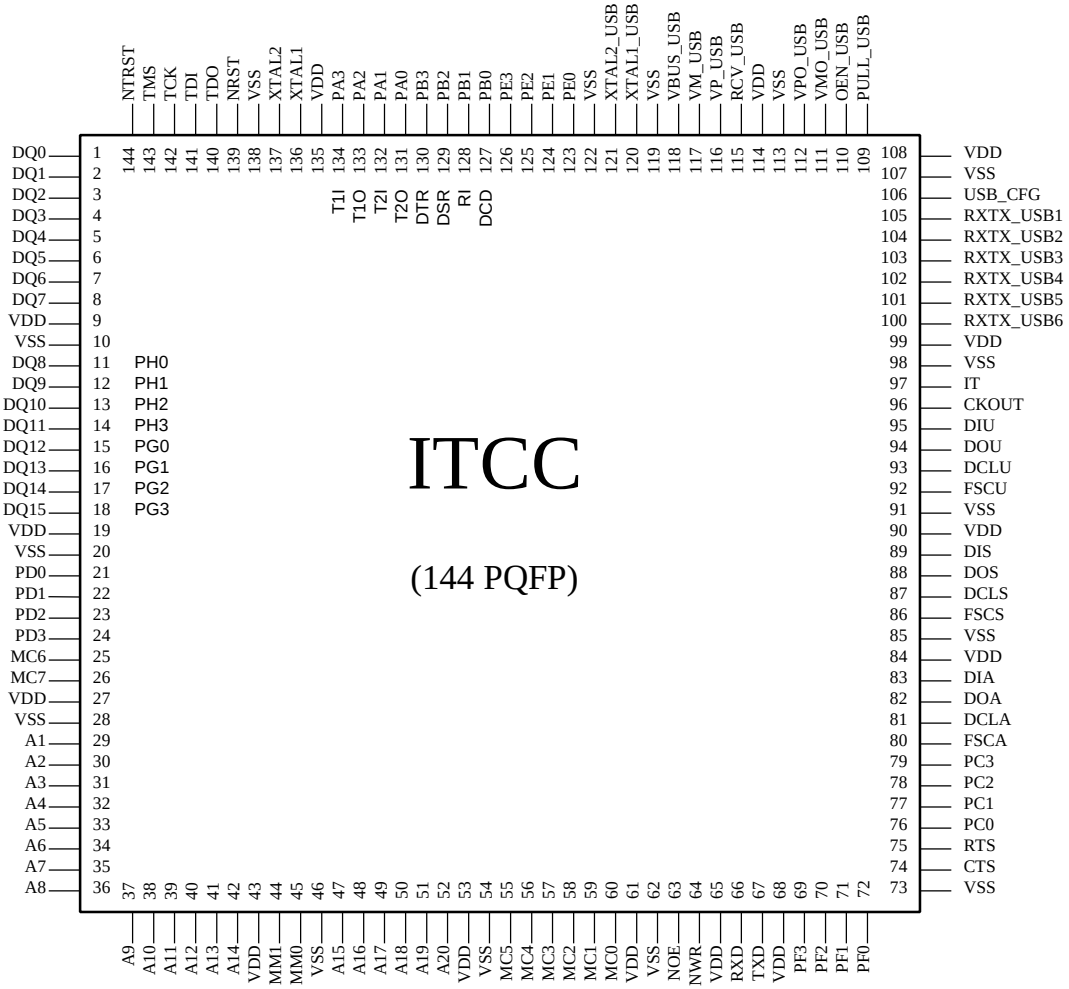
USB controller

The on-board Revision 1.1 compliant USB controller supports up to 12 end-points (6 bi-directional endpoints). In addition to memory-mapped control registers, a dual-port RAM implementation of user-definable FIFOs for each endpoint ensures that USB data transfers do not interfere with CPU activity, with resulting loss of CPU throughput. Full support of USB Plug&Play features is offered, and the execution of all standard USB commands is automatic (does not require CPU intervention). The USB controller block remains in a reset state until the user software has properly initialized the block. The USB controller communicates to an off-chip physical USB driver/receiver device via an interface as defined by the USB

Implementers Forum, and is thus compatible with industry-standard devices (the use of an off-chip physical device facilitates system design for EMC and the stringent isolation requirements of the telecommunications industry). 7 status indication outputs are provided, which can be used to drive indictor LEDs showing USB status and activity on each end-point pair.

Pinning information

A 144 pin PQFP package is used.



Electrical Characteristics.

Abs Max Ratings

Storage Temperature	-50 to + 150 °C
Temperature under bias	-50 to + 125 °C
Vdd	6V
Voltage on any pin	Vss-0.3V to Vdd+0,3V (except 5V compatible I/O's)

Operating Conditions

Operating temperature	0 to +70 (-40 to +85 option) °C
Vdd	2.7 to 3.6V
Pdd	<100 mW (average)
Pdd fallback	20mW (GCI through-routed)
Clock frequency	15.36 MHz