

February 1994

Features

- NCO and CMAC on One Chip
- 15MHz, 25.6MHz, 33MHz Versions
- 32-Bit Frequency Control
- 16-Bit Phase Modulation
- 16-Bit CMAC
- 0.008Hz Tuning Resolution at 33MHz
- Spurious Frequency Components < -90dBc
- Fully Static CMOS

Applications

- Frequency Synthesis
- Modulation - AM, FM, PSK, FSK, QAM
- Demodulation, PLL
- Phase Shifter
- Polar to Cartesian Conversions

Description

The Harris HSP45116 combines a high performance quadrature numerically controlled oscillator (NCO) and a high speed 16-bit Complex Multiplier/Accumulator (CMAC) on a single IC. This combination of functions allows a complex vector to be multiplied by the internally generated (cos, sin) vector for quadrature modulation and demodulation. As shown in the block diagram, the HSP45116 is divided into three main sections. The Phase/Frequency Control Section (PFCS) and the Sine/Cosine Section together form a complex NCO. The CMAC multiplies the output of the Sine/Cosine Section with an external complex vector.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The phase resolution of the PFCS is 32-bits, which results in frequency resolution better than 0.008Hz at 33MHz. The output of the PFCS is the argument of the sine and cosine. The spurious free dynamic range of the complex sinusoid is greater than 90dBc.

The output vector from the Sine/Cosine Section is one of the inputs to the Complex Multiplier/Accumulator. The CMAC multiplies this (cos, sin) vector by an external complex vector and can accumulate the result. The resulting complex vectors are available through two 20-bit output ports which maintain the 90dB spectral purity. This result can be accumulated internally to implement an accumulate and dump filter.

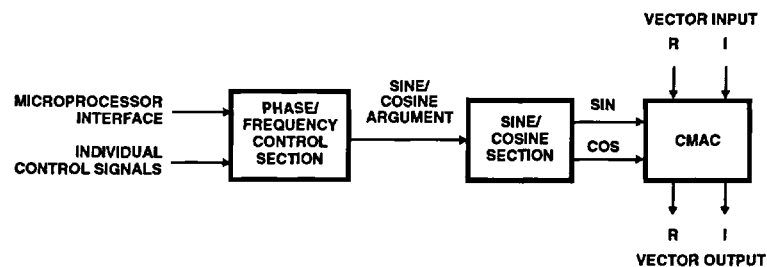
A quadrature down converter can be implemented by loading a center frequency into the Phase/Frequency Control Section. The signal to be downconverted is the Vector Input of the CMAC, which multiplies the data by the rotating vector from the Sine/Cosine Section. The resulting complex output is the down converted signal.

The pinout for the TAB package can be obtained by referring to the Metallization Mask Layout of the HSP45116/883 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45116VC-15	0°C to +70°C	160 Lead MQFP
HSP45116VC-25	0°C to +70°C	160 Lead MQFP
HSP45116VC-33	0°C to +70°C	160 Lead MQFP
HSP45116GC-15	0°C to +70°C	145 Lead PGA
HSP45116GC-25	0°C to +70°C	145 Lead PGA
HSP45116GC-33	0°C to +70°C	145 Lead PGA
HSP45116TM-15	-55°C to +125°C	156 Lead TAB
HSP45116TM-25	-55°C to +125°C	156 Lead TAB
HSP45116AVC-52	0°C to +70°C	160 Lead MQFP

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.
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File Number 2485.4

Pinouts

145 PIN PGA
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	VCC	IMIN 4	IMIN 6	IMIN 9	IMIN 11	IMIN 15	IMIN 16	GND	VCC	IO 18	IO 15	IO 12	IO 10	GND	VCC	A
B	GND	IMIN 1	IMIN 5	IMIN 7	IMIN 10	IMIN 13	IMIN 14	IO 19	IO 16	IO 14	IO 11	IO 8	IO 7	IO 5	IO 2	B
C	RIN 15	RIN 18	IMIN 2	IMIN 3	IMIN 8	IMIN 12	IMIN 17	IMIN 18	IO 17	IO 13	IO 9	IO 6	IO 4	IO 1	RO 18	C
D	RIN 13	RIN 17	IMIN 0	INDEX									IO 3	RO 19	RO 17	D
E	RIN 10	RIN 14	RIN 16										IO 0	RO 16	RO 15	E
F	RIN 7	RIN 11	RIN 12										RO 14	RO 13	RO 11	F
G	VCC	RIN 9	RIN 8										RO 9	RO 12	RO 10	G
H	GND	RIN 6	RIN 5										RO 8	RO 7	GND	H
J	RIN 3	RIN 1	RIN 4										RO 5	RO 4	VCC	J
K	RIN 2	RIN 0	SH 1										RO 1	RO 2	RO 8	K
L	SH 0	ACC	RBYTLD										PACO	DET	RO 3	L
M	ENPH REG	PEAK	MOD										OEREXT	OEI	RO 0	M
N	ENPH REG	ENPH REG	MOD	LOAD	ENPH REG	MOD	AD	C	C	C	C	OUT - MIX	OUT - MIX	OEREXT	DET	N
P	TICO	PACI	PMSBL	CLROPH	ENTHREG	CS	AD	C	C	C	C	C	C	OER	GND	P
Q	VCC	GND	ENPHAC	ENI	CLK	WR	VCC	GND	C	C	C	C	C	C	VCC	Q
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

BOTTOM VIEW

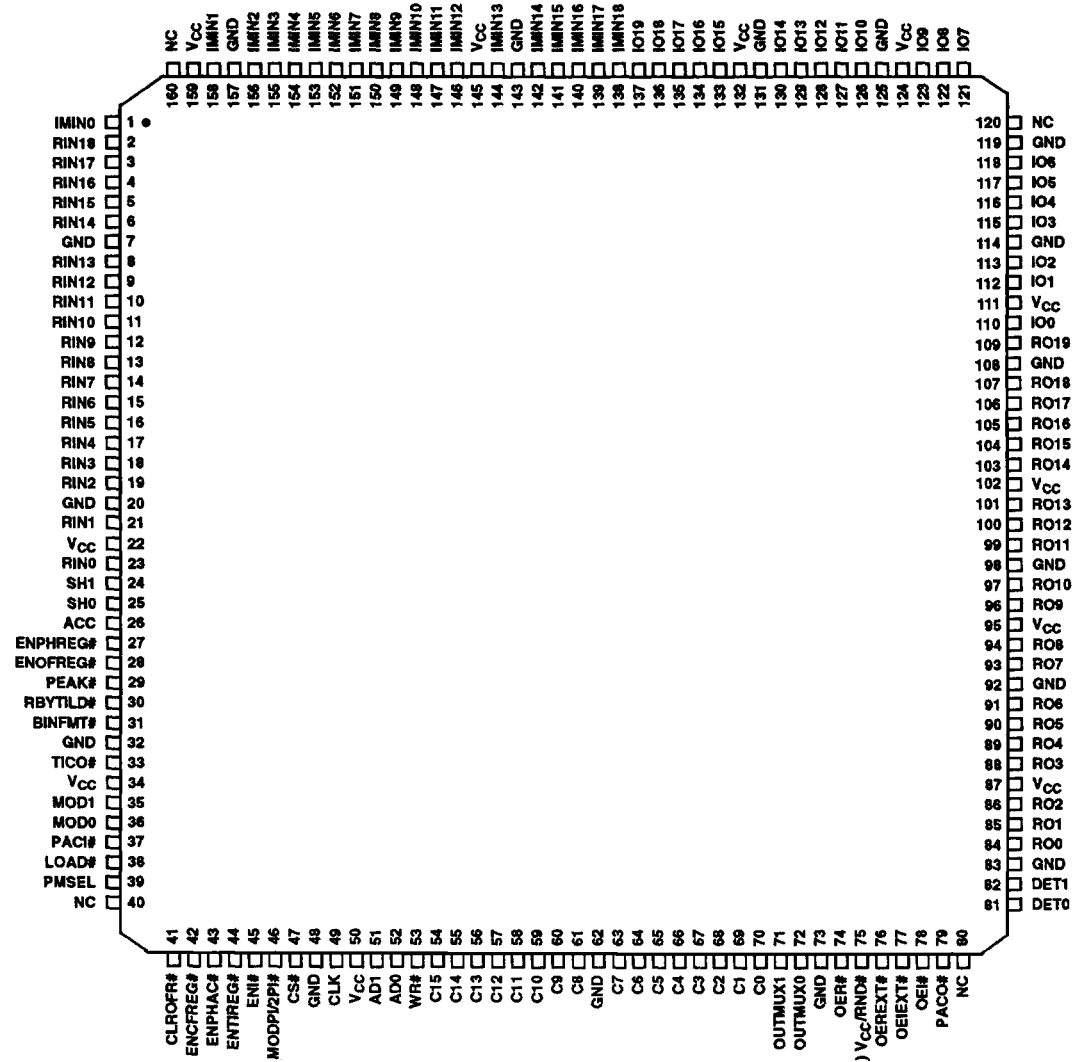
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	VCC	GND	IO 10	IO 12	IO 15	IO 18	VCC	GND	IMIN 18	IMIN 15	IMIN 11	IMIN 9	IMIN 8	IMIN 4	VCC	A
B	IO 2	IO 5	IO 7	IO 8	IO 11	IO 14	IO 16	IO 19	IMIN 14	IMIN 13	IMIN 10	IMIN 7	IMIN 5	IMIN 1	GND	B
C	RO 18	IO 1	IO 4	IO 6	IO 9	IO 13	IO 17	IMIN 18	IMIN 17	IMIN 12	IMIN 6	IMIN 3	IMIN 2	RIN 18	RIN 15	C
D	RO 17	RO 19	IO 3									INDEX	IMIN 0	RIN 17	RIN 13	D
E	RO 15	RO 18	IO 0										RIN 16	RIN 14	RIN 10	E
F	RO 11	RO 13	RO 14										RIN 12	RIN 11	RIN 7	F
G	RO 10	RO 12	RO 9										RIN 8	RIN 9	VCC	G
H	GND	RO 7	RO 8										RIN 5	RIN 6	GND	H
J	VCC	RO 4	RO 5										RIN 4	RIN 1	RIN 3	J
K	RO 6	RO 2	RO 1										SH 1	RIN 0	RIN 2	K
L	RO 3	DET	PACO										RBYTLD	ACC	SH 0	L
M	RO 0	OEI	OEREXT										MOD	PEAK	ENPH REG	M
N	DET	OEREXT	OUTMIX	OUTMIX	C	C	C	C	AD	MOD	ENPH REG	LOAD	MOD	ENPH REG	ENPH REG	N
P	GND	OER	C	C	C	C	C	C	AD	CS	ENTHREG	CLROPH	PMSBL	PACI	TICO	P
Q	VCC	C	C	C	C	C	C	GND	VCC	WR	CLK	ENI	ENPHAC	GND	VCC	Q
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

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SIGNAL SYNTHESIZERS

HSP45116

Pinouts (Continued)

160 LEAD MQFP
TOP VIEW



(SEE NOTE 1) V_{CC}/RND#

NOTE:

- Pin 75 functions as the round enable (RND#) on the HSP45116A. Pin 75 is V_{CC} on the HSP45116.

Pin Description

NAME	NUMBER	TYPE	DESCRIPTION
VCC	A1, A9, A15, G1, J15, Q1, Q7, Q15		+5 Power supply input
GND	A8, A14, B1, H1, H15, P15, Q2, Q8		Power supply ground input
C0-15	N8-11, P8-13, Q9-14	I	Control input bus for loading phase and frequency data into the PFCS. C15 is the MSB.
ADO-1	N7, P7	I	Address pins for selecting destination of C0-15 data
CS#	P6	I	Chip select (Active Low)
WR#	Q6	I	Write enable. Data is clocked into the register selected by ADO-1 on the rising edge of WR# when the CS# line is low.
CLK	Q5	I	Clock. All registers, except the control registers clocked with WR#, are clocked (when enabled) by the rising edge of CLK.
ENPHREG#	M1	I	Phase register enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENPHREG# enables the clocking of data into the phase register.
ENOFREG#	N1	I	Frequency offset register enable. (Active Low) Registered on chip by CLK. When active, after being clocked onto chip, ENOFREG# enables clocking of data into the frequency offset register.
ENCFREG#	N5	I	Center frequency register enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENCFREG# enables clocking of data into the center frequency register.
ENPHAC#	Q3	I	Phase accumulator register enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENPHAC# enables clocking of the phase accumulator register.
ENTIREG#	P5	I	Time interval control register enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENTIREG# enables clocking of data into the time accumulator register.
ENI#	Q4	I	Real and imaginary data input register (RIR, IIR) enable. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, ENI# enables clocking of data into the real and imaginary input data register.
MODPI/ 2PI#	N6	I	Modulo $\pi/2\pi$ select. When low, the Sine and Cosine ROMs are addressed modulo 2π (360 degrees). When high, the most significant address bit is held low so that the ROMs are addressed modulo π (180 degrees). This input is registered on chip by clock.
CLROFR#	P4	I	Frequency offset register output zero. (Active low) Registered on chip by CLK. When active, after being clocked onto chip, CLROFR# zeros the data path from the frequency offset register to the frequency adder. New data can still be clocked into the frequency offset register; CLROFR# does not affect the contents of the register.
LOAD#	N4	I	Phase accumulator load control. (Active low) Registered on chip by CLK. Zeroes feedback path in the phase accumulator without clearing the phase accumulator register.
MOD0-1	M3, N3	I	External modulation control bits. When selected with the PMSEL line, these bits add a 0, 90, 180, or 270 degree offset to the current phase in the phase accumulator. The lower 14 bits of the phase control path are set to zero. These bits are loaded into the phase register when ENPHREG# is low.
PMSEL	P3	I	Phase modulation select line. This line determines the source of the data clocked into the phase register. When high, the phase control register is selected. When low, the external modulation pins (MOD0-1) are selected for the most significant two bits and the least significant two bits and the least significant 14 bits are set to zero. This control is registered by CLK.
RBYTILD#	L3	I	ROM bypass, timer load. Active low, Registered by CLK. This input bypasses the sine/cosine ROM so that the 16 bit phase adder output and lower 16 bits of the phase accumulator go directly to the CMAC's sine and cosine inputs, respectively. It also enables loading of the timer accumulator register by zeroing the feedback in the accumulator.

Pin Description (Continued)

NAME	NUMBER	TYPE	DESCRIPTION
PACI#	P2	I	Phase accumulator carry input. (Active low) A low on this pin causes the phase accumulator to increment by one in addition to the values in the phase accumulator register and frequency adder.
PACO#	L13	O	Phase accumulator carry output. Active low and registered by CLK. A low on this output indicates that the phase accumulator has overflowed, i.e., the end of one sine/cosine cycle has been reached.
TICO#	P1	O	Time interval accumulator carry output. Active low, registered by CLK. This output goes low when a carry is generated by the time interval accumulator. This function is provided to time out control events such as synchronizing register clocking to data timing.
RINO-18	C1, C2, D1, D2, E1-3, F1-3, G2, G3, H2, H3, J1-3, K1, K2	I	Real input data bus. This is the external real component into the complex multiplier. The bus is clocked into the real input data register by CLK when ENI# is asserted. Two's complement.
IMINO-18	A2-7, B2-7, C3-8, D3	I	Imaginary input data bus. This is the external imaginary component into the complex multiplier. The bus is clocked into the real input data register by CLK when ENI# is asserted. Two's complement.
SHO-1	K3, L1	I	Shift control inputs. These lines control the input shifters of the RIN and IIN inputs of the complex multiplier. The shift controls are common to the shifters on both of the busses.
ACC	L2	I	Accumulate/dump control. This input controls the complex accumulators and their holding registers. When high, the accumulators accumulate and the holding registers are disabled. When low, the feedback in the accumulators is zeroed to cause the accumulators to load. The holding registers are enabled to clock in the results of the accumulation. This input is registered by CLK.
BINFMT#	N2	I	This input is used to convert the two's complement output to offset binary (unsigned) for applications using D/A converters. When low, bits RO19 and IO19 are inverted from the internal two's complement representation. This input is registered by CLK.
PEAK#	M2	I	This input enables the peak detect feature of the block floating point detector. When high, the maximum bit growth in the output holding registers is encoded and output on the DETO-1 pins. When the PEAK# input is asserted, the block floating point detector output will track the maximum growth in the holding registers, including the data in the holding registers at the time that PEAK# is activated.
OUTMUX0-1	N12, N13	I	These inputs select the data to be output on RO0-19 and IO0-19.
RO0-19	C15, D14, D15, E14, E15, F13-15, G13-15, H13, H14, J13, J14, K13-15, L15, M15	O	Real output data bus. These three state outputs are controlled by OER# and OEREXT#. OUTMUX0-1 select the data output on the bus.
IO0-19	A10-13, B8-15, C9-14, D13, E13	O	Imaginary output data bus. These three state outputs are controlled by OEI# and OEIEXT#. OUTMUX0-1 select the data output on the bus.
DETO-1	N15, L14	O	These output pins indicate the number of bits of growth in the accumulators. While PEAK# is low, these pins indicate the peak growth. The detector examines bits 15-18, real and imaginary accumulator holding registers and bits 30-33 of the real and imaginary CMAC holding registers. The bits indicate the largest growth of the four registers.
OER#	P14	I	Three state control for bits RO0-15. Outputs are enabled when the line is low.
OEREXT#	M13	I	Three state control for bits RO16-19. Outputs are enabled when the line is low.
OEI#	M14	I	Three state control for bits IO0-15. Outputs are enabled when the line is low.
OEIEXT#	N14	I	Three state control for bits IO16-19. Outputs are enabled when the line is low.
RND#	N/A	I	Round Enable (Available on HSP45116A only). This input enables rounding of the output data precision from 9 to 20 bits (see HSP45116A Description and Operation). This input is active "low". This input must be tied either high or low.

Functional Description

The Numerically Controlled Oscillator/Modulator (NCOM) produces a digital complex sinusoid waveform whose amplitude, phase and frequency are controlled by a set of input command words. When used as a Numerically Controlled Oscillator (NCO), it generates 16 bit sine and cosine vectors at a maximum sample rate of 33MHz. The NCOM can be preprogrammed to produce a constant (CW) sine and cosine output for Direct Digital Synthesis (DDS) applications. Alternatively, the phase and frequency inputs can be updated in real time to produce a FM, PSK, FSK, or MSK modulated waveform. The Complex Multiplier/Accumulator (CMAC) can be used to multiply this waveform by an input signal for AM and QAM signals. By stepping the phase input, the output of the ROM becomes an FFT twiddle factor; when data is input to the Vector Inputs (see Block Diagram), the NCOM calculates an FFT butterfly.

As shown in the Block Diagram, the NCOM consists of three parts: Phase and Frequency Control Section (PFCS), Sine/Cosine Generator, and CMAC. The PFCS stores the phase and frequency inputs and uses them to calculate the phase angle of a rotating complex vector. The Sine/Cosine Generator performs a lookup on this phase and outputs the appropriate values for the sine and cosine. The sine and cosine form one set of inputs to the CMAC, which multiplies them by the input vector to form the modulated output.

Phase and Frequency Control Section

The phase and frequency of the internally generated sine and cosine are controlled by the PFCS (Figure 1). The PFCS generates a 32 bit word that represents the current phase of the sine and cosine waves being generated: the Sine/Cosine Argument. Stepping this phase angle from 0 through full scale ($2^{32} - 1$) corresponds to the phase angle of a sinusoid starting at 0° and advancing around the unit circle counterclockwise. The PFCS automatically increments the phase by a preprogrammed amount on every rising edge of the external clock. The value of the phase step (which is the sum of the Center and Offset Frequency Registers) is:

$$\text{Phase Step} = \frac{\text{Signal Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

The PFCS is divided into 2 sections: the Phase Accumulator uses the data on C0-15 to compute the phase angle that is the input to the Sine/Cosine Section (Sine/Cosine Argument); the Time Accumulator supplies a pulse to mark the passage of a preprogrammed period of time.

The Phase Accumulator and Time Accumulator work on the same principle: a 32 bit word is added to the contents of a 32 bit accumulator register every clock cycle; when the sum

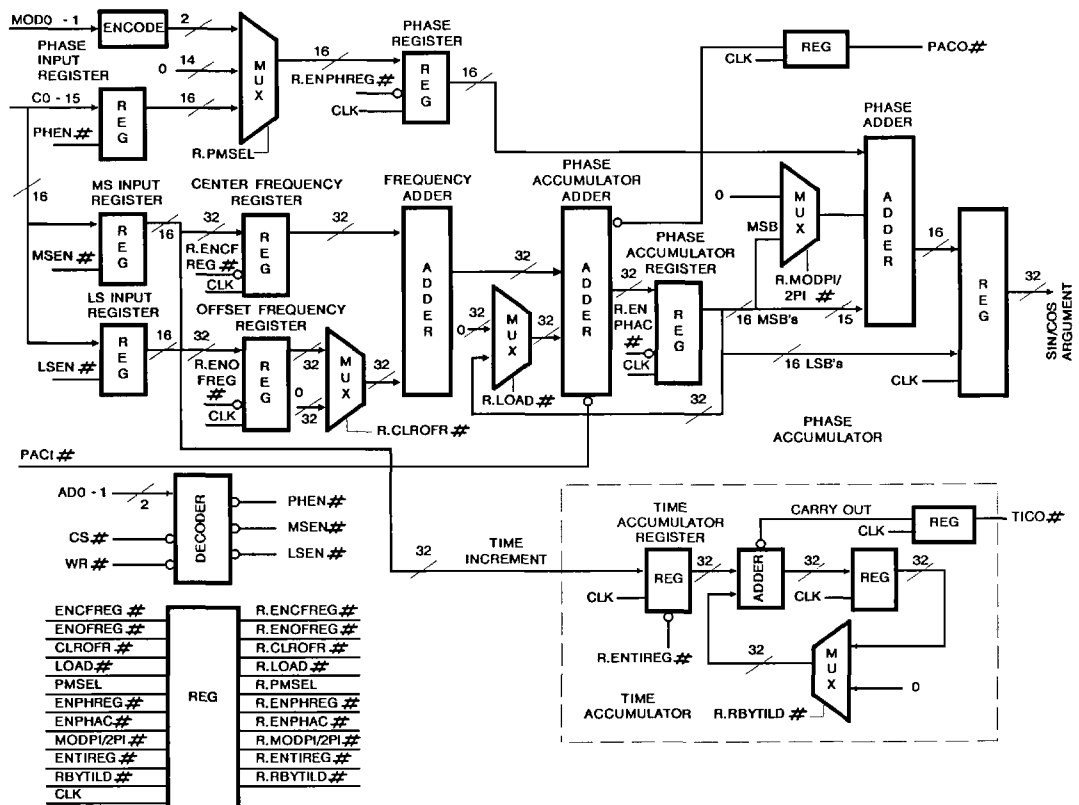


FIGURE 1. PHASE/FREQUENCY CONTROL SECTION BLOCK DIAGRAM

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SIGNAL SYNTHESIZERS

causes the adder to overflow, the accumulation continues with the 32 bits of the adder going into the accumulator register. The overflow bit is used as an output to indicate the timing of the accumulation overflows. In the Time Accumulator, the overflow bit generates TICO#, the Time Accumulator carry out (which is the only output of the Time Accumulator). In the Phase Accumulator, the overflow is inverted to generate the Phase Accumulator Carry Out, PACO#.

The output of the Phase Accumulator goes to the Phase Adder, which adds an offset to the top 16 bits of the phase. This 32 bit number forms the argument of the sine and cosine, which is passed to the Sine/Cosine Generator.

Both accumulators are loaded 16 bits at a time over the C0-15 bus. Data on C0-15 is loaded into one of the three input registers when CS# and WR# are low. The data in the Most Significant Input Register and Least Significant Input Register forms a 32 bit word that is the input to the Center Frequency Register, Offset Frequency Register and Time Accumulator. These registers are loaded by enabling the proper register enable signal; for example, to load the Center Frequency Register, the data is loaded into the LS and MS Input Registers, and ENCFREG# is set to zero; the next rising edge of CLK will pass the registered version of ENCFREG#, R.ENCFREG#, to the clock enable of the Center Frequency Register; this register then gets loaded on the following rising edge of CLK. The contents of the Input Registers will be continuously loaded into the Center Frequency Register as long as R.ENCFREG# is low.

The Phase Register is loaded in a similar manner. Assuming PMSEL is high, the contents of the Phase Input Register is loaded into the Phase Register on every rising clock edge that R.ENPHREG is low. If PMSEL is low, MOD0-1 supply the two most significant bits into the Phase Register (MOD1 is the MSB) and the least significant 14 bits are loaded with 0. MOD0-1 are used to generate a Quad Phase Shift Keying (QPSK) signal (Table 2).

TABLE 1. ADO-1 DECODING

AD1	AD0	CS#	WR#	FUNCTION
0	0	0	↑	Load least significant bits of frequency input
0	1	0	↑	Load most significant bits of frequency input
1	0	0	↑	Load phase register
1	1	X	X	Reserved
X	X	1	X	Reserved

The Phase Accumulator consists of registers and adders that compute the value of the current phase at every clock. It has three inputs: Center Frequency, which corresponds to the carrier frequency of a signal; Offset Frequency, which is the deviation from the Center Frequency; and Phase, which is a 16 bit number that is added to the current phase for

PSK modulation schemes. These three values are used by the Phase Accumulator and Phase Adder to form the phase of the internally generated sine and cosine.

The sum of the values in Center and Offset Frequency Registers corresponds to the desired phase increment (modulo 2^{32}) from one clock to the next. For example, loading both registers with zero will cause the Phase Accumulator to add zero to its current output; the output of the PFCS will remain at its current value; i.e., the output of the NCOM will be a DC signal. If a hexadecimal 00000001 is loaded into the Center Frequency Control Register, the output of the PFCS will increment by one after every clock. This will step through every location in the Sine/Cosine Generator, so that the output will be the lowest frequency above DC that can be generated by the NCOM, i.e., the clock frequency divided by 2^{32} . If the input to the Center Frequency Control Register is hex 80000000, the PFCS will step through the Generator with half of the maximum step size, so that frequency of the output waveform will be half of the sample rate.

The operation of the Offset Frequency Control Register is identical to that of the Center Frequency Control Register; having two separate registers allows the user to generate an FM signal by loading the carrier frequency in the Center Frequency Control Register and updating the Offset Frequency Control Register with the value of the frequency offset - the difference between the carrier frequency and the frequency of the output signal. A logic low on CLROFR# disables the output of the Offset Frequency Register without clearing the contents of the register.

TABLE 2. MOD0-1 DECODE

MOD1	MOD0	PHASE SHIFT (DEGREES)
0	0	0
0	1	90
1	0	270
1	1	180

Initializing the Phase Accumulator Register is done by putting a low on the LOAD# line. This zeroes the feedback path to the accumulator, so that the register is loaded with the current value of the phase increment summer on the next clock.

The final phase value going to the Generator can be adjusted using MODPI/2PI# to force the range of the phase to be 0° to 180° (modulo π) or 0° to 360° (modulo 2π). Modulo 2π is the mode used for modulation, demodulation, direct digital synthesis, etc. Modulo π is used to calculate FFTs. This is explained in greater detail in the Applications section.

The Phase Register adds an offset to the output of the Phase Accumulator. Since the Phase Register is only 16 bits, it is added to the top 16 bits of the Phase Accumulator.

The Time Accumulator consists of a register which is incremented on every clock. The amount by which it increments is loaded into the Input Registers and is latched into the Time Accumulator Register on rising edges of CLK while ENTIREG# is low. The output of the Time Accumulator is the accumulator carry out, TICO#. TICO# can be used as a timer to enable the periodic sampling of the output of the NCOM. The number programmed into this register equals $2^{32} \times \text{CLK period/desired time interval}$. TICO# is disabled and its phase is initialized by zeroing the feedback path of the accumulator with RBYTILD#.

Sine/Cosine Section

The Sine/Cosine Section (Figure 2) converts the output of the PFCS into the appropriate values for the sine and cosine. It takes the most significant 20 bits of the PFCS output and passes them through a look up table to form the 16 bit sine and cosine inputs to the CMAC.

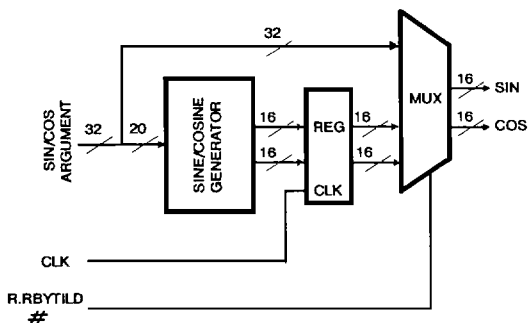


FIGURE 2. SINE/COSINE SECTION

The 20 bit word maps into 2π radians so that the angular resolution is $2\pi/2^{20}$. An address of zero corresponds to 0 radians and an address of hex FFFF corresponds to 2π ($2\pi/2^{20}$) radians. The outputs of the Generator section are 2's complement sine and cosine values. The sine and cosine outputs range from hexadecimal 8001, which represents negative full scale, to 7FFF, which represents positive full scale. Note that the normal range for two's complement numbers is 8000 to 7FFF; the output range of the SIN/COS generator is scaled by one so that it is symmetric about 0.

The sine and cosine values are computed to reduce the amount of ROM needed. The magnitude of the error in the computed value of the complex vector is less than -90.2dB. The error in the sine or cosine alone is approximately 2dB better.

If RBYTILD# is low, the output of the PFCS goes directly to the inputs of the CMAC. If the real and imaginary inputs of the CMAC are programmed to hex 7FFF and 0 respectively, then the output of the PFCS will appear on output bits 0 through 15 of the NCOM with the output multiplexers set to bring out the most significant bits of the CMAC output (OUTMUX = 00). The most significant 16 bits out of the PFCS appears on IOUT0-15 and the least significant bits come out on ROUT0-15.

Complex Multiplier/Accumulator

The CMAC (Figure 3) performs two types of functions: complex multiplication/accumulation for modulation and demodulation of digital signals, and the operations necessary to implement an FFT butterfly. Modulation and demodulation are implemented using the complex multiplier and its associated accumulator; the rest of the circuitry in this section, i.e., the complex accumulator, input shifters and growth detect logic are used along with the complex multiplier/accumulator for FFTs. The complex multiplier performs the complex vector multiplication on the output of the Sine/Cosine Section and the vector represented by the real and imaginary inputs RIN and IIN. The two vectors are combined in the following manner:

$$\text{ROUT} = \text{COS} \times \text{RIN} - \text{SIN} \times \text{IIN}$$

$$\text{IOUT} = \text{COS} \times \text{IIN} + \text{SIN} \times \text{RIN}$$

RIN and IIN are latched into the input registers and passed through the shift stages. Clocking of the input registers is enabled with a low on ENI#. The amount of shift on the latched data is programmed with SH0-1 (Table 3). The output of the shifters is sent to the CMAC and the auxiliary accumulators.

TABLE 3. INPUT SHIFT SELECTION

SH1	SH0	SELECTED BITS
0	0	RIN0-15, IMIN0-15
0	1	RIN1-16, IMIN1-16
1	0	RIN2-17, IMIN2-17
1	1	RIN3-18, IMIN3-18

The 33 bit real and imaginary outputs of the Complex Multiplier are latched in the Multiplier Registers and then go through the accumulator section of the CMAC. If the ACC line is high, the feedback to the accumulators is enabled; a low on ACC zeroes the feedback path, so that the next set of real and imaginary data out of the complex multiplier is stored in the CMAC Output Registers.

The data in the CMAC Output Registers goes to the Multiplexer, the output of which is determined by the OUTMUX0-1 lines (Table 4). BINFMT# controls whether the output of the Multiplexer is presented in two's complement or unsigned format; BINFMT# = 0 inverts ROUT19 and IOUT19 for unsigned output, while BINFMT# = 1 selects two's complement.

TABLE 4. OUTPUT MULTIPLEXER SELECTION

OUT MUX 1	OUT MUX 0	RO16-19	RO0-15	IO16-19	IO0-15
0	0	Real CMAC 31-34	Real CMAC 15-30	Imag CMAC 31-34	Imag CMAC 15-30
0	1	Real CMAC 31-34	0, Real CMAC 0-14	Imag CMAC 31-34	0, Imag CMAC 0-14
1	0	Real Acc 16-19	Real Acc 0-15	Imag Acc 16-19	Imag Acc 0-15
1	1	Reserved	Reserved	Reserved	Reserved

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SIGNAL SYNTHESIZERS

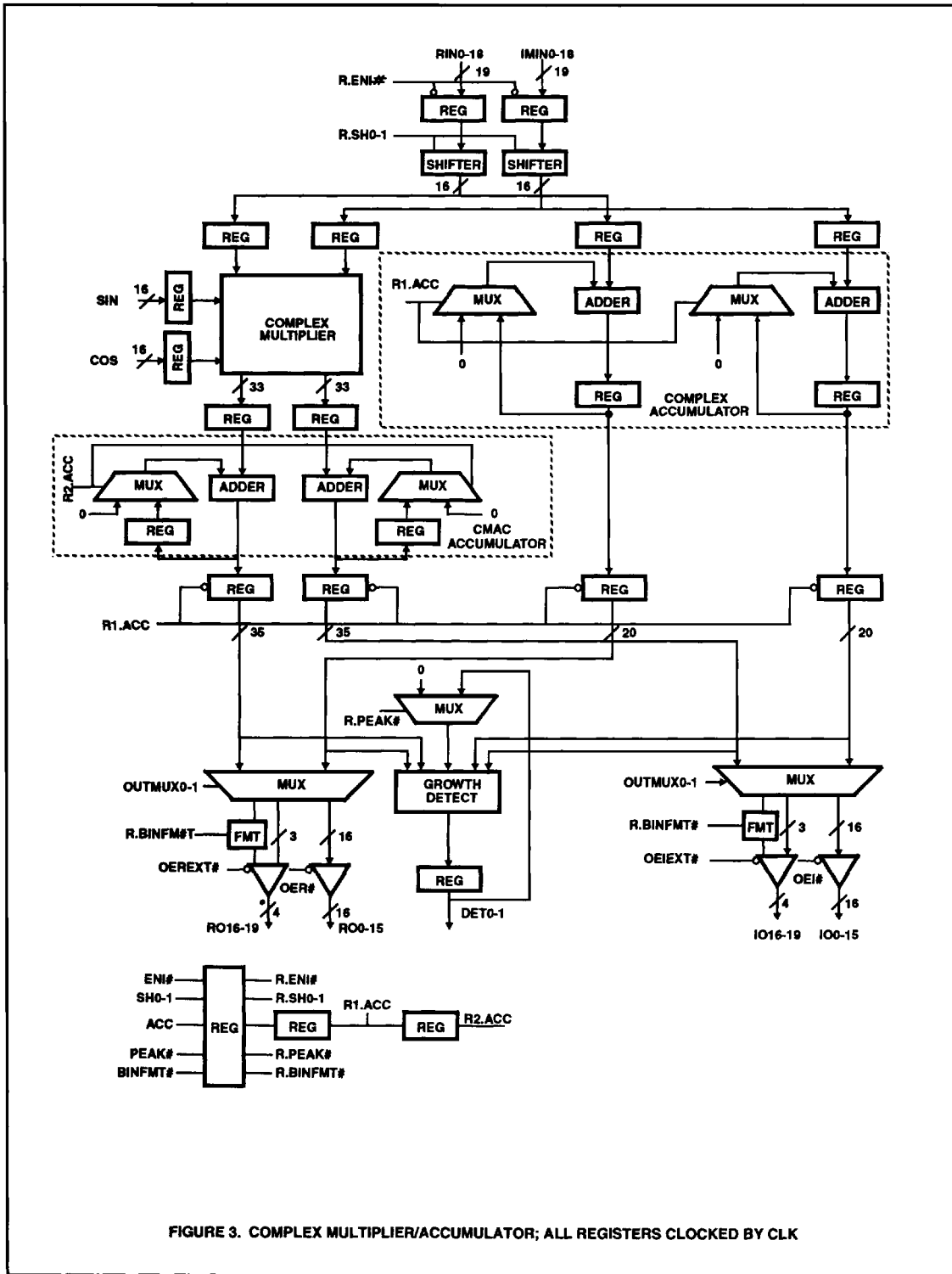


FIGURE 3. COMPLEX MULTIPLIER/ACCUMULATOR; ALL REGISTERS CLOCKED BY CLK

The Complex Accumulator duplicates the accumulator in the CMAC. The input comes from the data shifters, and its 20 bit complex output goes to the Multiplexer. ACC controls whether the accumulator is enabled or not. OUTMUX0-1 determines whether the accumulator output appears on ROUT and IOUT.

The Growth Detect circuitry outputs a two bit value that signifies the amount of growth on the data in the CMAC and Complex Accumulator. Its output, DET0-1, is encoded as shown in Table 5. If PEAK# is low, the highest value of DET0-1 is latched in the Growth Detect Output Register.

The relative weighting of the bits at the inputs and outputs of the CMAC is shown in figure 4. Note that the binary point of the sine, cosine, RIN and IIN is to the right of the most signif-

icant bit, while the binary point of RO and IO is to the right of the fifth most significant bit. These CMAC external input and output busses are aligned with each other to facilitate cascading NCOM's for FFT applications.

TABLE 5. GROWTH ENCODING

DET 1	DET 0	NUMBER OF BITS OF GROWTH ABOVE 2 ⁰
0	0	0
0	1	1
1	0	2
1	1	3

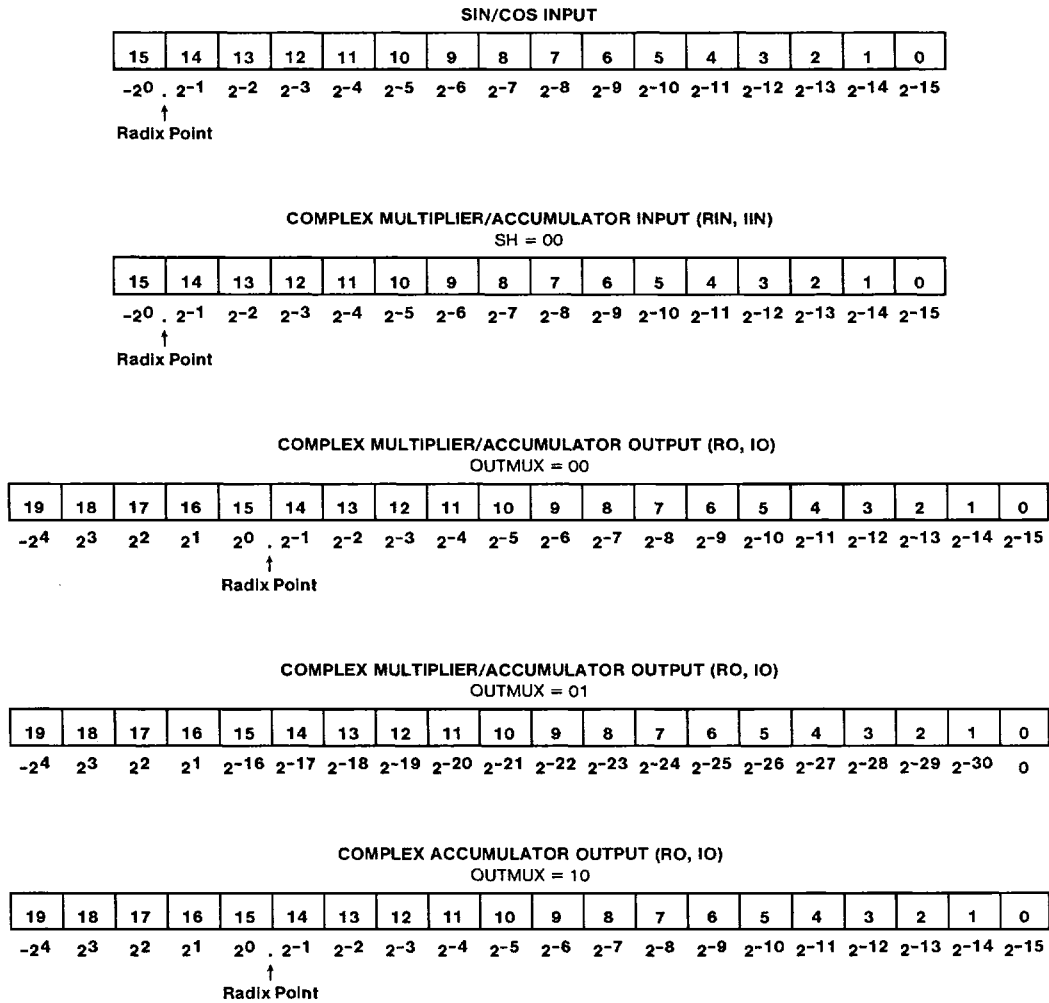


FIGURE 4. BIT WEIGHTING

HSP45116A Description and Operation

The operation of the HSP45116A is identical to the HSP45116 with the exception of a programmable rounding option added for the data outputs. The added functionality was achieved by using one of the HSP45116's reserved configuration registers to specify rounding precision and replacing a V_{CC} pin with a round enable (RND#) input. When RND# is "high", rounding is disabled, and the HSP45116A functions as a pin-for-pin equivalent of the HSP45116. When RND# is active "low" rounding is enabled. The RND# input replaces V_{CC} on PIN 75 of the 160 Lead MQFP package as seen in the pinout diagram.

rounding operation is determined by the least significant 8 bits loaded into the control register as shown in Table 6. The least significant four bits (C3-0) loaded into the register govern rounding of the real and imaginary outputs of the Complex Accumulator (ACC). The next more significant four bits (C7-4) govern the rounding of the complex outputs of the complex multiply accumulator (CMAC). The real and imaginary outputs from the CMAC or ACC are rounded to the same precision. The rounding is performed by adding a "one" to the bit position below the least significant bit desired in the output. For example, for a configuration that rounds to the most significant 20 bits of the CMAC output, a "one" would be added to bit position 2^{14} (See Figure 4 for output bit weightings).

The Round Control Register is loaded by placing the round control value on C15-0, setting AD1-0 = 11, setting CS# = 0, and forcing a low to high transition on the WR# input. The

TABLE 6. ROUNDING CONTROL

ROUND CONTROL REGISTER			ROUNDING OPERATION
C15-8	C7-4	C3-0	
UNUSED	CMAC ROUNDING	ACC ROUNDING	
XXXXXXXX	0000	0000	No Rounding
XXXXXXXX	0001	0001	CMAC outputs rounded to most significant 20 bits, bit positions -2^4 to 2^{15} ACC outputs rounded to most significant 20 bits, bit positions -2^4 to 2^{15}
XXXXXXXX	0010	0010	CMAC outputs rounded to most significant 19 bits, bit positions -2^4 to 2^{14} ACC outputs rounded to most significant 19 bits, bit positions -2^4 to 2^{14}
XXXXXXXX	0011	0011	CMAC outputs rounded to most significant 18 bits, bit positions -2^4 to 2^{13} ACC outputs rounded to most significant 18 bits, bit positions -2^4 to 2^{13}
XXXXXXXX	0100	0100	CMAC outputs rounded to most significant 17 bits, bit positions -2^4 to 2^{12} ACC outputs rounded to most significant 17 bits, bit positions -2^4 to 2^{12}
XXXXXXXX	0101	0101	CMAC outputs rounded to most significant 16 bits, bit positions -2^4 to 2^{11} ACC outputs rounded to most significant 16 bits, bit positions -2^4 to 2^{11}
XXXXXXXX	0110	0110	CMAC outputs rounded to most significant 15 bits, bit positions -2^4 to 2^{10} ACC outputs rounded to most significant 15 bits, bit positions -2^4 to 2^{10}
XXXXXXXX	0111	0111	CMAC outputs rounded to most significant 14 bits, bit positions -2^4 to 2^9 ACC outputs rounded to most significant 14 bits, bit positions -2^4 to 2^9
XXXXXXXX	1000	1000	CMAC outputs rounded to most significant 13 bits, bit positions -2^4 to 2^8 ACC outputs rounded to most significant 13 bits, bit positions -2^4 to 2^8
XXXXXXXX	1001	1001	CMAC outputs rounded to most significant 12 bits, bit positions -2^4 to 2^7 ACC outputs rounded to most significant 12 bits, bit positions -2^4 to 2^7
XXXXXXXX	1010	1010	CMAC outputs rounded to most significant 11 bits, bit positions -2^4 to 2^6 ACC outputs rounded to most significant 11 bits, bit positions -2^4 to 2^6
XXXXXXXX	1011	1011	CMAC outputs rounded to most significant 10 bits, bit positions -2^4 to 2^5 ACC outputs rounded to most significant 10 bits, bit positions -2^4 to 2^5
XXXXXXXX	1100	1100	CMAC outputs rounded to most significant 9 bits, bit positions -2^4 to 2^4 ACC outputs rounded to most significant 9 bits, bit positions -2^4 to 2^4
XXXXXXXX	1101-1111	1101-1111	Undefined

Applications

The NCOM can be used for Amplitude, Phase and Frequency modulation, as well as in variations and combinations of these techniques, such as QAM. It is most effective in applications requiring multiplication of a rotating complex sinusoid by an external vector. These include AM and QAM modulators and digital receivers. The NCOM implements AM and QAM modulation on a single chip, and is a element in demodulation, where it performs complex down conversion. It can be combined with the Harris HSP43220 Decimating Digital Filter to form the front end of a digital receiver.

Modulation/Demodulation

Figure 5 shows a block diagram of an AM modulator. In this example, the phase increment for the carrier frequency is loaded into the center frequency register, and the modulating input is clocked into the real input of the CMAC, with the imaginary input set to 0. The modulated output is obtained at the real output of the CMAC. With a sixteen bit, two's complement signal input, the output will be a 16 bit real number, on ROU0-15 (with OUTMUX = 00).

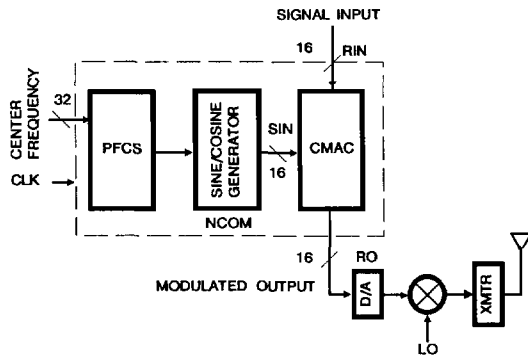


FIGURE 5. AMPLITUDE MODULATION

By replacing the real input with a complex vector, a similar setup can generate QAM signals (Figure 6). In this case, the carrier frequency is loaded into the center frequency register as before, but the modulating vector now carries both amplitude and phase information. Since the input vector and the internally generated sine and cosine waves are both 16 bits, the number of states is only limited by the characteristics of the transmission medium and by the analog electronics in the transmitter and receiver.

The phase and amplitude resolution for the Sine/Cosine section (16 bit output), delivers a spectral purity of greater than 90dBc. This means that the unwanted spectral components due to phase uncertainty (phase noise) will be greater than 90dB below the desired output (dBc, decibels below the carrier). With a 32 bit phase accumulator in the Phase/

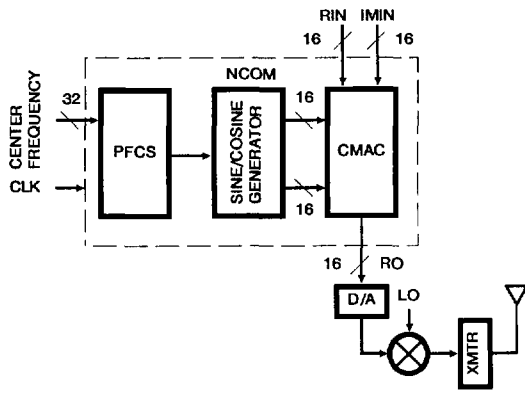


FIGURE 6. QUADRATURE AMPLITUDE MODULATION (QAM)

Frequency Control Section, the frequency tuning resolution equals the clock frequency divided by 2^{32} . For example, a 25MHz clock gives a tuning resolution of 0.006Hz.

The NCOM also works with the HSP43220 Decimating Digital Filter to implement down conversion and low pass filtering in a digital receiver (Figure 7). The NCOM performs complex down conversion on the wideband input signal by multiplying the input vector and the internally generated complex sinusoid. The resulting signal has components at twice the center frequency and at DC. Two HSP43220's, one each on the real and imaginary outputs of the HSP45116, perform low pass filtering and decimation on the down converted data, resulting in a complex baseband signal.

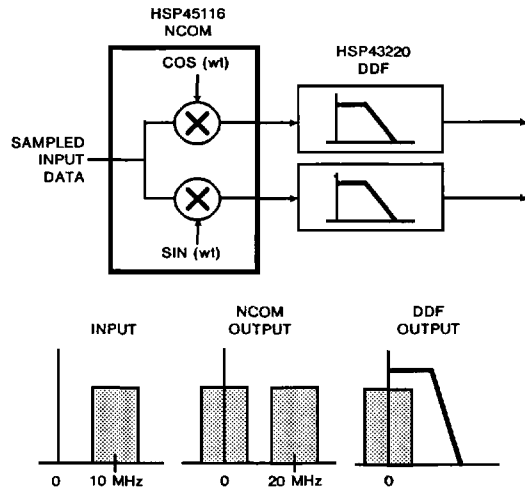


FIGURE 7. CHANNELIZED RECEIVER CHIP SET

FFT Butterfly

Figure 8 shows a Fast Fourier Transform (FFT) implementation. The FFT is a highly efficient way of calculating the Discrete Fourier Transform [1]. The basic building block in FFTs is called the butterfly. The butterfly calculation involves adding complex numbers and multiplying by complex sinusoids. The Phase/Frequency Control Section and Sine/Cosine Generator provide the complex sinusoids and the CMAC performs the complex multiplies and adds.

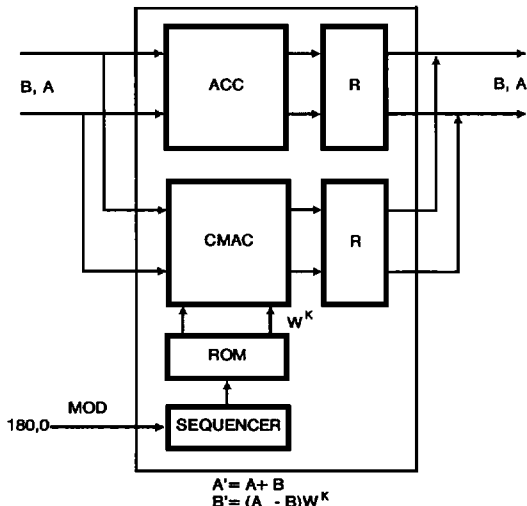


FIGURE 8. RADIX-2 FFT BUTTERFLY

The NCOM circuit shown implements the butterfly shown in Figure 9. The two complex inputs A and B produce two complex outputs A' and B' using the equations $A' = A + B$, $B' = (A - B)W^k$ where $W^k = e^{-jwk} = \cos(wk) + j\sin(wk)$. Two clock cycles are required to calculate the butterfly. A is clocked into the chip first and then B is clocked in. The complex accumulator in the CMAC section adds A and B. The

CMAC calculates $(A - B)W^k$ as $AW^k + B(-W^k)$. $-W^k$ is generated by phase shifting the ROM address 180 degrees using the phase modulation inputs. For radix-2 decimation in frequency FFTs, the phase of the complex sinusoid starts at 0 degrees and increments by a fixed step size (for each pass) after each butterfly. The phase/frequency section is initialized to 0 degrees and the frequency control loaded with the appropriate phase step size for the pass. The resulting words, A' and B', are held in output registers and multiplexed through the output pins for writing to memory. Using a single NCOM clocked at 25MHz, a 1024 point radix-2 FFT can be computed in $(\text{CLK period}) \times (N \log_2 N)$, or 410 microseconds.

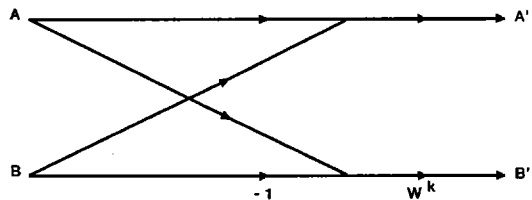


FIGURE 9. DECIMATION IN FREQUENCY BUTTERFLY

Circuitry is included to implement block floating point FFTs. In block floating point, an exponent is generated for an entire block of data. To implement block floating point, the maximum bit growth during a set of calculations is detected. The number of bits of growth is used to adjust the block's exponent and to scale the block on the next set of calculations to maintain a desired number of bits of precision. This technique requires less memory than true floating point and yields better performance than fixed point implementations, though its resolution does not meet that of true floating point implementations.

References

[1] Oppenheim, A. V. and Schaffer, R. W., *Discrete Time Signal Processing*, Prentice Hall

Specifications HSP45116

Absolute Maximum Ratings

Supply Voltage	+8.0V
Input, Output or I/O Voltage Applied.....	GND -0.5V to $V_{CC} + 0.5V$
Storage Temperature Range	-65°C to +150°C
Junction Temperature	
MQFP	+150°C
PGA	+175°C
Lead Temperature (Soldering 10s).....	+150°C
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
MQFP Package	22.0°C/W	7.7°C/W
PGA Package	23.1°C/W	8.3°C/W
Maximum Package Power Dissipation		
MQFP	3.6W	
PGA	4.55W	
Component Count.....	103,000 Transistors	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.75V to +5.25V	Operating Temperature Range	0°C to +70°C
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DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	$V_{CC} = 5.25V$
Logical Zero Input Voltage	V_{IL}	-	0.8	V	$V_{CC} = 4.75V$
High Level Clock Input	V_{IHC}	3.0	-	V	$V_{CC} = 5.25V$
Low Level Clock Input	V_{ILC}	-	0.8	V	$V_{CC} = 4.75V$
Output HIGH Voltage	V_{OH}	2.6	-	V	$I_{OH} = -400mA, V_{CC} = 4.75V$
Output LOW Voltage	V_{OL}	-	0.4	V	$I_{OL} = +2.0mA, V_{CC} = 4.75V$
Input Leakage Current	I_I	-10	10	μA	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$
I/O Leakage Current	I_O	-10	10	μA	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 5.25V$
Standby Power Supply Current	I_{CCSB}	-	500	μA	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.25V$, Note 3
Operating Power Supply Current	I_{CCOP}	-	150	mA	$f = 15MHz, V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$, Notes 1 and 3

Capacitance $T_A = +25^\circ C$, Note 2

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}	-	15	pF	FREQ = 1MHz, $V_{CC} =$ Open, All measurements are referenced to device ground
Output Capacitance	C_O	-	15	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 10mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Output load per test load circuit with switch open and $C_L = 40pF$.

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SIGNAL SYNTHESIZERS

Specifications HSP45116

A.C. Electrical Specifications $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ (Note 1)

SYMBOL	PARAMETER	-15 (15MHz)		-25 (25.6MHz)		-33 (33MHz)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
T_{CP}	CLK Period	66		39		30		ns	
T_{CH}	CLK High	26		15		12		ns	
T_{CL}	CLK Low	26		15		12		ns	
T_{WL}	WR# Low	26		15		12		ns	
T_{WH}	WR# High	26		15		12		ns	
T_{AWS}	Set-up Time; ADO-1, CS# to WR# Going High	18		13		13		ns	
T_{AWH}	Hold Time; ADO, AD1, CS# from WR# Going High	0		0		0		ns	
T_{CWS}	Set-up Time C0-15 from WR# Going High	20		15		15		ns	
T_{CWH}	Hold Time C0-15 from WR# Going High	0		0		0		ns	
T_{WC}	Set-up time WR# High to CLK High	20		16		12		ns	Note 3
T_{MCS}	Set-up Time MODO-1 to CLK Going High	20		15		15		ns	
T_{MCH}	Hold Time MODO-1 from CLK Going High	0		0		0		ns	
T_{PCS}	Set-up Time PACI# to CLK Going High	25		15		11		ns	
T_{PCH}	Hold Time PACI# from CLK Going High	0		0		0		ns	
T_{ECS}	Set-up ENPHREG#, ENCFREG#, ENOFREG#, ENPHAC#, ENTIREG#, CLROFR#, PMSSEL, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SHO-1, RBYTILD# from CLK Going High	18		12		12		ns	
T_{ECH}	Hold Time ENPHREG#, ENCFREG#, ENOFREG#, ENPHAC#, ENTIREG#, CLROFR#, PMSSEL, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SHO-1, RBYTILD# from CLK Going High	0		0		0		ns	
T_{DS}	Set-up Time RINO-18, IMINO-18 to CLK Going High	18		12		12		ns	
T_{DH}	Hold Time RINO-18, IMINO-18 from CLK Going High	0		0		0		ns	
T_{DO}	CLK to Output Delay ROO-19, IOO-19		40		24		19	ns	
T_{DEO}	CLK to Output Delay DETO-1		40		27		20	ns	
T_{PO}	CLK to Output Delay PACO#		30		20		12	ns	
T_{TO}	CLK to Output Delay TICO#		30		20		12	ns	
T_{OE}	Output Enable Time OER#, OEI#, OEREXT#, OEIEXT#		25		20		20	ns	
T_{MD}	OUTMUX0-1 to Output Delay		40		28		26	ns	
T_{OD}	Output Disable Time		20		15		15	ns	Note 2
T_{RF}	Output Rise, Fall Time		8		8		6	ns	Note 2

NOTES:

- A.C. testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with switch closed and $C_L = 40pF$. Output transition is measured at $V_{OH} \geq 1.5V$ and $V_{OL} \leq 1.5V$.
- Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
- Applicable only when outputs are being monitored and ENCFREG#, ENPHREG#, or ENTIREG# is active.

Specifications HSP45116A Preliminary

Absolute Maximum Ratings

Supply Voltage	+7.0V
Input, Output Voltage	GND -0.5V to V_{CC} +0.5V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 10s)	+300°C
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
MQFP Package	22.0°C/W	7.7°C/W
Maximum Package Power Dissipation at TBD		
Gate Count	26,000 Gates	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	Operating Temperature Range
Commercial	Commercial
+4.75V to +5.25V	0°C to +70°C

Electrical Specifications $(V_{CC} = 5.0V \pm 5\%, T_A = 0^\circ \text{ to } +70^\circ\text{C})$

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Power Supply Current	I_{CCOP}	-	TBD	mA	$V_{CC} = \text{Max}$, CLK Frequency 52.6Mhz Notes 1, 2
Standby Power Supply Current	I_{CCSB}	-	500	μA	$V_{CC} = \text{Max}$, Outputs Not Loaded
Input Leakage Current	I_I	-10	10	μA	$V_{CC} = \text{Max}$, Input = 0V or V_{CC}
Output Leakage Current	I_O	-10	10	μA	$V_{CC} = \text{Max}$, Input = 0V or V_{CC}
Logical One Input Voltage	V_{IH}	2.0	-	V	$V_{CC} = \text{Max}$
Logical Zero Input Voltage	V_{IL}	-	0.8	V	$V_{CC} = \text{Min}$
Logical One Input Voltage: CLK	V_{IHC}	3.0	-	V	$V_{CC} = \text{Max}$
Logical One Output Voltage	V_{OH}	2.6	-	V	$I_{OH} = -5\text{mA}$, $V_{CC} = \text{Min}$
Logical Zero Output Voltage	V_{OL}	-	0.4	V	$I_{OL} = 5\text{mA}$, $V_{CC} = \text{Min}$
Input Capacitance	C_{IN}	-	10	pF	CLK Frequency 1MHz All measurements referenced to GND. $T_A = +25^\circ\text{C}$, Note 3
Output Capacitance	C_{OUT}	-	10	pF	

NOTES:

1. Power supply current is proportional to frequency. Typical rating is TBD mA/MHz. Note that operation at maximum clock frequency will exceed maximum junction temperature of device. Use of a heat sink and/or air flow is required under these conditions: recommended heat sink is TBD.
2. Output load per test circuit and $C_L = 40\text{pF}$.
3. Not tested, but characterized at initial design and at major process/design changes.

AC Electrical Specifications $V_{CC} = 5.0V \pm 5\%, T_A = 0^\circ \text{ to } +70^\circ\text{C}$, (Note 1)

PARAMETER	SYMBOL	52MHz (-52) (PRELIMINARY)		COMMENTS
		MIN	MAX	
CLK Period	T_{CP}	19	-	ns
CLK High	T_{CH}	7	-	ns
CLK Low	T_{CL}	7	-	ns
WR# Low	T_{WL}	7	-	ns

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SIGNAL SYNTHESIZERS

Specifications HSP45116A Preliminary

AC Electrical Specifications $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^\circ$ to $+70^\circ C$, (Note 1)

PARAMETER	SYMBOL	52MHz (-52) (PRELIMINARY)		COMMENTS
		MIN	MAX	
WR# High	T_{WH}	7	-	ns
Setup Time AD0-1, CS# to WR#	T_{AWS}	10	-	ns
Hold Time AD0-1, CS# from WR#	T_{AWH}	0	-	ns
Setup Time C0-15 to WR#	T_{CWS}	10	-	ns
Hold Time C0-15 from WR#	T_{CWH}	0	-	ns
Setup Time WR# to CLK	T_{WC}	10	-	ns, Note 3
Setup Time MOD0-1 to CLK	T_{MCS}	10	-	ns
Hold Time MOD0-1 from CLK	T_{MCH}	0	-	ns
Setup Time PACI# to CLK	T_{PCS}	10	-	ns
Hold Time PACI# from CLK	T_{PCH}	0	-	ns
Setup Time ENPHREG#, ENCFREG#, ENOFREG#, ENPHAC#, ENTIREG#, CLROFFR#, PMSEL, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# to CLK	T_{ECS}	10	-	ns
Hold Time ENPHREG#, ENCFREG#, ENOFREG#, ENPHAC#, ENTIREG#, CLROFFR#, PMSEL, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK	T_{ECH}	0	-	ns
Setup Time RIN0-18, IMIN0-18 to CLK	T_{DS}	10	-	ns
Hold Time RIN0-18, IMIN0-18 from CLK	T_{DH}	0	-	ns
CLK to Output Delay RO0-19, IO0-19	T_{DO}	-	12	ns
CLK to Output Delay DET0-1	T_{DEO}	-	12	ns
CLK to Output Delay PACO#	T_{PO}	-	12	ns
CLK to Output Delay TICO#	T_{TO}	-	12	ns
Output Enable Time OER#, OEI#, OER-EXT#, OEIEXT#	T_{OE}	-	8	ns
Output Enable Time OUTMUX0-1	T_{MD}	-	14	ns
Output Disable Time	T_{OD}	-	8	ns, Note 2
Output Rise, Fall Time	T_{RF}	-	6	ns, Note 2

NOTES:

- AC tests performed with $C_L = 40pF$, $I_{OL} = TBd mA$, and $I_{OH} = -TBd mA$. Input reference level for CLK = 2.0V, all other inputs 1.5V. Test $V_{IH} = 3.0V$, $V_{IHC} = 4.0V$, $V_{IL} = 0V$; $V_{OH} = TBDV$, $V_{OL} = TBDV$.
- Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
- Applicable only when outputs are being monitored and ENCFREG#, ENPHREG# or ENTIREG# is active.

Specifications HSP45116TM Preliminary

Absolute Maximum Ratings

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.5V to $V_{CC} + 0.5V$
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+175°C
Lead Temperature (Soldering 10s)	300°C
ESD Classification	Class 1

Reliability Information

Device Count	103,000 Transistors
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CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.5V to +5.5V	Operating Temperature Range	-55°C to +125°C
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DC Electrical Specifications $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.2	-	V	$V_{CC} = 5.5V$
Logical Zero Input Voltage	V_{IL}	-	0.8	V	$V_{CC} = 4.5V$
Logical One Input Voltage Clock	V_{IHC}	3.0	-	V	$V_{CC} = 5.5V$
Logical Zero Input Voltage Clock	V_{ILC}	-	0.8	V	$V_{CC} = 4.5V$
Output HIGH Voltage	V_{OH}	2.6	-	V	$I_{OH} = -400\mu A$, $V_{CC} = 4.5V$ (Note 1)
Output LOW Voltage	V_{OL}	-	0.4	V	$I_{OL} = +2.0mA$, $V_{CC} = 4.5V$ (Note 1)
Input Leakage Current	I_I	-10	+10	μA	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5V$
Output or I/O Leakage Current	I_O	-10	+10	μA	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 5.5V$
Standby Power Supply Current	I_{CCSB}	-	500	μA	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5V$, (Note 4)
Operating Power Supply Current	I_{CCOP}	-	150	mA	$f = 15MHz$, $V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5V$ (Notes 2, 4)
Functional Test	FT	-	-		(Note 3)

NOTES:

- Interchanging of force and sense conditions is permitted.
- Operating Supply Current is proportional to frequency, typical rating is 10mA/MHz.
- Tested as follows: $f = 1MHz$, V_{IH} (clock inputs) = 3.4V, V_{IH} (all other inputs) = 2.6V, $V_{IL} = 0.4V$, $V_{OH} \geq 1.5V$, and $V_{OL} \leq 1.5V$.
- Output per test load circuit with switch open and $C_L = 40pF$.

AC Electrical Specifications $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$

PARAMETER	SYMBOL	-15 (15MHz)		-25 (25.6MHz)		UNITS	(NOTE 1) CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Period	T_{CP}	66	-	39	-	ns	
CLK High	T_{CH}	26	-	15	-	ns	
CLK Low	T_{CL}	26	-	15	-	ns	
WR# Low	T_{WL}	26	-	15	-	ns	
WR# High	T_{WH}	26	-	15	-	ns	
Set-up Time; AD0-1, CS# to WR# Going High	T_{AWS}	20	-	18	-	ns	
Hold Time; AD0, AD1, CS# from WR# Going High	T_{AWH}	0	-	0	-	ns	
Set-up Time C0-15 from WR# Going High	T_{CWS}	20	-	18	-	ns	

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SIGNAL SYNTHESIZERS

Specifications HSP45116TM Preliminary

AC Electrical Specifications $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (Continued)

PARAMETER	SYMBOL	-15 (15MHz)		-25 (25.6MHz)		UNITS	(NOTE 1) CONDITIONS
		MIN	MAX	MIN	MAX		
Hold Time C0-15 from WR# Going High	T_{CWH}	0	-	0	-	ns	
Set-up Time WR# to CLK High	T_{WC}	20	-	16	-	ns	(Note 2)
Set-up Time MOD0-1 to CLK Going High	T_{MCS}	20	-	18	-	ns	
Hold Time MOD0-1 from CLK Going High	T_{MCH}	0	-	0	-	ns	
Set-up Time PACI# to CLK Going High	T_{PCS}	25	-	18	-	ns	
Hold Time PACI# from CLK Going High	T_{PCH}	0	-	0	-	ns	
Set-up Time ENPHREG#, ENCFRCTL#, ENPHAC#, ENTICTL#, CLROFR#, PMSEL#, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK Going High	T_{ECS}	20	-	15	-	ns	
Hold Time ENPHREG#, ENCFRCTL#, ENPHAC#, ENTICTL#, CLROFR#, PMSEL#, LOAD#, ENI#, ACC, BINFMT#, PEAK#, MODPI/2PI#, SH0-1, RBYTILD# from CLK Going High	T_{ECH}	0	-	0	-	ns	
Set-up Time RIN0-18, IMIN0-18 to CLK Going High	T_{DS}	20	-	15	-	ns	
Hold Time RIN0-18, IMIN0-18, to CLK Going High	T_{DH}	0	-	0	-	ns	
CLK to Output Delay, ROO-19, IO0-19	T_{DO}	-	40	-	25	ns	
CLK to Output Delay, DET0-1	T_{DEO}	-	40	-	27	ns	
CLK to Output Delay, PACO#	T_{PO}	-	30	-	20	ns	
CLK to Output Delay, TICO#	T_{TO}	-	30	-	20	ns	
Output Enable Time, OER#, OEI#, OEREXT#, OEIEXT#	T_{OE}	-	25	-	20	ns	(Note 3)
OUTMUX0-1 to Output Delay	T_{MD}	-	40	-	28	ns	

NOTES:

- AC testing is performed as follows: $V_{CC} = 4.5\text{V}$ and 5.5V . Input levels (CLK Input) 4.0V and 0V ; Input levels (all other inputs) 3.0V and 0V ; Timing reference levels (CLK) 2.0V ; All others 1.5V . Output load per test load circuit with switch closed and $C_L = 40\text{pF}$. Output transition is measured at $V_{OH} \geq 1.5\text{V}$ and $V_{OL} \leq 1.5\text{V}$.
- Applicable only when outputs are being monitored and ENCFREG#, ENPHREG#, or ENTIREG# is active.
- Transition is measured at $\pm 200\text{mV}$ from steady state voltage. Output loading per test load circuit, with switch closed and $C_L = 40\text{pF}$.

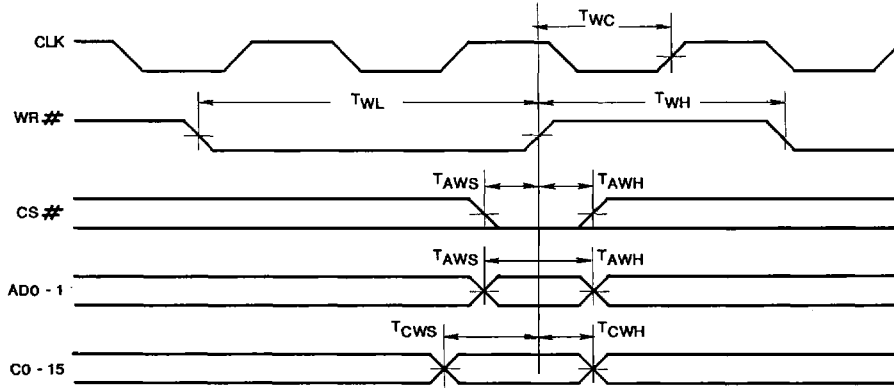
Electrical Specifications

PARAMETER	SYMBOL	NOTES	-15		-25		UNITS	CONDITIONS
			MIN	MAX	MIN	MAX		
Output Disable Time	T_{OD}	1, 2	-	20	-	15	ns	
Output Rise Time	T_R	1, 2	-	8	-	8	ns	From 0.8V to 2.0V
Output Fall Time	T_F	1, 2	-	8	-	8	ns	From 2.0V to 0.8V

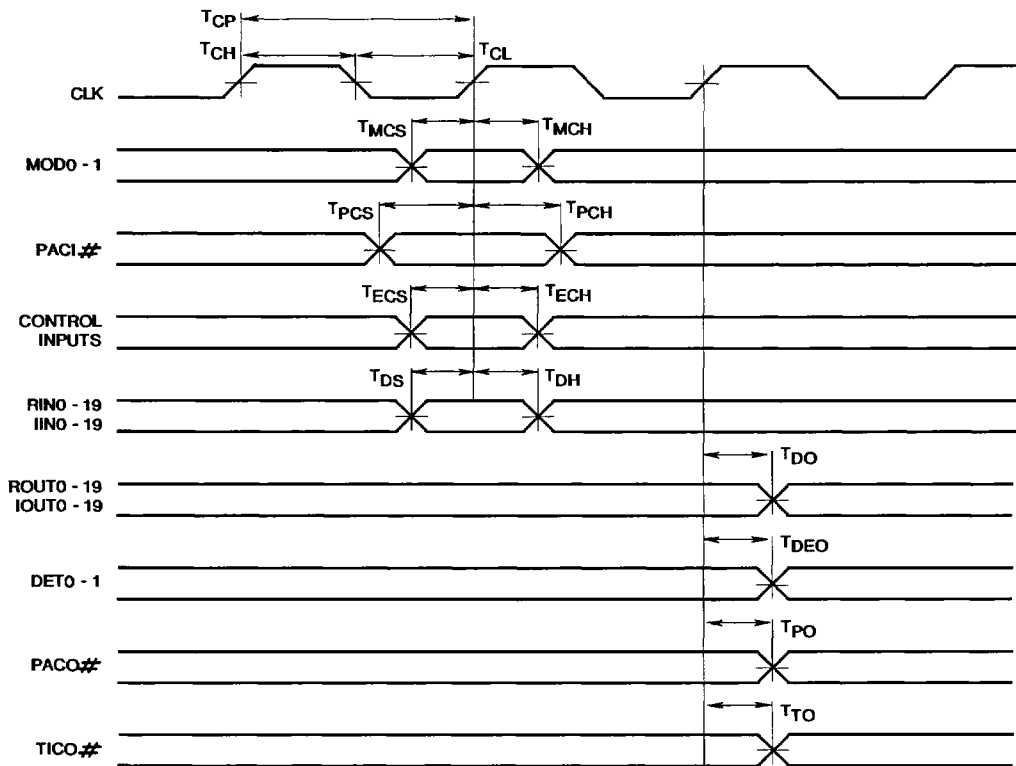
NOTES:

- The parameters in this table are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
- Loading is as specified in the test load circuit with $C_L = 40\text{pF}$.

Waveforms

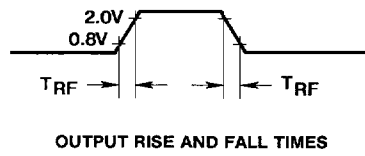
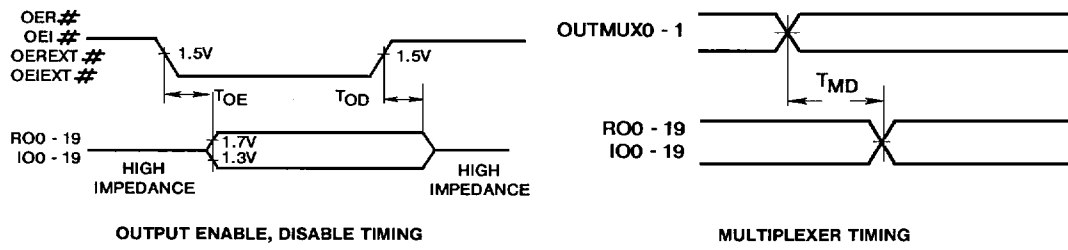


CONTROL BUS TIMING

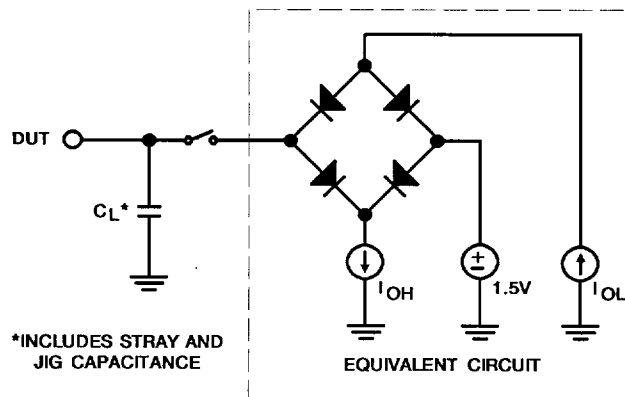


INPUT AND OUTPUT TIMING

Waveforms (Continued)



Test Load Circuit



*INCLUDES STRAY AND JIG CAPACITANCE

Switch S1 open for ICCSB and ICCOP tests

EQUIVALENT CIRCUIT