Preliminary

XRD64L06

CMOS

3V, 6 MSPS, 10-Bit, High Speed Analog-to-Digital Converter

January 1999-2

FEATURES

- 10-Bit Resolution
- Sampling Rate to 6 MSPS
- DNL = ±1 LSB, INL = ±2 LSB
- Internal S/H Function
- Single 3V Power Supply
- V_{IN} DC Range: 0V to V_{DD}
- V_{REF} DC Range: 1V to V_{DD}
- Low Power: 30mW
- Three-State Digital Outputs
- Latch-Up Free
- Pin Compatible With: MP87L84

APPLICATIONS

- Digital Color Copiers
- Precision CCDs and Scanners
- Digital Radio

BENEFITS

- Simplified Analog Design
- Rugged
- Few External Components, no S/H Needed
- Reduced Board Space

GENERAL DESCRIPTION

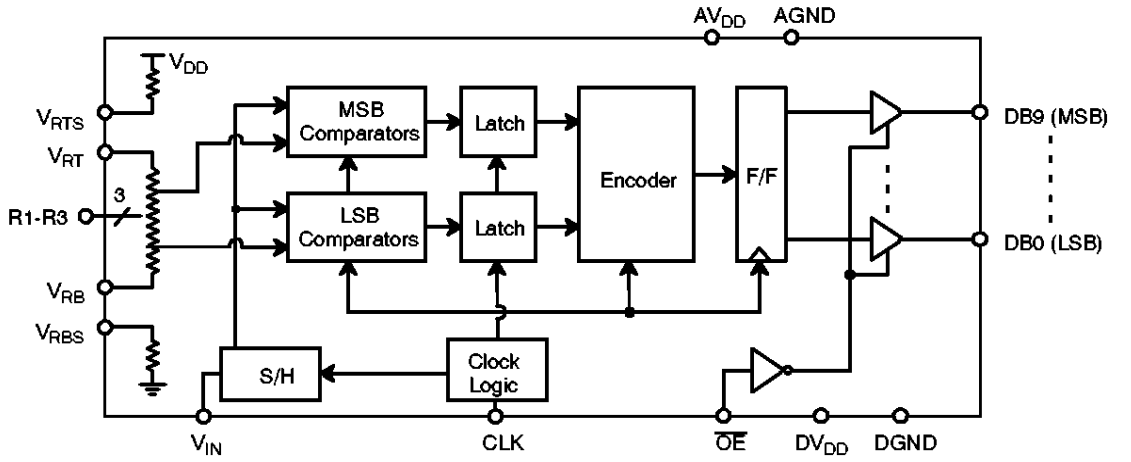
The XRD64L06 is a 3V, 10-bit, 6 MSPS, Analog-to-Digital Converter for applications that require high speed and high accuracy. Designed using an advanced CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The XRD64L06 uses a subranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance. The input circuitry of the XRD64L06 includes an on-chip S/H function that allows this part to digitize analog input signals between AGND and AV_{DD}.

The designer can choose the internally generated reference voltages, or provide external reference voltages to the V_{RB} and V_{RT} pins. The internal reference generates 0.6V at V_{RB} and 2.4V at V_{RT}. Providing external reference voltages allows easy interface to any input signal range between GND and V_{DD}. This also allows the system to cancel zero scale and full scale errors. The Reference Ladder taps (R1 to R3) can be used to externally trim any INL errors.

This device operates from a single 3V supply. Power consumption from a 3V supply is typically 30mW at F_S=6MHz.

SIMPLIFIED BLOCK DIAGRAM



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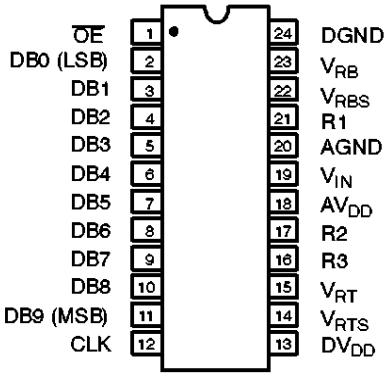
ORDERING INFORMATION

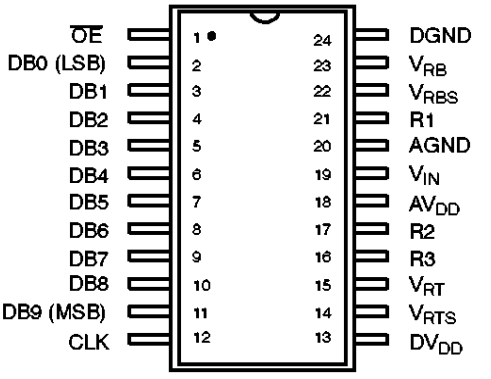
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	-40 to +85°C	XRD64L06AIP	±1	±2
SOIC	-40 to +85°C	XRD64L06AID	±1	±2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")



24 Pin SOIC (Jedec, 0.300")

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{OE}$	Output Enable
2	DB0	Data Output Bit 0 (LSB)
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5	Data Output Bit 5
8	DB6	Data Output Bit 6
9	DB7	Data Output Bit 7
10	DB8	Data Output Bit 8
11	DB9	Data Output Bit 9 (MSB)
12	CLK	Clock Input

PIN NO.	NAME	DESCRIPTION
13	DV_{DD}	Digital Power Supply
14	V_{RTS}	Top Internal Reference
15	V_{RT}	Top of Reference
16	R3	3/4 Reference Tap Point
17	R2	1/2 Reference Tap Point
18	AV_{DD}	Analog Power Supply
19	V_{IN}	Analog Input Voltage
20	AGND	Analog Ground
21	R1	1/4 Reference Tap Point
22	V_{RBS}	Bottom Internal Reference
23	V_{RB}	Bottom of Reference
24	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 3V, FS = 6MHz (50% Duty Cycle), V_{RT} = 2.4, V_{RB} = 0.6, T_A = 25°C

Parameter	Symbol	Min	25°C Typ	Max	Units	Test Conditions/Comments
KEY FEATURES						
Resolution		10			Bits	
Maximum Sampling Rate	FS	6			MHz	
ACCURACY (A Grade)[1]						
Differential Non-Linearity	DNL			±1	LSB	
Integral Non-Linearity	INL			±2	LSB	Best Fit Line (Max INL - Min INL)/2
Zero Scale Error	EZS		10		LSB	
Gain Error	EFS		6		LSB	
REFERENCE VOLTAGES						
Positive Ref. Voltage[2,3]	V_{RT}			AV_{DD}	V	
Negative Ref. Voltage[2,3]	V_{RB}	AGND			V	
Differential Ref. Voltage[2,3]	V_{REF}	1.0		AV_{DD}	V	$V_{REF} = V_{RT} - V_{RB}$
Ladder Resistance	R_L		1400		Ω	
Ladder Temp. Coefficient[2]	R_{TCO}		2000		ppm/°C	
Top Internal Reference	V_{RTS}		2.4		V	V_{RT} connected to V_{RTS} &
Bottom Internal Reference	V_{RBS}		0.6		V	V_{RB} connected to V_{RBS}
ANALOG INPUT						
Input Bandwidth (-1 dB)[2,4]	BW		25		MHz	
Input Voltage Range	V_{IN}	V_{RB}		V_{RT}	V	
Input Capacitance (Sample)[2,5]	C_{IN}		25	40	pF	
Input Capacitance (Convert)[2,5]			7	12	pF	
Aperture Delay[2]	t_{AP}		25	30	ns	
Aperture Uncertainty [2] (Jitter)	t_{AJ}		50		ps	
DIGITAL INPUTS						
Logical "1" Voltage	V_{IH}	2.6			V	
Logical "0" Voltage	V_{IL}			0.2	V	
DC Leakage Currents[6]	I_{IN}					V_{IN}=DGND to DV_{DD}
CLK			5		µA	
$\overline{OE}$			5		µA	
Input Capacitance			5		pF	
Clock Timing (*See Figure 1*)						
Clock Period	1/FS		167		ns	
Rise & Fall Time[7]	t_R, t_F		2		ns	
"High" Pulse Width[3]	t_{PWH}		84		ns	
"Low" Pulse Width[3]	t_{PWL}		84		ns	
Duty Cycle[3]			50		%	
DIGITAL OUTPUTS						C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	2.6			V	I_{LOAD} = 2mA
Logical "0" Voltage	V_{OL}			0.2	V	I_{SINK} = 2mA
3-state Leakage	I_{OZ}		10		µA	V_{OUT}=DGND to DV_{DD}
Data Valid Delay	t_{DL}		40	45	ns	
Data Enable Delay	t_{DEN}		25	30	ns	
Data 3-state Delay	t_{DHZ}		25	30	ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Description	Symbol	Min	25°C Typ	Max	Units	Conditions
POWER SUPPLIES						
Operating Voltage (AV_{DD}, DV_{DD})[2, 8, 9]	V_{DD}	2.7	3.0	3.6	V	
Current (AV_{DD} + DV_{DD})	I_{DD}		10	13.5	mA	

Notes:

1 *Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/1024) is the DNL error (Figure 3.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 4.). Accuracy is a function of the sampling rate (FS).*

2 *Guaranteed. Not tested.*

3 *Specified values guarantee functionality, but INL & DNL specifications may not be met.*

4 *–1 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.*

5 *See V_{IN} equivalent circuit (Figure 8.). Switched capacitor analog input requires driver with low output resistance.*

6 *All inputs have diodes to DV_{DD} and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.*

7 *Condition to meet aperture delay specifications (t_{AP}, t_{AJ}). Actual rise/fall time can be less stringent with no loss of accuracy.*

8 *The AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.*

9 *The AV_{DD} & DV_{DD} pins should be tied together at the package.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

AV_{DD} to AGND ..... +7V

V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND –0.5V

V_{IN} ..... V_{DD} +0.5 to GND –0.5V

All Inputs ..... V_{DD} +0.5 to GND –0.5V

All Outputs ..... V_{DD} +0.5 to GND –0.5V

Storage Temperature ..... –65 to +150°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC 1000mW

Derates above 75°C ..... 14mW/°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Notes

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

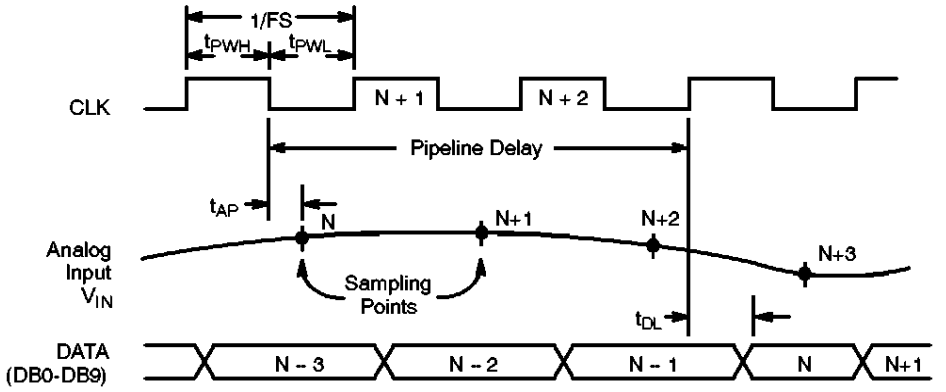


Figure 1. XRD64L06 Timing Diagram

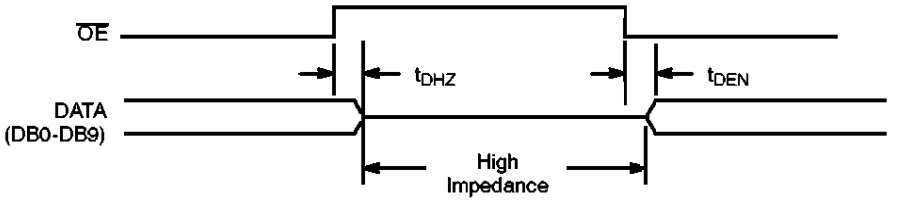


Figure 2. 3-State Timing Diagram

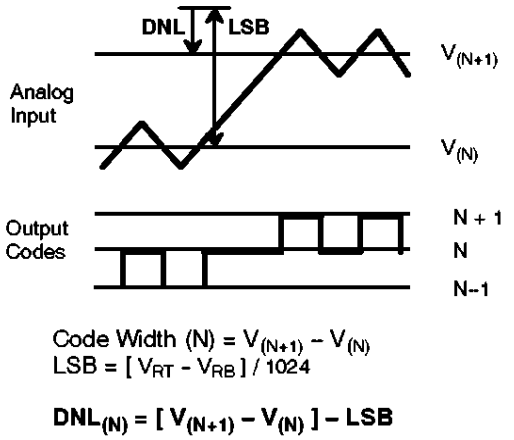


Figure 3. DNL Measurement

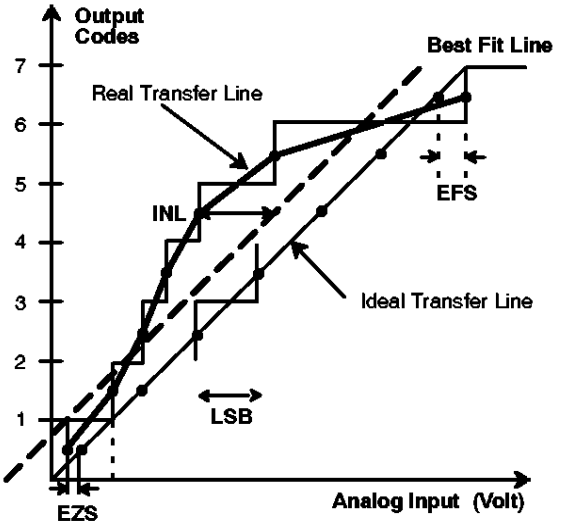


Figure 4. INL Error Calculation

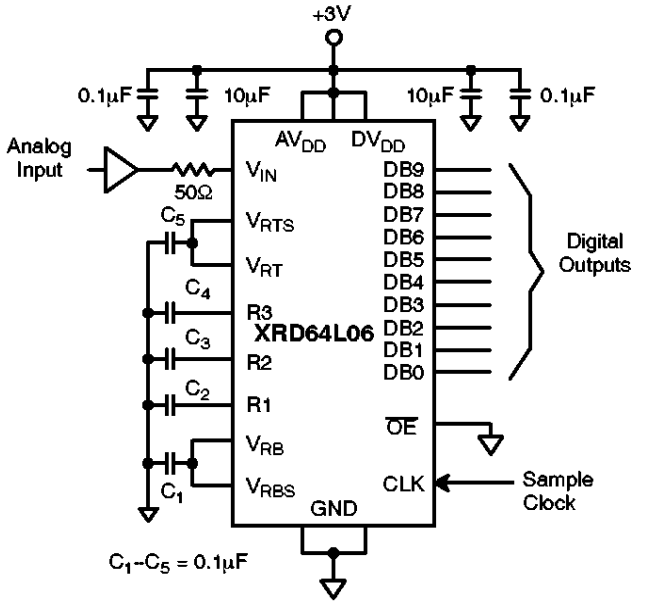


Figure 5. Typical Circuit Connections

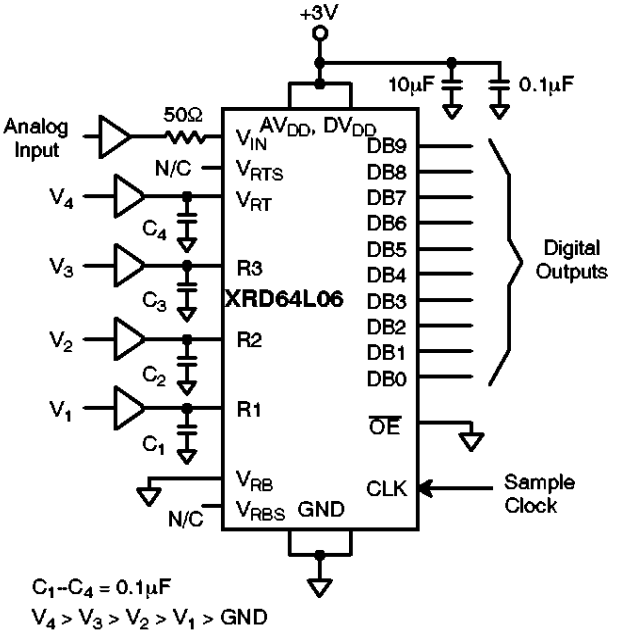


Figure 6. Creating a Piece Wise Linear Transfer Function

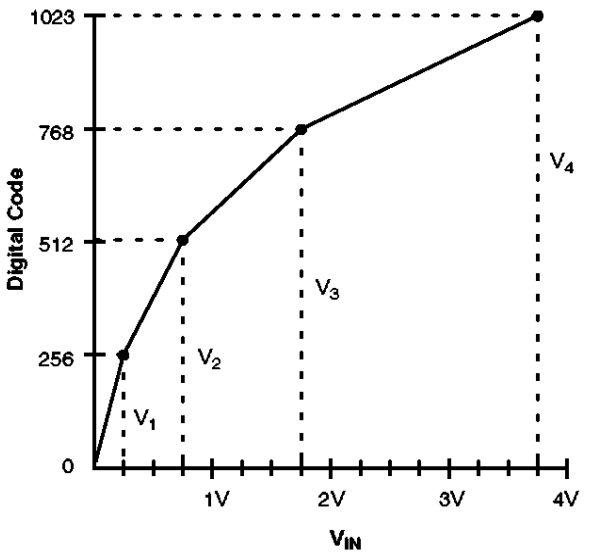


Figure 7. A Piece Wise Linear, Logarithmic Transfer Function

APPLICATION NOTES

Signals should not exceed AV_{DD} or DV_{DD} +0.5V or go below DGND or AGND –0.5V. All pins have internal protection diodes that will protect them from short transients (<100µs) outside the supply range.

AGND and DGND pins are connected internally through the P– substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

The power supply (AV_{DD}) and reference voltage (V_{RT} & V_{RB}) pins should be decoupled with 0.1µF and 10µF capacitors to AGND, placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

V_{IN} Analog Input

This part has a switched capacitor type input circuit. This means that the input impedance changes with the phase of the input clock. V_{IN} is sampled at the high to low clock transition. *Figure 8.* shows an equivalent input circuit.

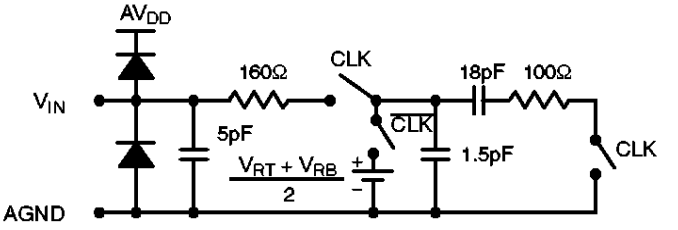


Figure 8. Equivalent Input Circuit

RTS & RBS Internal Bias Resistors

Two matched resistors are provided on the chip. These resistors can be used to generate on chip reference voltages. Each resistor has a value equal to 1/3 of the reference ladder resistor. By connecting RTS to V_{RT}, and connecting RBS to V_{RB}, the reference ladder will be biased to 0.6V at V_{RB} and 2.4V at V_{RT}.

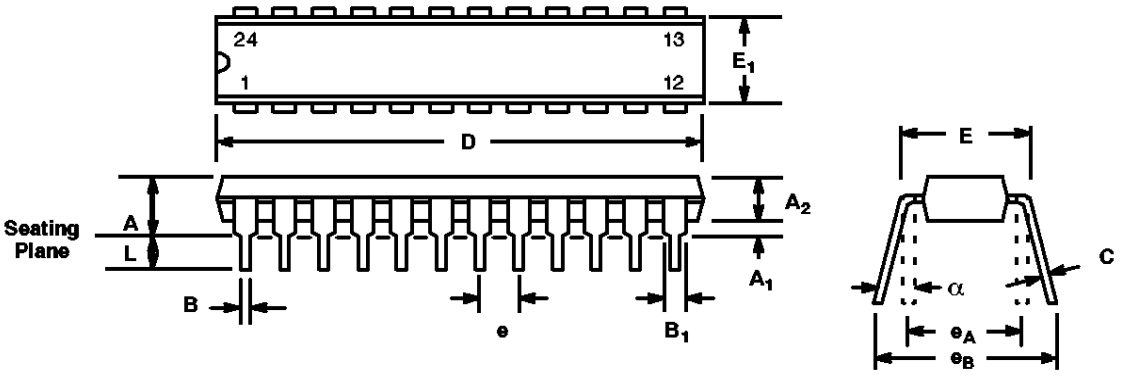
If the internal reference pins V_{RTS} and/or V_{RBS} are not used they should be left unconnected.

R1 thru R3 Reference Ladder Taps

These taps connect to every quarter point along the reference ladder; R1 is 1/4th up from V_{RB}, R3 is 3/4ths up from V_{RB} (or 1/4th down from V_{RT}). Normally these pins should have 0.1 microfarad capacitors to AGND; this helps reduce the INL errors by stabilizing the reference ladder voltages. These taps can also be used to alter the transfer curve of the ADC. A four segment, piecewise linear, custom transfer curve can be designed by connecting voltage sources to these pins. (See *Figure 7.*)

24 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

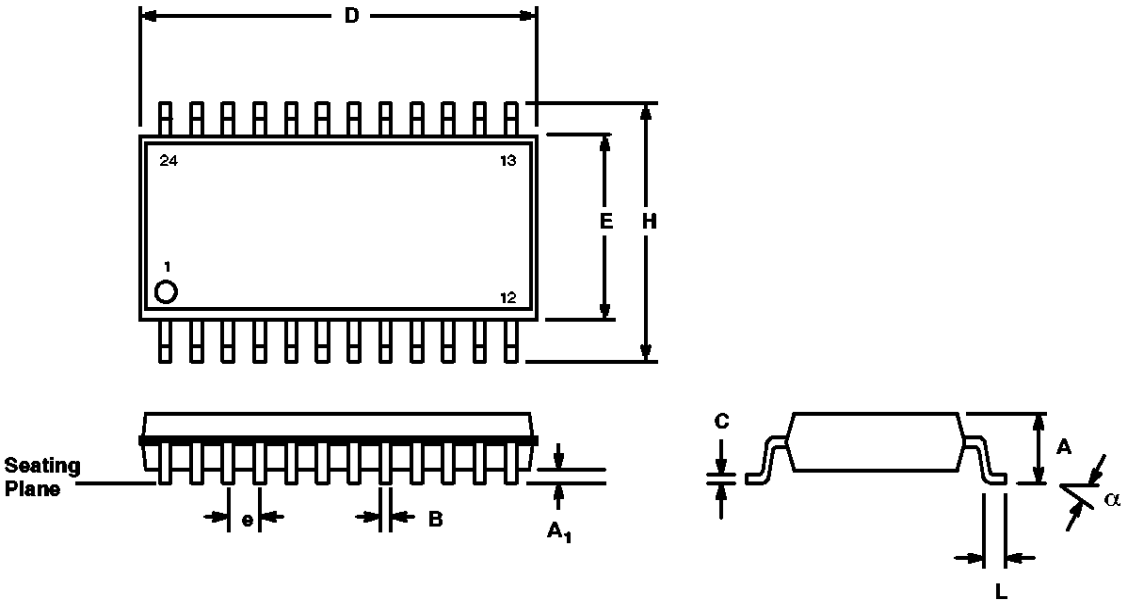


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	1.125	1.275	28.58	32.39
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

24 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

Notes

NOTICE

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Datasheet January 1999