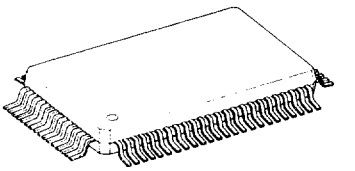
T6A85

TENTATIVE DATA

DOT MATRIX LCD CONTROLLER

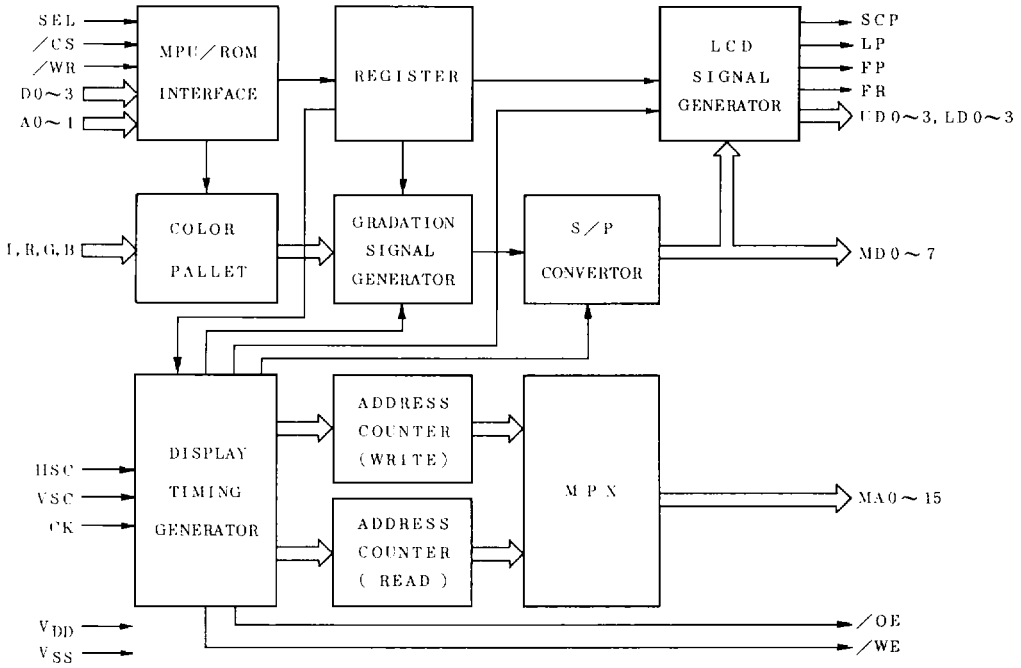
The T6A85 is a dot matrix LCD controller that is fabricated by low power and high speed CMOS silicon gate technology. This LSI converts video signals for CRT display into LCD signals, and can display 16-level gray scale data corresponding to the video I,R,G,B signals with an existing LCD driver. Therefore, a CRT display is replaced by a LCD panel without any software changes. A display size is selected by a program from 320×200 to 720×512(maximum).



QFP80-P-1420A

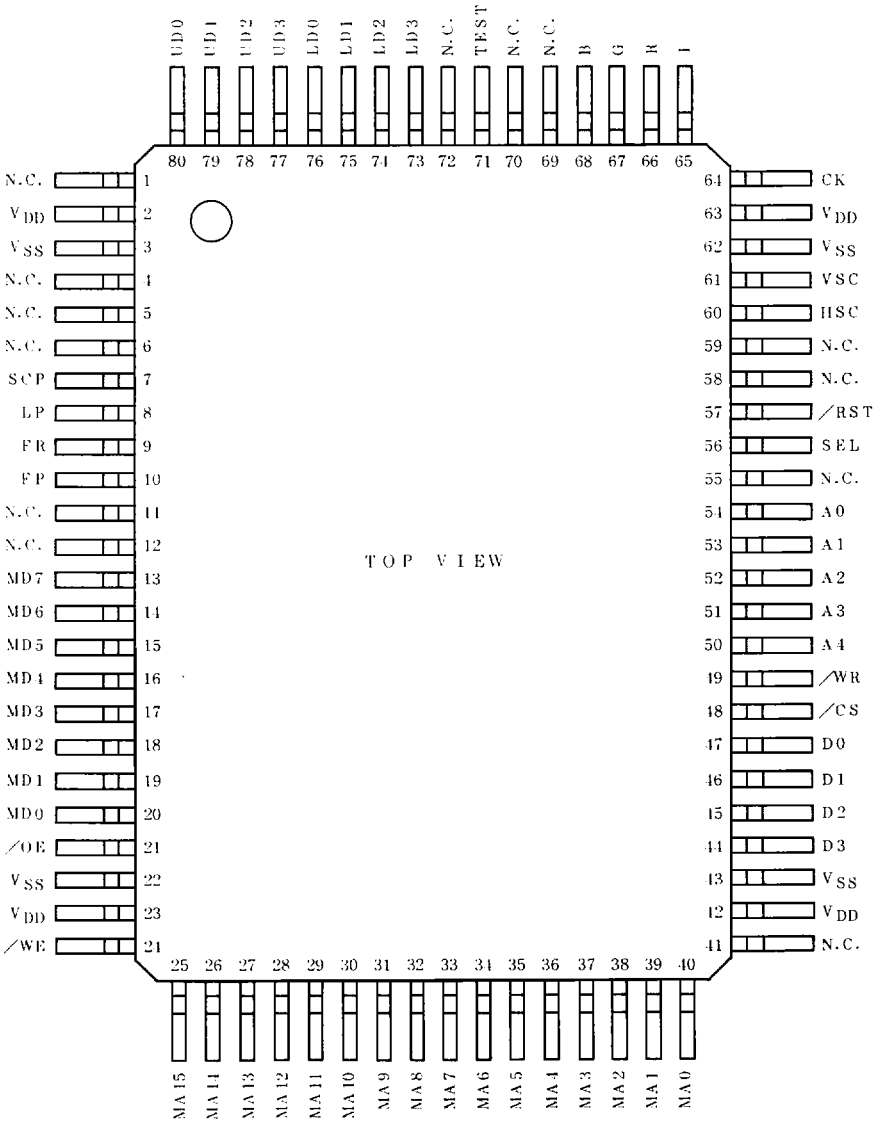
- Display 16-level gray scale data
  Convert 4-bit video data I,R,G,B for CRT display into LCD signals
  Gray scale level is selected by pallet function
  Can use existing LCD driver
- LCD screen size
  320×200, 640×200, 640×350, 640×400, 640×480, 720×400, 720×480, 720×512
- LCD interface
  1-screen/2-screen mode
  4bit-bus/8bit-bus(8bit-bus is available in 1-screen mode only)
- CRT interface
  TTL compatible input
  Maximum dot frequency : 30MHz
  Display position on LCD screen is adjustable
- MPU interface
  A various modes and screen sizes are selected by a MPU program
- Memory interface
  Direct control up to 45k bytes S-RAM as a buffer memory
  A buffer memory is not necessary in 1-screen mode
- Single +5V power supply with 10% voltage margine
- C-MOS, Si-Gate structure
- 80pin plastic flat package

BLOCK DIAGRAM



PIN FUNCTION

PIN CONFIGURATION



PIN DESCRIPTION

PIN NAME	PIN No.	I/O/Z	FUNCTION
MA0~15	40~25	O	Memory address to frame buffer memory
MD0~7	20~13	I/O	Bidirectional data bus to frame buffer memory
/WE	24	O	Write enable signal to frame buffer memory
/OE	21	O	Output enable signal to frame buffer memory
D0~3	47~44	I	Data bus input for internal register
A0~4	54~50	I/O	Bidirectional address bus for internal register
/CS	48	I	Chip select signal input
/WR	49	I	Write signal input
SEL	56	I	Select register write method(ROM/MPU)
/RST	57	I	Reset signal input
I,R,G,B	65~68	I	Video data input
CK	64	I	Dot clock input
HSC	60	I	Horizontal sync signal input
VSC	61	I	Vertical sync signal input
UD0~3	80~77	O	Data bus for column driver
LD0~3	76~73	O	Data bus for column driver
SCP	7	O	Shift clock pulse for column driver
LP	8	O	Latch pulse for column driver, Shift clock pulse for row driver
FP	10	O	Synchronous signal for row driver
FR	9	O	Alternating signal for LCD
TEST	71	I	Test terminal(Normaly open)
V_{DD}	2,23,42,63		Power supply(+5V)
V_{SS}	3,22,43,62		Power supply(0V)

FUNCTIONAL DESCRIPTION

MPU INTERFACE

The T6A85 has two methods to program internal registers. One is a MPU programing method and the other is a ROM programing method. These two method are selected by SEL terminal. The relation between programing method and SEL is as follows:

SEL	Programing Method
"0"	MPU programing method (/CS=0, /WR=positive edge)
"1"	ROM programing method (/CS=0 or 1, /WR=0 or 1)

MODE REGISTERS

The mode registers determine a screen size, a screen position, a display size, a LCD interface method and a polarity of video signal.

Register Address					Register		Data			
A4	A3	A2	A1	A0	NO	Register	D3	D2	D1	D0
0	0	0	0	0	R0	Horizontal Backporch Register (L)	K3	K2	K1	K0
0	0	0	0	1	R1	Horizontal Backporch Register (H)	K7	K6	K5	K4
0	0	0	1	0	R2	Vertical Backporch Register (L)	L3	L2	L1	L0
0	0	0	1	1	R3	Vertical Backporch Register (H)	L7	L6	L5	L4
0	0	1	0	0	R4	Not Use				
0	0	1	0	1	R5					
0	0	1	1	0	R6					
0	0	1	1	1	R7					
0	1	0	0	0	R8	Screen Size Register	S3	S2	S1	S0
0	1	0	0	1	R9	Operating Mode Register	S7	S6	S5	S4
0	1	0	1	0	R10	Video Signal Polarity Register	P3	P2	P1	P0
0	1	0	1	1	R11	Display Size Register	M3	M2	M1	M0
0	1	1	0	0	R12	Not Use				
0	1	1	0	1	R13					
0	1	1	1	0	R14					
0	1	1	1	1	R15	Test Register	-	-	T1	T0

When /RST is "0", R0~R3 and R8~R11 are all "0".

When /RST is "0", T0 and T1 of R15 are all "1". T0 and T1 of R15 must be "1".

1. Horizontal Backporch Register (R0,R1)

A[4:0]	D3	D2	D1	D0
0	K3	K2	K1	K0
1	K7	K6	K5	K4

A[4:0]=[A4,A3,A2,A1,A0]
MSB LSB

This 8-bit write-only register specifies a horizontal backporch. The horizontal backporch is a number of dots between the edge of HSC and the valid I,R,G,B. The value programmed in this register is one less than the number of horizontal backporch.

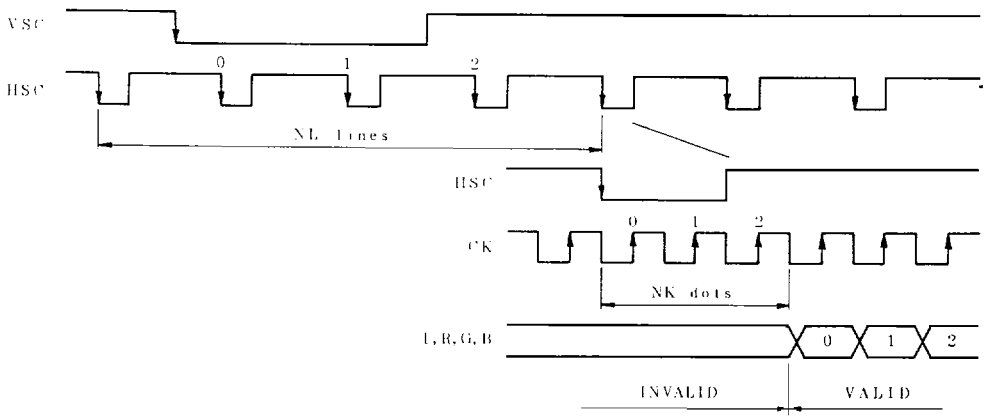
2. Vertical Backporch Register (R2,R3)

A[4:0]	D3	D2	D1	D0
2	L3	L2	L1	L0
3	L7	L6	L5	L4

A[4:0]=[A4,A3,A2,A1,A0]
MSB LSB

This 8-bit write-only register specifies a vertical backporch. The vertical backporch is a number of lines between the edge of VSC and the 1'st valid I,R,G,B. The value programmed in this register is two less than the number of vertical backporch.

Ex.) Condition: P1=0, P2=0, P3=0 (R10)



Note) When Vertical backporch NL=4 and Horizontal backporch NK=3

L[7:0]=NL-2=2

K[7:0]=NK-1=2

3. Screen Size Register (R8)

A[4:0]	D3	D2	D1	D0
8	S3	S2	S1	S0

A[4:0]=[A4,A3,A2,A1,A0]
MSB LSB

This 4-bit write-only register specifies a LCD screen size. The relation between S0,S1,S2,S3 and the screen size is as follows:

S3	S2	S1	Screen Size (Column×Row)
0	0	0	640×400
0	0	1	640×200
0	1	0	640×480
0	1	1	640×350
1	0	0	720×400
1	0	1	720×480
1	1	0	720×512
1	1	1	320×200

S0	Screen Configuration
0	Dual Screen
1	Single Screen

4. Operating Mode Register (R9)

A[4:0]	D3	D2	D1	D0
9	S7	S6	S5	S4

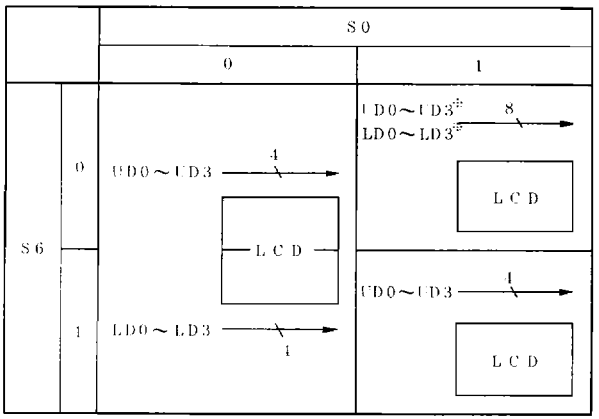
A[4:0]=[A4,A3,A2,A1,A0]
MSB LSB

This 4-bit write-only register specifies an operating mode. The relation between S4,S5,S6,S7 and the operating mode is as follows:

S4	Stand by Mode
0	OFF
1	ON

S5	FR Wave Form
0	For Gray Scale
1	For Black/White

S6	LCD Interface
0	8-bit
1	4-bit



※:MD[7,6,5,4,3,2,1,0]=LD[3,2,1,0],UD[3,2,1,0]

S7	Gray Scale (On period ratio)									
	0	1	2	3	4	5	6	7	8	9
0	0/16	1/16	2/16	3/16	4/16	5/16	6/16	7/16	8/16	9/16
1	0/16	2/16	3/16	4/16	5/16	6/16	7/16	8/16	9/16	10/16

S7	Gray Scale (On period ratio)					
	10	11	12	13	14	15
0	10/16	11/16	12/16	13/16	14/16	16/16
1	11/16	12/16	13/16	14/16	15/16	16/16

(Unit:Frame)

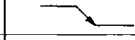
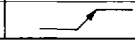
5. Video Signal Polarity Register (R10)

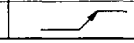
A[4:0]	D3	D2	D1	D0
A(hex)	P3	P2	P1	P0

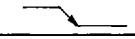
A[4:0]=[A4,A3,A2,A1,A0]
MSB LSB

This 4-bit write-only register specifies a video signal polarity. The relation between P0,P1,P2,P3 and the polarity is as follows:

P0	I,R,G,B
0	Invert
1	Non-invert

P1	HSC
0	
1	

P2	VSC
0	
1	

P3	CK
0	
1	

6. Display Size Register (R11)

A[4:0]	D3	D2	D1	D0
B(hex)	M3	M2	M1	M0

A[4:0]=[A4,A3,A2,A1,A0]
MSB LSB

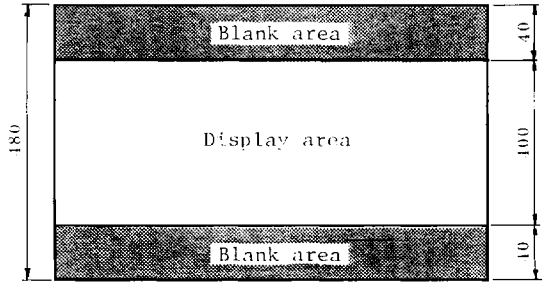
This 4-bit write-only register specifies a display size. The relation between M0,M1,M2,M3 and the display size is as follows:

M3	M2	M1	Display Size (Column×Row)
0	0	0	640×400
0	0	1	640×200
0	1	0	640×480
0	1	1	640×350
1	0	0	720×400
1	0	1	720×480
1	1	0	720×512
1	1	1	320×200

M0	Doubled-in-height Display
0	ON
1	OFF

The T6A85 can be set the display size that is different from the LCD panel size. However, S3 must be equal to M3. And, when [S3,S2,S1] are all "1", [M3,M2,M1] must be all "1".

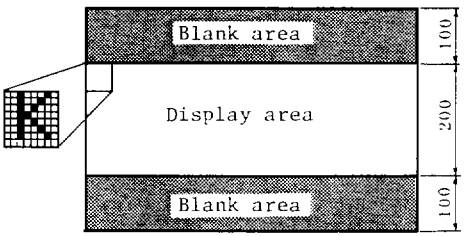
Ex.) 640×480 LCD Module



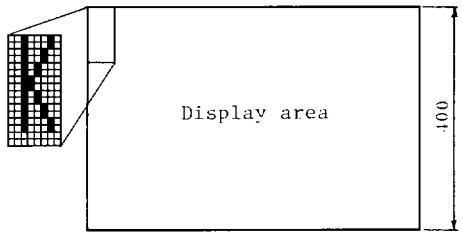
[S3,S2,S1]=[0,1,0]
[M3,M2,M1]=[0,0,0]

When [S3,S2,S1]=[0,0,0] / [M3,M2,M1]=[0,0,1] or [S3,S2,S1]=[0,1,0] / [M3,M2,M1]=[0,0,1], the doubled-in-height display is available.

Ex.) 640×400 LCD Module

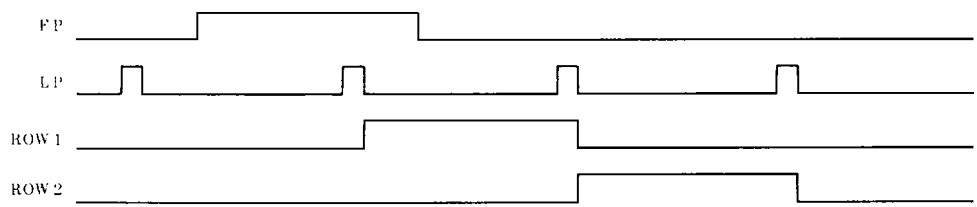


[S3,S2,S1]=[0,0,0]
[M3,M2,M1]=[0,0,1]
[M0]=[1]

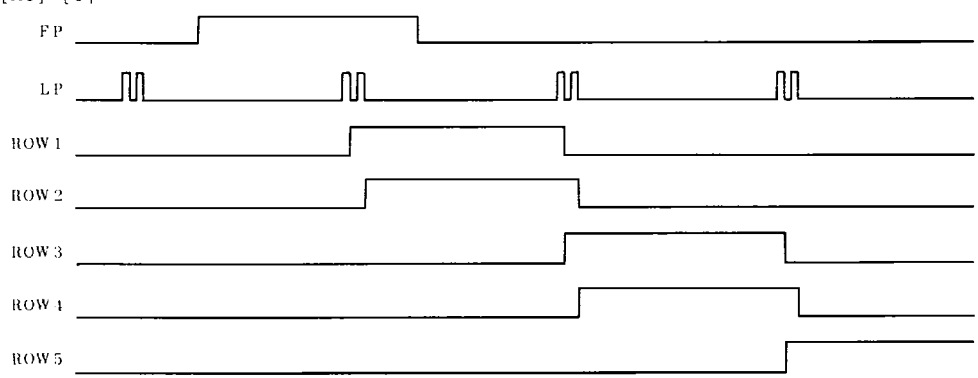


[S3,S2,S1]=[0,0,0]
[M3,M2,M1]=[0,0,1]
[M0]=[0]

[M0]=[1]



[M0]=[0]



COLOR PALETTE REGISTERS

The color palette registers determine the relation between a color data and a palette data.

Register Address					Palette No.	Color Data (Preset Value)				Gray Scale No.
A4	A3 I	A2 R	A1 G	A0 B		D3	D2	D1	D0	
1	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0	1	1
1	0	0	1	0	2	0	0	1	0	2
1	0	0	1	1	3	0	0	1	1	3
1	0	1	0	0	4	0	1	0	0	4
1	0	1	0	1	5	0	1	0	1	5
1	0	1	1	0	6	0	1	1	0	6
1	0	1	1	1	7	0	1	1	1	7
1	1	0	0	0	8	1	0	0	0	8
1	1	0	0	1	9	1	0	0	1	9
1	1	0	1	0	10	1	0	1	0	10
1	1	0	1	1	11	1	0	1	1	11
1	1	1	0	0	12	1	1	0	0	12
1	1	1	0	1	13	1	1	0	1	13
1	1	1	1	0	14	1	1	1	0	14
1	1	1	1	1	15	1	1	1	1	15

BUFFER MEMORY

The T6A85 needs the external memory except when [S1,S2,S3]=[M1,M2,M3] and S0="1".
The relation between the screen size and the memory is as follows:

	320×200 62.5kbit	640×200 125kbit	640×350 218.8kbit	640×400 250kbit	640×480 300kbit	720×400 281.3kbit	720×480 337.5kbit		720×512 360kbit	
64k SRAM	1	2			1	1		2		2
256kSRAM			1	1	1	1	2	1	2	1

The T6A85 accesses the memory on a $4t_{CKC}$ cycle. The t_{CKC} is a dot clock cycle.

i) In the case f_{CK}=16MHz
$4t_{CKC}=4\times(1/16MHz)=250ns$
ii) In the case f_{CK}=24MHz
$4t_{CKC}=4\times(1/24MHz)=167ns$
iii) In the case f_{CK}=30MHz
$4t_{CKC}=4\times(1/30MHz)=133ns$

Prepared RAM:
64k SRAM=TC5565APL-12
256k SRAM=TC55257BPL-10

MAXIMUM RATINGS

ITEM	SYMBOL	TEST CONDITION	RATING	UNIT
Power Supply Voltage	V_{DD}	Ta=25°C	-0.3~7.0	V
Input Voltage	V_{IN}	Ta=25°C	-0.3~V_{DD}+0.3	V
Operating Temperature	T_{opr}		-20~75	°C
Storage Temperature	T_{stg}		-55~125	°C

Note: All voltage values referenced to V_{SS}=0V

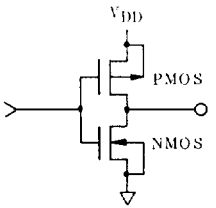
ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

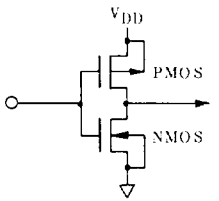
(Unless otherwise specified, V_{DD}=5.0V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Operating Voltage	V_{DD}		4.5	-	5.5	V	
"1" Input Voltage	V_{IH}		2.0	-	-	V	I,R,G,B,CK,HSC, VSC MD0~7,A0~4,D0~3 /CS,/WR,/RST,SEL
"0" Input Voltage	V_{IL}		-	-	0.8	V	
"H" Output Voltage 1	V_{OH1}	I_{OH}=-0.2mA	2.4	-	-	V	MD0~7,A0~4,MA0~15
"L" Output Voltage 1	V_{OL1}	I_{OL}=1.6mA	-	-	0.4	V	/WE,/OE
"H" Output Voltage 2	V_{OH2}	I_{OH}=-0.2mA	V_{DD}-0.8	-	-	V	UD0~3,LD0~3
"L" Output Voltage 2	V_{OL2}	I_{OL}=0.2mA	-	-	0.8	V	SCP,LP,FP,FR
Input Leakage Current	I_{IL}	V_{IN}=0~V_{DD}	-1	-	1	μA	I,R,G,B,CK,HSC, VSC,MD0~7,A0~4, D0~3, /CS,/WR,/RST,SEL
Pull Up MOS Current	-IP	V_{DD}=5.0V Ta=25°C	20	50	100	μA	TEST,MD0~7,A0~4
Operating Frequency	f_{CK}		-	-	30	MHz	CK
Current Consumption	I_{DD}	V_{DD}=5.0V f_{CK}=30MHz	-	-	30	mA	

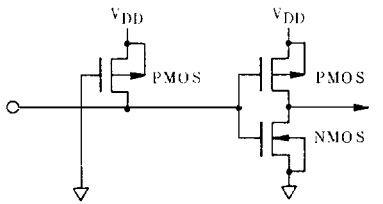
. OUTPUT TERMINAL : MA0~15, /WE, /OE, UD0~3, LD0~3, SCP, LP, FP, FR



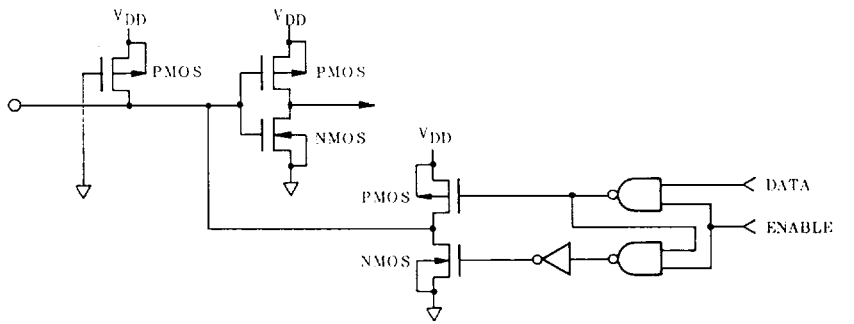
. INPUT TERMINAL : I,R,G,B,CK,HSC,VSC,D0~3,/CS,/WR,/RST,SEL



. INPUT TERMINAL (WITH PULL UP) : TEST



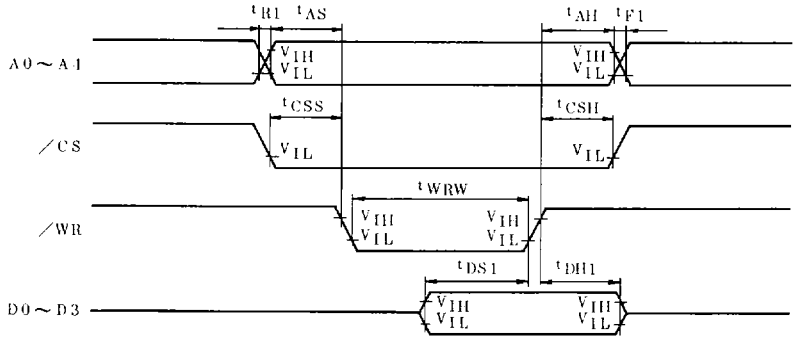
. I/O TERMINAL : MD0~7, A0~4



AC CHARACTERISTICS

1. REGISTER PROGRAMING

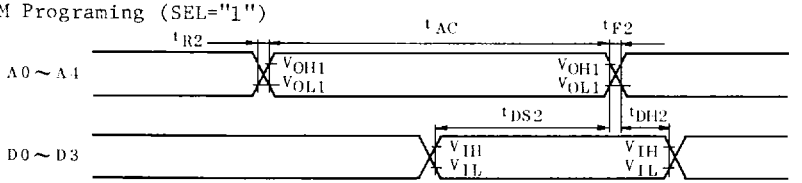
. MPU Programing (SEL="0")



(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Signal Rise/Fall Time	t_{R1}/t_{F1}	Except CK	-	-	10	ns
A0~A4 Set Up Time	t_{AS}		50	-	-	ns
A0~A4 Hold Time	t_{AH}		50	-	-	ns
/CS Set Up Time	t_{CSS}		50	-	-	ns
/CS Hold Time	t_{CSH}		50	-	-	ns
/WR Pulse Width	t_{WRW}		50	-	-	ns
D0~D3 Set Up Time	t_{DS1}		100	-	-	ns
D0~D3 Hold Time	t_{DH1}		50	-	-	ns

. ROM Programing (SEL="1")

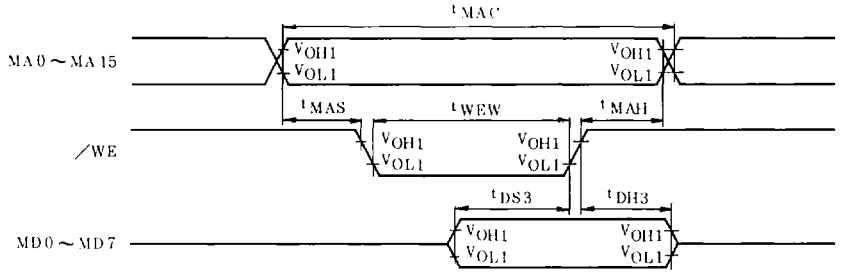


(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Signal (TTL) Rise/Fall Time	t_{R2}/t_{F2}		-	-	20	ns
A0~A4 Cycle Time	t_{AC}		$32t_{CKC}$-100	-	-	ns
D0~D3 Set Up Time	t_{DS2}		t_{CKC}+50	-	-	ns
D0~D3 Hold Time	t_{DH2}		0	-	-	ns

2. RAM INTERFACE

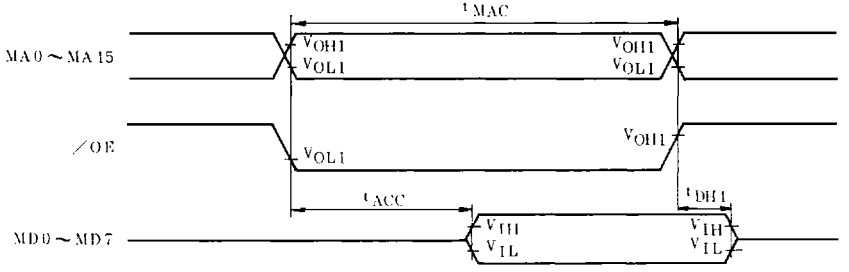
. Write Cycle



(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
MA0~MA15 Cycle Time	t_{MAC}		$4t_{CKC}$	-	-	ns
MA0~MA15 Set Up Time	t_{MAS}		$0.5t_{CKC}$-14	-	-	ns
MA0~MA15 Hold Time	t_{MAH}		$0.5t_{CKC}$-14	-	-	ns
/WE Pulse Width	t_{WEW}		$3t_{CKC}$-20	-	-	ns
MD0~MD7 Set Up Time	t_{DS3}		$3t_{CKC}$-14	-	-	ns
MD0~MD7 Hold Time	t_{DH3}		5	-	-	ns

. Read Cycle

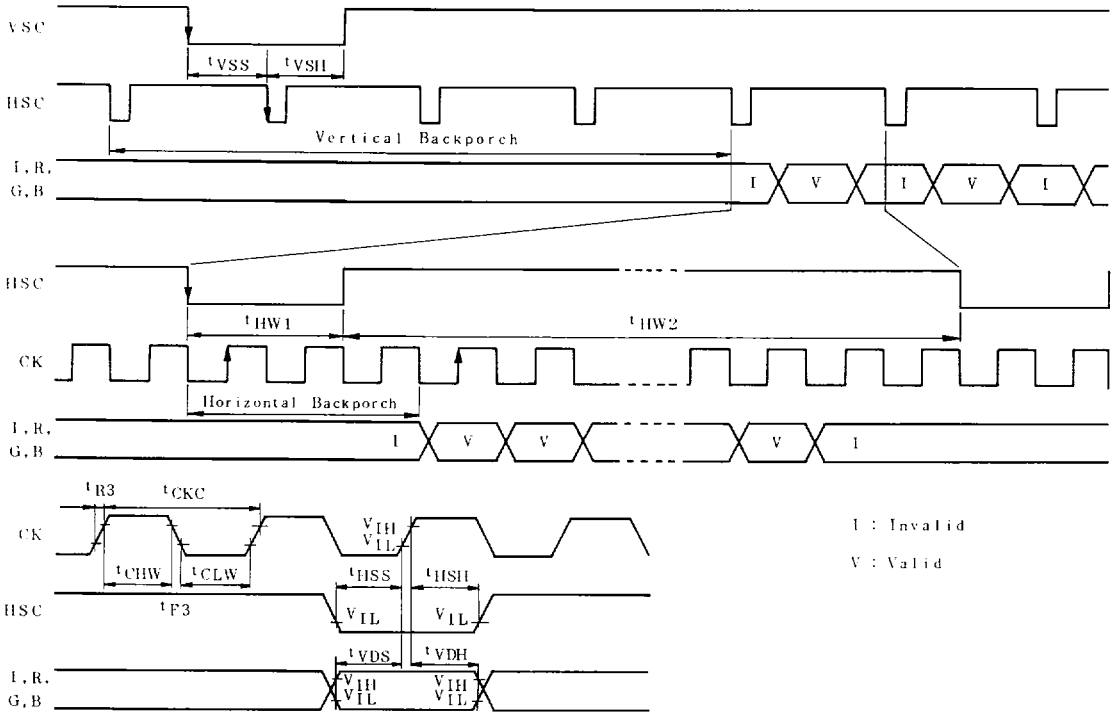


(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
MA0~MA15 Cycle Time	t_{AC}		$4t_{CKC}$	-	-	ns
MD0~MD7 Access Time	t_{ACC}		-	-	$4t_{CKC}$-20	ns
MD0~MD7 Hold Time	t_{DH4}		10	-	-	ns

3. VIDEO INTERFACE

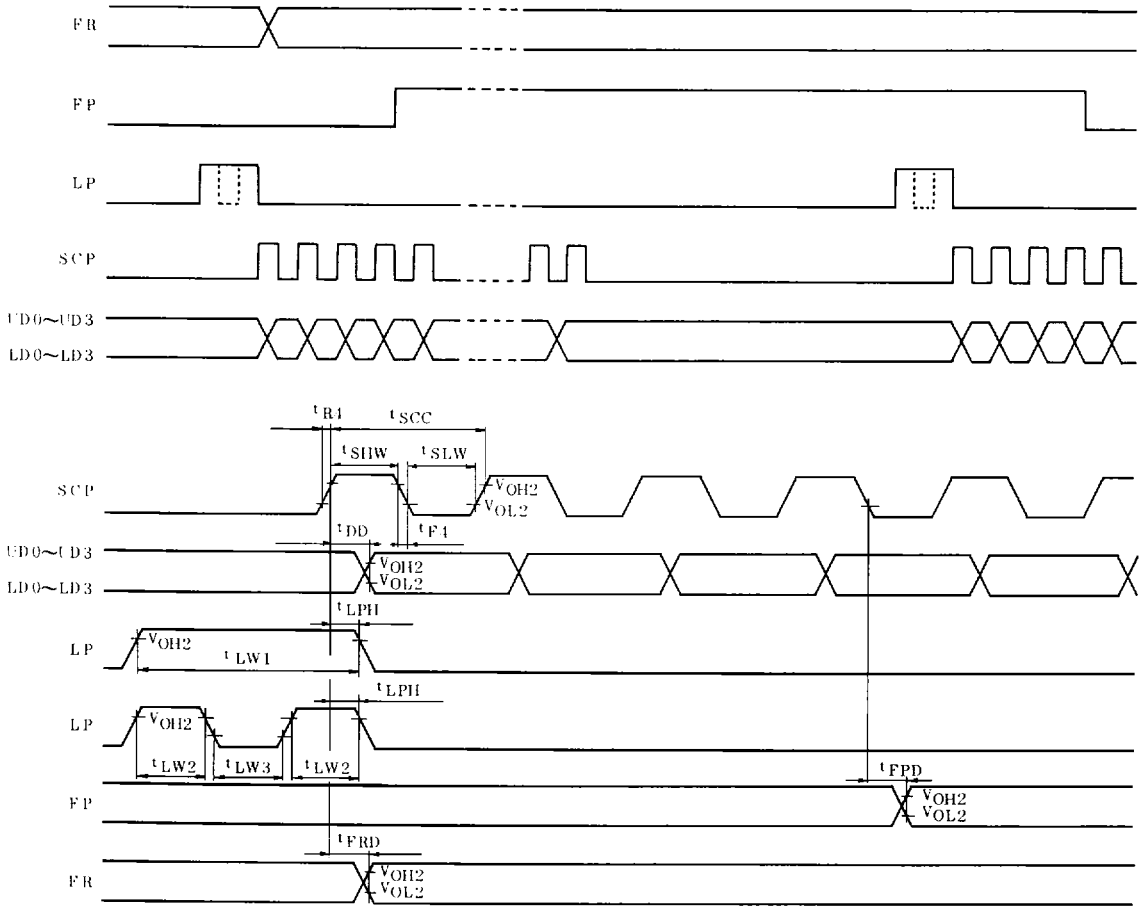
In the case P1="0", P2="0", P3="0":



(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CK Rise/Fall Time	t_{R3}/t_{F3}		-	-	5	ns
CK Cycle Time	t_{CKC}		33	-	-	ns
CK "1" Pulse Width	t_{CHW}		12	-	-	ns
CK "0" Pulse Width	t_{CLW}		12	-	-	ns
VSC Set Up Time	t_{VSS}		20	-	-	ns
VSC Hold Time	t_{VSH}		20	-	-	ns
HSC Enable Pulse Width	t_{HW1}		t_{CKC}	-	-	ns
HSC Disable Pulse Width	t_{HW2}		t_{CKC}	-	-	ns
HSC Set Up Time	t_{HSS}		6	-	-	ns
HSC Hold Time	t_{HSH}		14	-	-	ns
I,R,G,B Set Up Time	t_{VDS}		4	-	-	ns
I,R,G,B Hold Time	t_{VDH}		12	-	-	ns

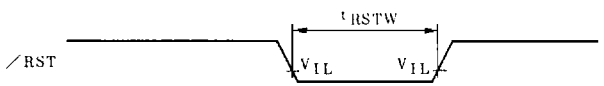
4. LCD INTERFACE



(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SCP Cycle Time	t_{SCC}	S0,S6="1,1"	$4t_{CKC}$	-	-	ns
		Others	$8t_{CKC}$	-	-	
SCP "1" Pulse Width	t_{SHW}	S0,S6="1,1"	$2t_{CKC}$-20	-	-	ns
		Others	$4t_{CKC}$-20			
SCP "0" Pulse Width	t_{SLW}	S0,S6="1,1"	$2t_{CKC}$-20	-	-	ns
		Others	$4t_{CKC}$-20	-	-	
Output Signal(CMOS) Rise/Fall Time	t_{R4}/t_{F4}		-	-	20	ns
UD0~UD3, LD0~LD3 Delay Time	t_{DD}		-20	-	20	ns
LP Hold Time	t_{LPH}		-30	-	0	ns
LP Pulse Width 1	t_{LW1}		$6t_{CKC}$-20	-	-	ns
LP Pulse Width 2	t_{LW2}		$2t_{CKC}$-20	-	-	ns
LP Pulse Width 3	t_{LW3}		$2t_{CKC}$-20	-	-	ns
FP Delay Time	t_{FPD}		-20	-	20	ns
FR Delay Time	t_{FRD}		-20	-	20	ns

5. RESET

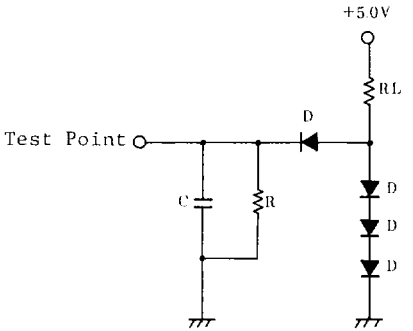


(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
/RST Pulse Width	t_{RSTW}		1.0	-	-	μs

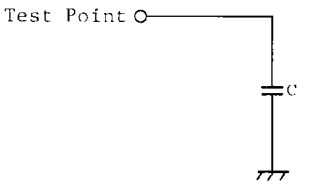
6. LOAD CIRCUIT

. TTL Load



RL=2.4kΩ
R=10kΩ
C=40pF(Including wiring capacity)
D=1S1588
Pin:MD0~7, A0~4, MA0~15, /WE, /OE

. Capacitive Load



C=40pF(Including wiring capacity)
Pin:UD0~3, LD0~3, SCP, LP, FP, FR

APPLICATION

EVALUATION BOARD

The T6A85 EV BOARD is prepared in order to evaluate the T6A85 in a short time. The EV BOARD contains RAM, ROM and some logic ICs. Any of ROM/MPU can determine the T6A85's internal registers. If only the video signals and the LCD module are connected to the EV BOARD, it is possible to evaluate the T6A85.

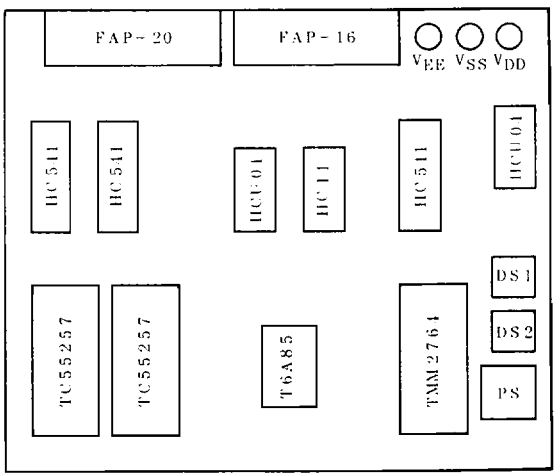
1. SPECIFICATIONS

The following figure shows the EV BOARD specification.

LCD Controller		T6A85
Frame Buffer Memory		TC55257×2
Program ROM		TMM2764
Video Interface	Input Level	I,R,G,B TTL-Level Separate Signal (Digital)
	Input Connector	FAP-16(YAMAICHI)
MPU Interface	Input Level	TTL-Level Signal
	Input Connector	DIP28
LCD Interface	Output Level	CMOS-Level Signal
	Output Connector	FAP-20(YAMAICHI)
Power Supply		5V±10%
Speed		30MHz max.
Current Consumption		100mA max.
Board Size		110mm×130mm

2. EV BOARD LAYOUT

The following figure shows the EV BOARD layout.



3. RECOMMENDED COMPONENTS

The following figure shows the recommended components.

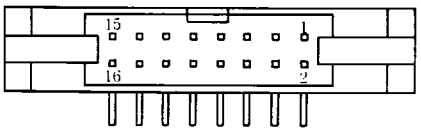
COMPONENT	NAME/VALUE	Q'TY	MAKER	DESCRIPTION
IC	T6A85	1	TOSHIBA	LCD Controller, QFP80
	TC55257	2	TOSHIBA	256kbit SRAM, DIP28
	TMM2764	1	TOSHIBA	64kbit PROM, DIP28
	TC74HCU04	2	TOSHIBA	Inverter, DIP14
	TC74HC14	1	TOSHIBA	Schmitt Inverter, DIP14
	TC74HC541	3	TOSHIBA	Non-Inverting Buffer, DIP20
Resistor	3.3k×8	1		0.25-watt, 10%
	10k×8	1		0.25-watt, 10%
	2.2k	1		0.25-watt, 10%
	10k	1		0.25-watt, 10%
	33k	1		0.25-watt, 10%
	100k	1		0.25-watt, 10%
Capacitor	220pF	1		50V, Ceramic
	0.1μF	13		50V, Ceramic
	10μF	2		16V
Diode	1S1538	1	TOSHIBA	
Socket	28pin DIP	1		ROM Socket or MPU Interface
Connector	FAP-16-07#2	1	YAMAICHI	Video Interface Connector
	FAP-20-07#2	1	YAMAICHI	LCD Interface Connector
Jumper Plug	UFP-06A-03#4	1	YAMAICHI	
	UFP-10A-03#4	2	YAMAICHI	
Short Plug	DIC-252	5	HONDA	
Switch	KDS16-422	2	KEL	Dip Switch (4bit)
	DP1-100-C	1	FUJISOKU	Push Switch
Terminal	T-16	3	SATO PARTS	

4. INTERFACE CONNECTORS

. Vidro Interface Connector

The following figure shows the pin assignment of the video interface connector.

FAP-16-07#2

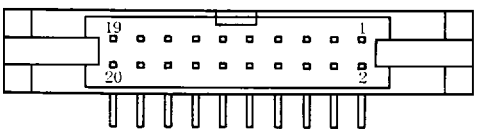


Pin No.	Signal Name	Pin No.	Signal Name
1	B	2	GND
3	G	4	GND
5	R	6	GND
7	I	8	GND
9	VSC	10	GND
11	HSC	12	GND
13	CK	14	GND
15	GND	16	GND

. LCD Interface Connector

The following figure shows the pin assignment of the LCD interface connector.

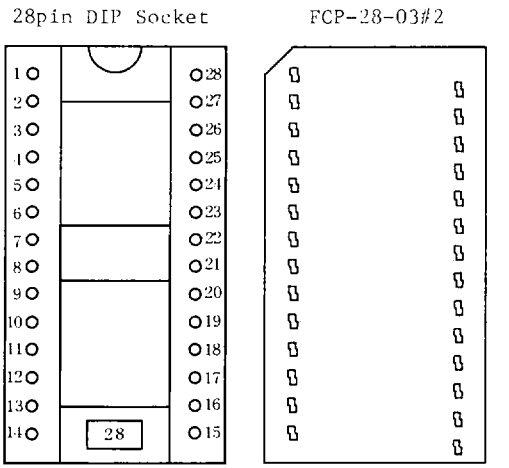
FAP-20-07#2



Pin No.	Signal Name	Pin No.	Signal Name
1	UD0	2	UD1
3	UD2	4	UD3
5	LD0	6	LD1
7	LD2	8	LD3
9	SCP	10	LP
11	FP	12	FR
13	N.C.	14	N.C.
15	V_{DD}	16	V_{DD}
17	V_{SS}	18	V_{SS}
19	V_{EE}	20	V_{EE}

. MUP Interface Connector

The following figure shows the pin assignment of the MPU interface connector.



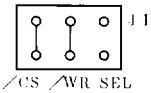
Recommended Connector

Pin. No.	Sugnal Name	Pin No.	Signal Name
1	N.C.	28	N.C.
2	N.C.	27	N.C.
3	N.C.	26	N.C.
4	N.C.	25	N.C.
5	N.C.	24	N.C.
6	A4	23	N.C.
7	A3	22	/OE
8	A2	21	N.C.
9	A1	20	/CE
10	A0	19	N.C.
11	D0	18	N.C.
12	D1	17	N.C.
13	D2	16	N.C.
14	GND	15	D3

5. ROM PROGRAMMING METHOD (SEL="1")

A ROM is mounted on the EV BOARD. It contains the registers data. The data is divided into 256 pages. The page is selected by two DIP code switches on the EV BOARD. The ROM programing method is shoen as follows:

i) Set J1 switches
/CS=ON
/WR=ON
SEL=OFF



ii) Set DS1,DS2 DIP code switches
DS2=[A12,A11,A10,A9]=0~F(hex.)
DS1=[A8,A7,A6,A5]=0~F (hex.)
DS2·DS1=[A12,A11,A10,A9]·[A8,A7,A6,A5]=00~FF (hex.)

iii) Example data

Page Address	Register Address					Reg. No.	Data				Note
A12~A5	A4	A3	A2	A1	A0		D3	D2	D1	D0	
0000 0000 (0 page)	0	0	0	0	0	R0	0	0	1	1	K=93H
	0	0	0	0	1	R1	1	0	0	1	
	0	0	0	1	0	R2	0	0	0	0	L=20H
	0	0	0	1	1	R3	0	0	1	0	
	0	0	1	0	0	R4	1	1	1	1	
	0	0	1	0	1	R5	1	1	1	1	
	0	0	1	1	0	R6	1	1	1	1	
	0	0	1	1	1	R7	1	1	1	1	
	0	1	0	0	0	R8	0	0	0	0	Screen size=640×400, Dual Screen Operating mode
	0	1	0	0	1	R9	0	0	0	0	
	0	1	0	1	0	R10	0	0	0	1	Signal polarity=Non-invert,HSC↓,VSC↓CK↑
	0	1	0	1	1	R11	0	0	0	1	
	0	1	1	0	0	R12	1	1	1	1	Disp. size=640×400, Doubled-in-height OFF
	0	1	1	0	1	R13	1	1	1	1	
	0	1	1	1	0	R14	1	1	1	1	
	0	1	1	1	1	R15	1	1	1	1	
	1	0	0	0	0		0	0	0	0	Color palette
	1	0	0	0	1		0	0	0	1	
	1	0	0	1	0		0	0	1	0	
	1	0	0	1	1		0	0	1	1	
	1	0	1	0	0		0	1	0	0	
	1	0	1	0	1		0	1	0	1	
	1	0	1	1	0		0	1	1	0	
	1	0	1	1	1		0	1	1	1	
	1	1	0	0	0	Pale.	1	0	0	0	
	1	1	0	0	1		1	0	0	1	
	1	1	0	1	0		1	0	1	0	
	1	1	0	1	1		1	0	1	1	
	1	1	1	0	0		1	1	0	0	
	1	1	1	0	1		1	1	0	1	
	1	1	1	1	0		1	1	1	0	
	1	1	1	1	1		1	1	1	1	

iv) ROM data

DIP Switch		Page	Upper Address	Lower Address															
DS2	DS1			0H	1H	2H	3H	4H	5H	6H	7H	8H	9H	AH	BH	CH	DH	EH	FH
0	0	0	000H	3H	9H	0H	2H	FH	FH	FH	FH	0H	0H	1H	1H	FH	FH	FH	FH
			001H	0H	1H	2H	3H	4H	5H	6H	7H	8H	9H	AH	BH	CH	DH	EH	FH
0	1	1	002H																
			003H																
0	2	2	004H																
			005H																
0	3	3	006H																
			007H																
0	4	4	008H																
			009H																
0	5	5	00AH																
			00BH																
0	6	6	00CH																
			00DH																
0	7	7	00EH																
			00FH																
0	8	8	010H																
			011H																
0	9	9	012H																
			013H																
0	A	10	014H																
			015H																
0	B	11	016H																
			017H																
0	C	12	018H																
			019H																
0	D	13	01AH																
			01BH																
0	E	14	01CH																
			01DH																
0	F	15	01EH																
			01FH																
1	0	16	020H																
			021H																
1	1	17	022H																
			023H																
〃	〃	〃																	
F	F	255	1FEH																
			1FFH																

6. MPU PROGRAMING METHOD (SEL="0")

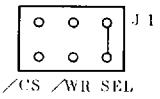
When the MPU programing method is selected, the ROM socket is used to the interface connector. If it is connected to a MPU, it is possible to control the T6A85's registers by the MPU. The MPU programing method is shown as follows:

i) Set J1 switches

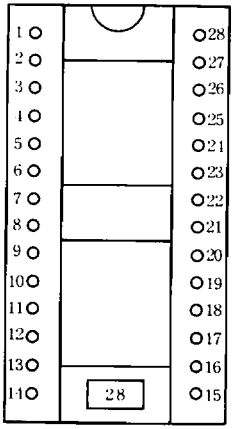
/CS=OFF

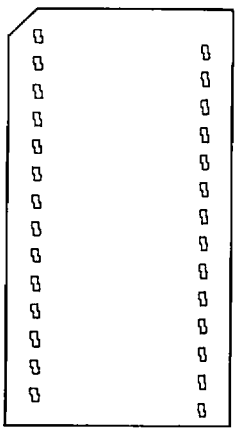
/WR=OFF

SEL=ON



ii) Connect MPU and EV BOARD



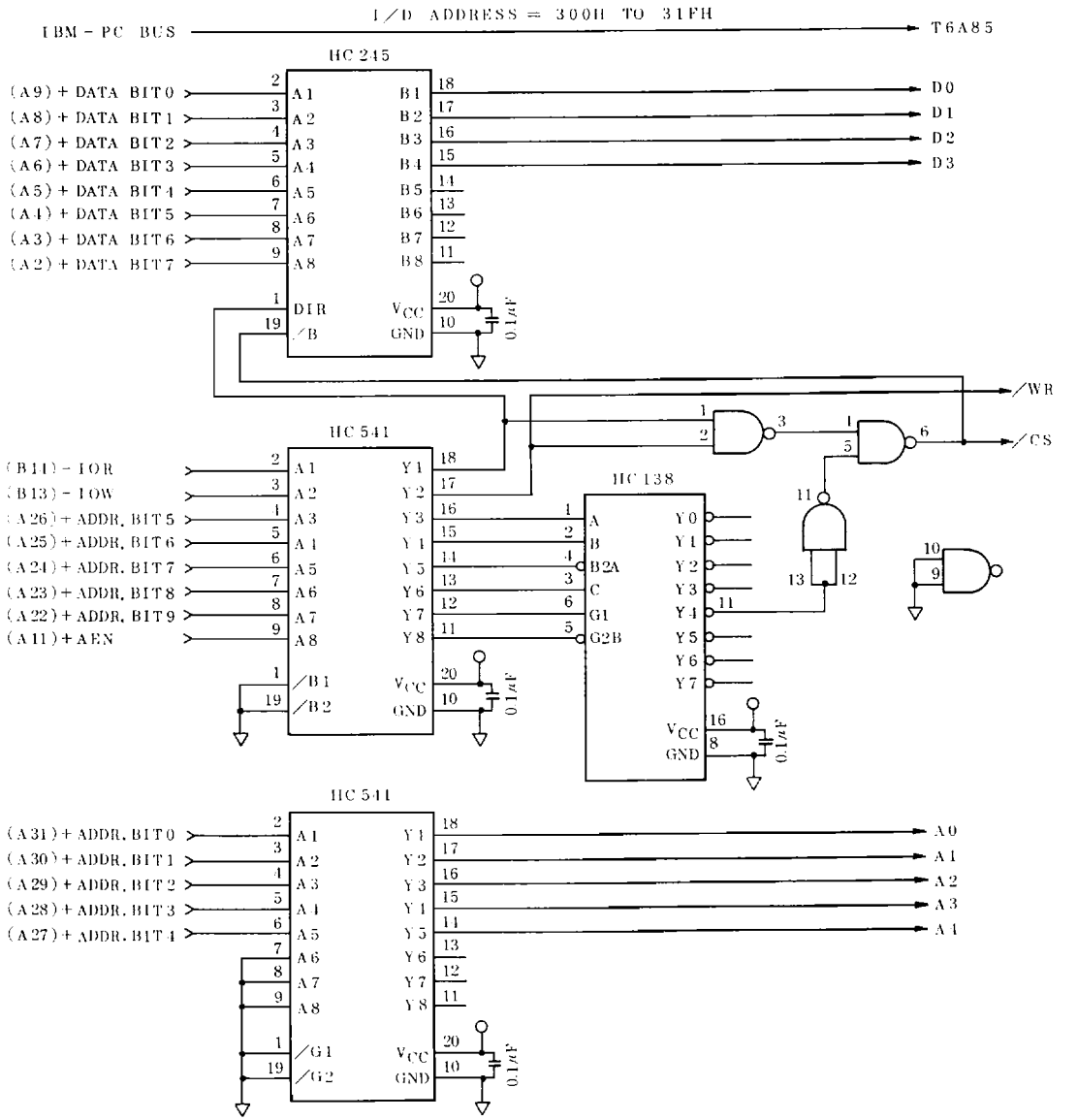


Recommended Connector

Pin No.	Signal Name	Pin No.	Signal Name
1	N.C.	28	N.C.
2	N.C.	27	N.C.
3	N.C.	26	N.C.
4	N.C.	25	N.C.
5	N.C.	24	N.C.
6	A4	23	N.C.
7	A3	22	/OE
8	A2	21	N.C.
9	A1	20	/CE
10	A0	19	N.C.
11	D0	18	N.C.
12	D1	17	N.C.
13	D2	16	N.C.
14	GND	15	D3

. Interface Circuit

An interface circuit between IBM-PC and T6A85 is shown as follows:



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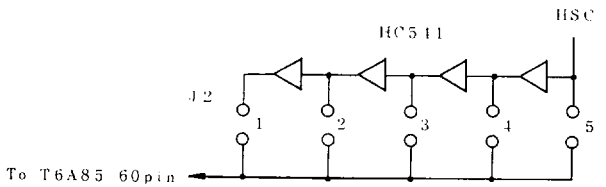
. Interface Program

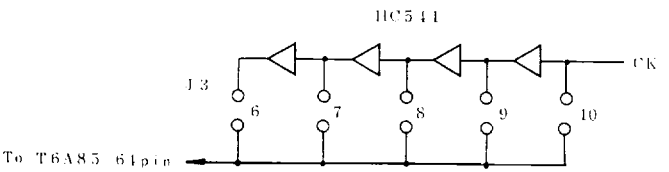
An example BASIC program is shown as follows:

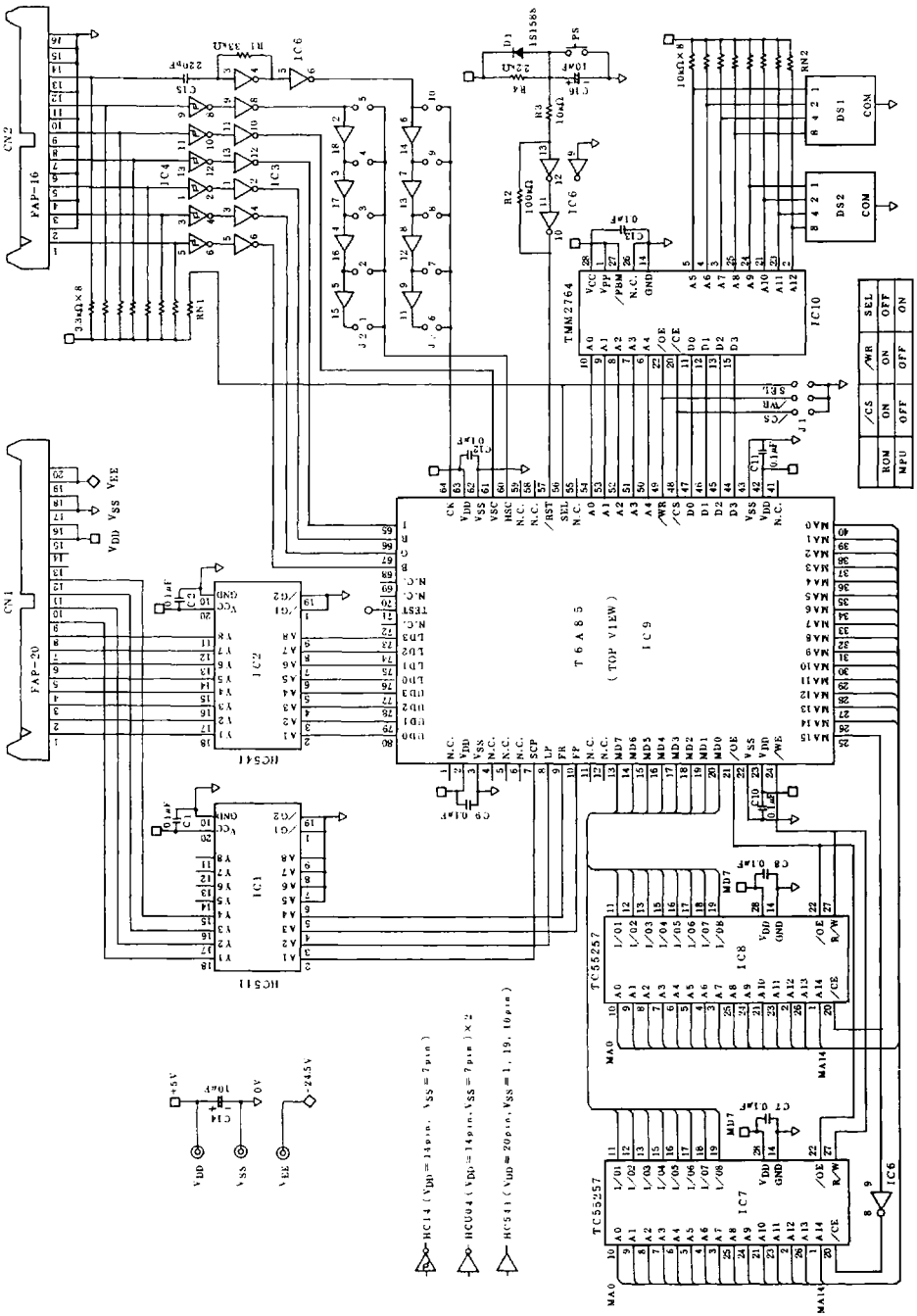
```
10 CMD=&H300
20 FOR I=0 TO 31
30    READ A:OUT CMD+I,A
40 NEXT I
50 DATA &H04,&H09,&H00,&H02,&HFF,&HFF,&HFF,&HFF
60 DATA &H01,&H00,&H01,&H01,&HFF,&HFF,&HFF,&HFF
70 DATA &H00,&H01,&H02,&H03,&H04,&H05,&H06,&H07
80 DATA &H08,&H09,&H0A,&H0B,&H0C,&H0D,&H0E,&H0F
90 END
```

7. ADJUST CK AND HSC

The EV BOARD has two jumper connector to adjust interface timing. J3 is the jumper connector to adjust interface timing between IRGB and CK. J2 is the jumper connector to adjust interface timing between CK and HSC.






CN2
FAP-16
CN1
FAP-20
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
T6A85
(TOP VIEW)
TMM2764
TC55257
HC541
HC14 (VDD=14pin, VSS=7pin)
HCU04 (VDD=14pin, VSS=7pin)×2
HC541 (VDD=20pin, VSS=1, 19, 10pin)
+5V
0V
-24.5V
VDD
VSS
VEE
RON
MPU
/CS
/WR
SEL
ON
OFF